4

Structural Design of a CMOS Voltage Regulator for an Implanted Device

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1. Introduction

There is a great interest in the development of equipment and devices that can accurately and efficiently monitor biological signals such as blood pressure, heart beat and body temperature, among others. It is highly desirable to have those devices operating in an environment free of wires, where the information can be accessed remotely and processed in real time by external equipments.

When the equipments are connected to communication network they form a telemedicine system by which the patients can be monitored remotely (biotelemetry), even over the internet, thus indicating the portability of these instruments (Miyazaki, 2003; Puers, 2005; Scanlon et al, 1996).

Microelectronics has become a powerful tool when used in this scenario. In recent years, integrated circuits are being fabricated with large densities and endowed with intelligence. The reliability of those systems has been increasing and the costs are lowering. The interaction between medicine and technology, as it is the case of microelectronics and biosensor materials, allows the development of diagnosing devices capable of monitoring pathogens and deceases. The design of sensors, signal conditioners and processing units aims to find solutions in which the whole system can be placed directly in the patient or, more desirable, implanted. It becomes a Lab-on-Chip and Point-of-Care device (Colomer-Farrarons, 2009). Since the implanted device becomes part of a biological data acquisition system it must meet few requirements such as reduced size, low power consumption and the possibility of being powered by an RF link, then it operates as a passive RFID tag (Landt, 2005).

The low power restriction is extremely important for the patient safety, by avoiding heating due to the increase of current density in the tissues surrounding the implant that could cause tissue damage. The power restrictions mean also limited power of RF transmitter that can, as well, to induce dangerous electromagnetic fields – EMF.

The focus in this chapter is to discuss the implementation of a Linear Voltage Regulator – LVR by considering the use of a low cost CMOS process, low-power, low silicon area and simple circuit topology.

The LVR is an ASIC structure whose electrical characteristics depend on the specific load conditions. Therefore, the idea is to discuss few structural solutions.

2. Implanted Device - Smart Biological Sensors

A typical CMOS front-end architecture of an in-vivo Biomedical Implanted Device – BID is shown in Figure 1. The system consists, basically, of the sensitive biological element, the transducer or detector element, the associate electronics and signal processors, and the RF link to establish a communication with the manager unit. The combination of the implanted device, the local wireless link and a communication network forms the Wireless Biosensor Network – WBSN (Guennoun, 2008).

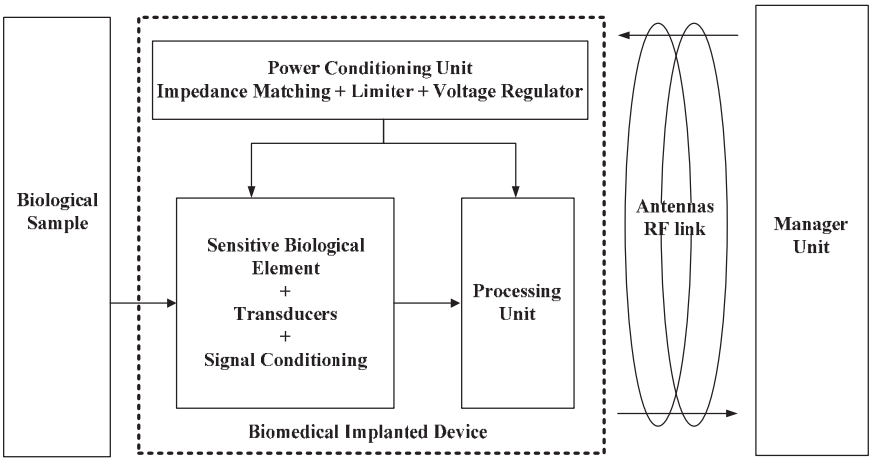

Fig. 1. Typical Implanted Biomedical Device acting as a RFID Tag.

Linear systems based on semiconductor devices demand a stable power supply voltage for proper operation. Fluctuations on the input line voltage, load current fluctuations and temperature variations may cause the circuit to deviate from its optimum operation bias point and even loose its linearity. Therefore, the power supply system must experience minimum impacts on the linearity due to those variations. Nevertheless, the impact of temperature variations in implantable devices is minimized since the body temperature is kept stable at approximately 37^0C (Mackowiak, 1992).

The LVR is part of the power conditioning block that is responsible to supply a stable voltage to the sensors/transducers and its associated electronics.

Unlike the general voltage regulator application, an implantable device does not suffer a large range, but it is more limited. This condition minimizes the impact of load regulation specification.

The tag operation frequency is one of the most important considerations when designing a solution to suit the requirements. The operation frequency has enormous effect on price, performance, range and suitability for RFID projects. The general bands used to broadly classify the RFID tag families are low, high, and ultra high.

The low frequency range (typically between 125 kHz and 134 kHz) is most commonly used for access control, animal tracking and assets tracking. It offers low cost.

The high frequency range (typically 13.56MHz) is used for medium data rate transfer and reading range of up to 1.5 meters, usually for passive tagging. This frequency has also the advantage of not being susceptible to interference from the presence of water or metals. Since the user of an implantable monitoring system is exposed to a RF source near the skin, few safety considerations must be taken into account. The main biohazards and risks due to the RF exposure is mainly the heating from the electromagnetic field distribution on biological tissues (Osepchuk, J.M. & Petersen R. C., 2001). This frequency provides a good tradeoff between power level and human tissue penetration (Sauer, 2005; Vaillantcourt, 1997).
The ultra high band (typically between 850MHz and 950MHz) offers the largest reading ranges, of up to approximately 3 meters for passive tags and 100 meters for active tags. Relatively high reading speeds can be achieved at that band.

3. The topology of a voltage regulator

Classic topologies used in voltage regulators can be classified as linear or switched. Switched regulators present complex circuitry, mainly due to control unit, thus frequently requiring larger power consumption and larger silicon area. Furthermore they provide larger noise at the output due to the switched operation (Rincon-Mora & Allen, 1997).
Low dropout – LDO voltage regulators is one of the most popular power converters used in power management and is more suitable for implanted systems (Rincon-Mora, 1998, 2000). The basic topology of an LDO is presented in Figure 2.

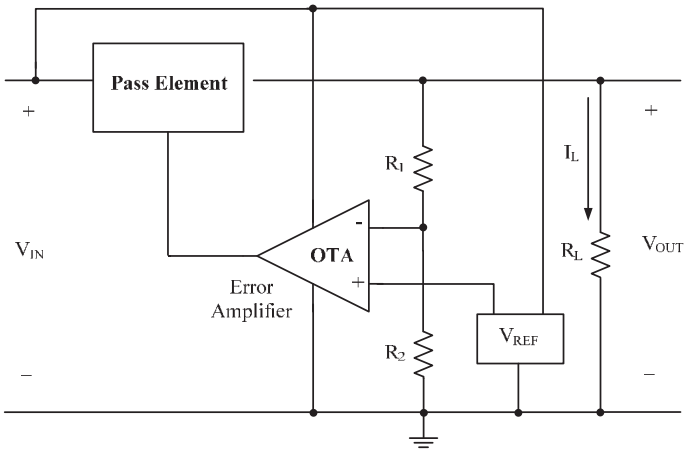

Fig. 2. Basic LDO topology.

The pass element can be implemented using bipolar or MOS transistors. Since a MOS transistor is controlled by its gate voltage, it offers the advantage of smaller power consumption and consequently higher efficiency for the voltage regulator. The MOS transistor can be either N or P type. The NMOS transistor requires a gate voltage higher than the source voltage, and therefore it may be necessary a charge pump to increase the voltage level. The proper choice for low voltage systems, such as implantable devices, it is the use of a PMOS LDO, as indicated in Figure 3 (Kugelstadt, 1999; Simpson, 1997). A

NMOS LDO without charge pump is reported in (Ahmadi & Jullien, 2009) using native transistors (zero threshold) and an internal capacitor to improve the stability, but two external capacitors are required.

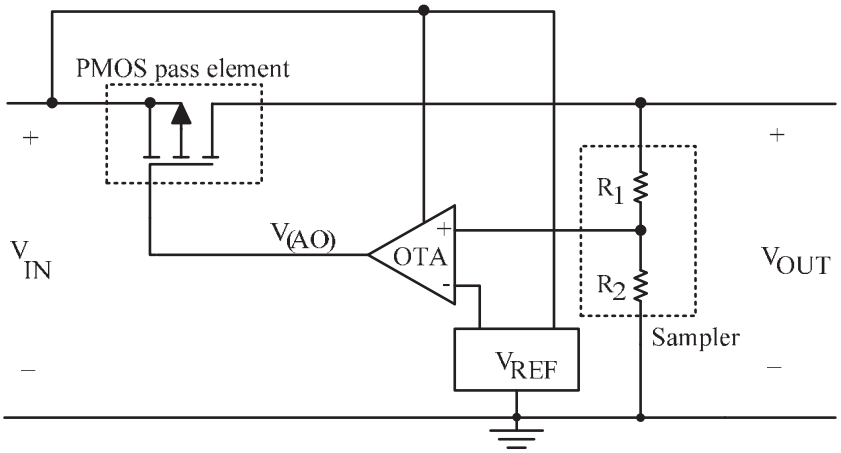

Fig. 3. PMOS based LDO.

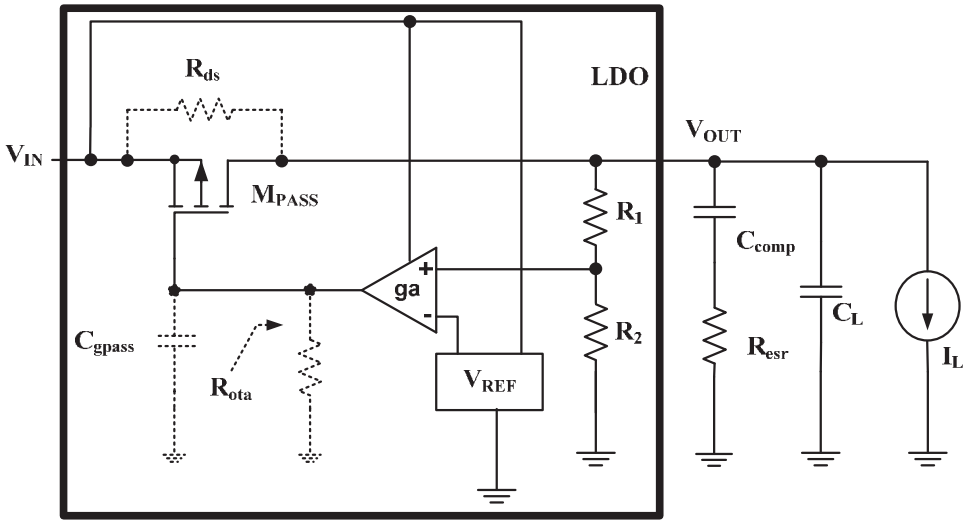

Fig. 4. Classic PMOS LDO with discrete frequency compensation scheme.

The closed loop system output voltage can be found to be:

$$V_{OUT} = \left(1 + \frac{R_1}{R_2}\right) V_{REF} \quad [V] \tag{1}$$

The use of an LDO circuit requires the stability analysis since it forms a closed loop system. The frequency response is degraded by the presence of two poles besides the dominant pole that can lead to an unstable condition. It is necessary to add a zero between these two poles to achieve a frequency compensation. The insertion of this zero is normally implemented by adding a discrete electrolytic capacitor (C_{comp}) at the output node that also contributes with an additional resistance R_{esr}, as represented in Figure 4. Additionally, R_{ota} is the output resistance of the transconductance amplifier, C_{gpass} is the gate capacitance of the PMOS pass transistor and R_{ds} is the channel resistance of the PMOS pass transistor.
The frequencies of these poles and zero are given by (Rogers, 1999):

$$f_{P0} = \frac{-1}{2\pi\left(R_{ds} + R_{esr}\right)C_{comp}} \approx \frac{-1}{2\pi R_{ds} C_{comp}} \quad [\text{Hz}] \tag{2}$$

$$f_{P1} = \frac{-1}{2\pi\left(R_{ds} // R_{esr}\right)C_{L}} \approx \frac{-1}{2\pi R_{esr} C_{L}} \quad [\text{Hz}] \tag{3}$$

$$f_{Z0} = \frac{-1}{2\pi R_{esr} C_{comp}} \quad [\text{Hz}] \tag{4}$$

$$f_{P2} = \frac{-1}{2\pi R_{ota} C_{gpass}} \quad [\text{Hz}] \tag{5}$$

Equation (1) shows that the dominant pole frequency depends on the drain-source resistance, which in turn depends on the drain current. As a consequence, the dominant pole can change its position according to the load. To overcome this situation, the zero must follow the pole. It is common to establish not just a single value for R_{esr} but a range of values as a function of load current.

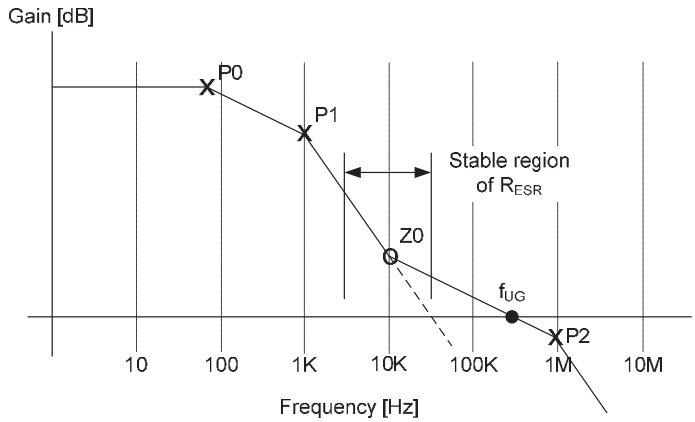

Fig. 5. Frequency response of a PMOS LDO regulator with external compensation capacitor PMOS based LDO.

Figure 5 presents the frequency response of a PMOS LDO. Unfortunately, the use of an external capacitor, such as an electrolytic capacitor, is prohibitive for an implantable device. Thus, the literature provides many contributions to solve the LDO stability problem. Few approaches maintain the external capacitor and modify the internal feedback loop by using buffers (Stanescu, 2003) and Miller compensation capacitor (Huang et al, 2006). Other approaches insert and internal zero, discarding the compensation capacitor, by using controlled sources and even Miller compensation (Huang et al, 2006).

Load Conditions: I_L = 500µA, C_L = 5pF	
V_{IN}	2.2V±10%
V_{OUT}	1V±5%
V_{BIAS}	2V
V_{REF}	200mV*
P_D	1mW**

* A lower value of 200mV was adopted to provide a wider range of output values, as stated by eq. (1)
** A safe value for the RF link power transfer is 10mW/cm² (Lazzi, 2005). The LVR power dissipation should be taken as just 10% of it, corresponding to 1mW, which represents twice as much as required by the load (0.5mW). Reported voltage regulators for implanted devices list a power dissipation range that can be as high as tents of mW (Zheng & Ma, 2010).

Table 1. LVR target values for an implanted blood pressure monitoring system.

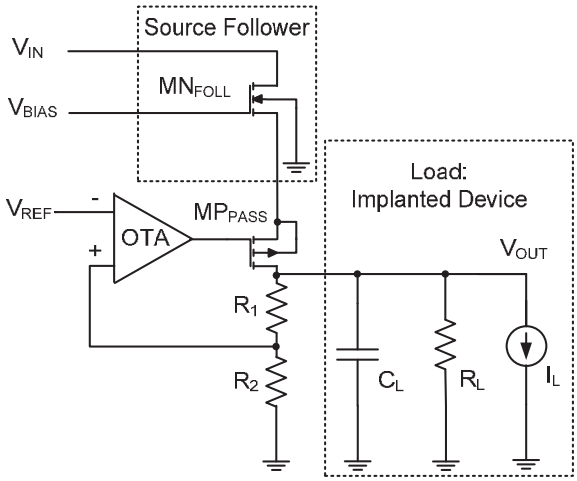

Fig. 6. LVR architecture.

The solution proposed here is the introduction of a source follower (MN_{FOL}) stage in between the input voltage and the LDO block, and the removal of the compensation capacitor C_{comp}, as shown in Figure 6. The source follower maintains the PMOS pass element in the triode region, which leads to an unconditionally stable system, as it will be described later.
The introduction of the extra source follower represents a disadvantage since it introduces extra power consumption and requires additional silicon area. The overall efficiency is also

affected, nevertheless the advantages overpasses de disadvantages, mainly for implanted devices.
Table 1 shows the target values for a project example. The load is an implanted physiological signal system that is used to monitor the blood pressure.

4. Frequency response analysis

The frequency analysis of the LVR can be evaluated by finding initially the open loop gain (Aβ) Figure 7. The originally closed loop is broken at a particular point, and the loop gain is given by:

$$A\beta = -\frac{v_r}{v_x} \quad [-] \tag{6}$$

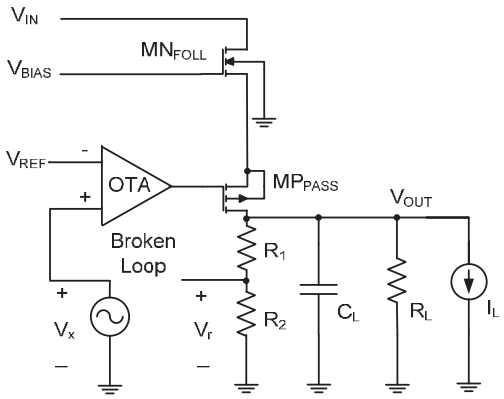

Fig. 7. Feedback broken to analyze the open loop gain.

In Figure 8 the OTA and the pass transistor (MP_{PASS}) are replaced by the small signal model.

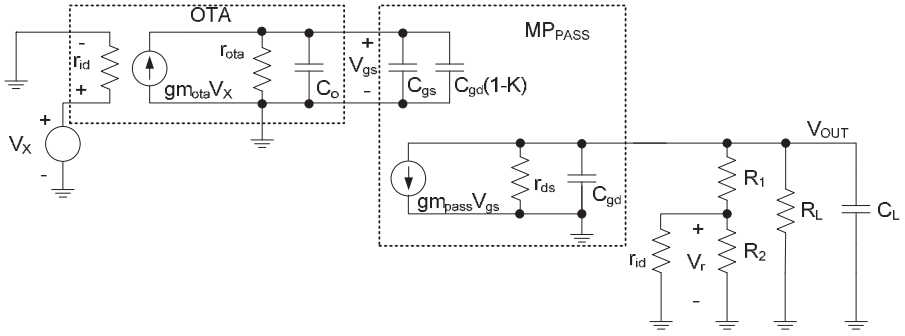

Fig. 8. Small signal equivalent circuit of the LVR

The total load resistance is minimized by the low value of r_{ds}, therefore the drain-gate voltage gain of MP_{PASS} is:

$$K = -\frac{v_{out}}{v_{gs}} = -gm_{pass} r_{ds} \quad [-] \tag{7}$$

The output voltage is:

$$v_{out} = -\frac{gm_{pass} r_{ds}}{\left(1+\frac{S}{p_1}\right)} \frac{gm_{ota} r_{ota}}{\left(1+\frac{S}{p_2}\right)} v_x \quad [V] \tag{8}$$

Considering that r_{id} is much larger than R_2, then v_r is:

$$v_r = v_{out} \frac{R_2}{R_1 + R_2} \quad [V] \tag{9}$$

By combing (7) and (8), the loop gain is:

$$A\beta = \frac{gm_{pass} r_{ds}}{\left(1+\frac{S}{p_1}\right)} \frac{gm_{ota} r_{ota}}{\left(1+\frac{S}{p_2}\right)} \frac{R_2}{R_1 + R_2} \quad [V] \tag{10}$$

It can be observed from Equation (9) that the feedback gain β is $R_2/(R_1+R_2)$. It is compatible with Equation (1) that states the relationship between V_{OUT} and V_{IN} is given by the factor $1/\beta$.

The poles p_1 and p_2 are:

$$f_{P1} = \frac{-1}{2\pi\left(C_{gd} + C_L\right) r_{ds}} \quad [Hz]$$

$$f_{P2} = \frac{-1}{2\pi\left[C_o + C_{gs} + C_{gd}\left(1 + gm_{pass} r_{ds}\right)\right] r_{ota}} \quad [Hz] \tag{11}$$

Pole p_2 is the dominant one since r_{ota} is in the range of MΩ and can be at least 10^5 times larger than r_{ds}, which is the range of tens of Ohms. So the frequency stability of the regulator is a function of the OTA design, the geometric aspect ratio of MP_{PASS} and the load. As an ASIC application, the load current (I_L), resistance (R_L) and capacitance (C_L) can be stated as constants without impacting in the pole frequencies. The OTA output capacitance C_O can be neglected since the PMOS pass transistor has a larger geometric aspect and, consequently, larger C_{gs} and C_{gd}.

Equation (9) shows that at low frequencies (DC), the gain A is given by:

$$A = gm_{pass} r_{ds} gm_{ota} r_{ota} \quad [-] \tag{12}$$

Considering typically g_m in the range of 10^{-3} [V/A], tens of Ohm to r_{ds} and 10^6 Ohm for r_{ota}, than the gain is greater than 40 [dB]. The dominant pole will have a frequency in the range of tens of H_z and the unit frequency gain in the range of hundreds of KH_Z.

5. The sampler circuit

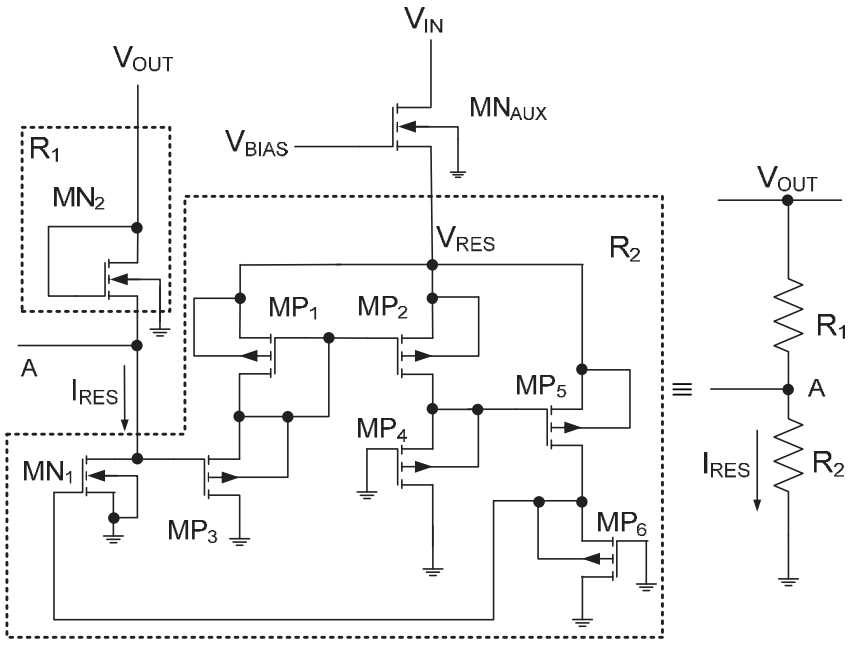

Fig. 9. Sampler Circuit for the LVR.

Figure 9 presents the sampler circuit. In order to implement the whole circuit in a single CMOS chip, R_1 is realized as a MOS diode (transistor MN_2) and R_2 is implemented through an interesting topology, a grounded MOS resistor (Dejhan, 2004). The use of the source follower transistor MN_{AUX} guarantees that the grounded MOS resistor is isolated from V_{IN}, thus avoiding a significant transference of ripple voltage to the output voltage. MN_{AUX} also imposes a smaller effective voltage to the MOS resistor, thus reducing the sampler current.
The power supply voltage of the sampling circuit (PMOS array) is reduced by approximately 1V, thus settling V_{RES} to 1.2V. This is important to reduce the ground current and to maximize the LVR efficiency and improving the overall power dissipation. The relationship R_1/R_2 is optimized by the adjustments of the aspect ratio of transistor MN_1 and MN_2.
The sampler circuit current I_{RES} is designed to be ≈1% of the maximum current load (≈ 5μA). The voltage at point A is virtually V_{REF}, due to the OTA virtual short circuit. Therefore, the R_1 equivalent resistance is given as:

$$R_2 = \frac{200\text{mV}}{5\mu\text{A}} = 40 \quad [\text{K}\Omega] \tag{13}$$

The aspect ratio of MN_1 was adjusted in order to set I_{RES} as close as to the target value of 5μA. So, R_1 (transistor MN_2) will be adjusted as a 160KΩ resistor.
The additional capacitances introduced by the grounded MOS resistor and MN_2 are smaller enough so that can be discarded in the previous frequency response analyses. All those transistors have small source and drain areas leading to capacitances in the range of fF. The eventual poles will be far away from the dominant one and the unit frequency gain.

6. The voltage references

On designing any system that requires a voltage reference, the temperature and power supply sensitivity must be taken into account.
Classical voltage references are based on the bandgap voltages, where two distinct voltages with opposite thermal coefficients (PTAT and CTAT) are summed to obtain an overall near zero coefficient. Besides, their bias circuits must be robust to guarantee a low sensitivity to the power line fluctuations. The bandgap voltage is about 1.12V for silicon at room temperature (Tzanateas, 1979).
Nevertheless, the evolution of fabrication process is pushing down the supply voltages. For instance, it is about 1.2V for a CMOS 0.13μm process. So there is a demand for new voltage references topologies to produce values bellow the classical bandgap value of 1.2V.
A literature revision shows the trends into this challenge (Koushaeian & Skafidas, 2010). However, these contributions show one or more of these aspect: complex circuits topologies with an elevated number of components, the need of special components that are not ready available from the CMOS common process, the need of trimming procedures, use of external components and use of MOS transistors that are not operating in classical modes. An alternative mode is the weak inversion in which the MOS transistor behavior approaches the bipolar ones.

6.1 Current mirror core

The core to produce the voltages references are the self biased current mirror illustrated in Figure 9. The use of a parasitic vertical PNP bipolar transistor Q_1 in a CMOS digital technology is justified since it presents known V_{BE} voltage and temperature behavior. The temperature does not represent the main impact factor since the whole system will be implanted.
Equations (12) and (13) are the starting point to establish the values of the currents I_E and I_D. The currents values are set to approximately 5μA (1% of maximum load current) in order to improve the LVR overall efficiency.

$$I_d = \frac{KP}{2(1+\delta)}\left(\frac{W}{L}\right)\left(V_{gs} - \left|V_{th0}\right|\right)^2 = \beta\left(V_{gs} - \left|V_{th0}\right|\right)^2 \quad [A] \tag{14}$$

$$I_e = I_{cs}\exp\left(\frac{V_{be}}{U_T} - 1\right) \quad [A] \tag{15}$$

where KP is the MOS transconductance given in [μA²/V], δ is a dimensionless fitting parameter for short channel devices, (W/L) is the geometric aspect ratio, V_{th0} is MOS the threshold voltage given in [V], I_{CS} is the bipolar saturation current given in [nA] and U_T the thermal voltage that is about 26.7 [mV] at 37°C.

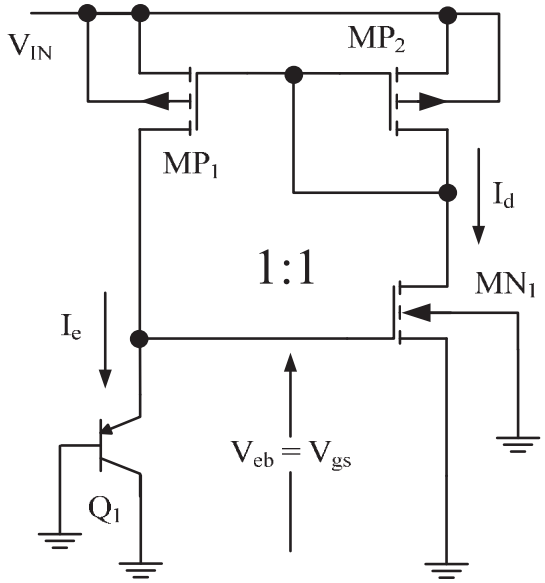

Fig. 10. Self biased current mirror.

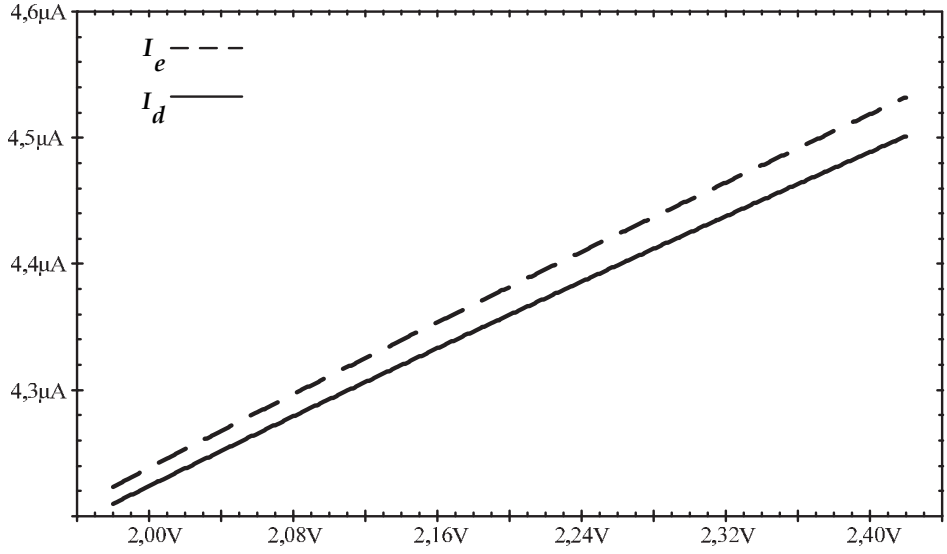

Fig. 11. Simulated results for the mirror currents @ T=37º.

There is no closed solution for both equations and it is necessary to develop an interactive simulation process to reach the optimum result for I_d, which is equal to I_e. The target value for these simulation is the geometric aspect ratio of the MOS transistors, since it is used a vertical PNP bipolar with a 100µm² emitter area. To minimize the short channel effects, the

channel length was fixed to 1μm for MN_1 and 2μm for MP_1 and MP_2 to improve the mirroring matching. The PMOS geometric aspects are also optimized by simulation.
Figure 11 shows the simulated currents for an input voltage variation of ±10% around to the ideal value of 2.2V. The temperature was fixed in 37ºC.
The relative error between the mirror currents, at the ideal operating point of V_{IN}=2.2V, can be calculated as:

$$E_{rr}(\%) = \frac{I_{eQ} - I_{dQ}}{I_{eQ}} 100 = \frac{4,38.10^{-6} - 4,36.10^{-6}}{4,38.10^{-6}} 100 \approx 0,45 \quad [\%] \tag{16}$$

It is important to evaluate the power supply dependence of those currents. The sensitivity is an adequate parameter to measure it and is given by (Gray & Meyer, 1993):

$$S_{V_{IN}}^{I_d} = \frac{V_{IN}}{I_d}\bigg|_Q \frac{\partial I_d}{\partial V_{IN}}\bigg|_Q \quad [-] \tag{17}$$

The derivative term can be found directly from the circuit topology to be:

$$\frac{\partial I_d}{\partial V_{IN}} = \frac{I_{dQ}\lambda_n}{1 - \frac{2U_T}{\left(V_{eb} - V_{th0(N)}\right)}} \tag{18}$$

where λ_n is the channel length modulation coefficient that is obtained by simulation and $V_{th0(N)}$ is the NMOS threshold voltage. Substituting (17) in (16) leads to:

$$S_{V_{IN}}^{I_d} = \frac{\lambda_n V_{INQ}}{\left(1 - \frac{2U_T}{V_{eb} - V_{th0(N)}}\right)} \quad [-] \tag{19}$$

An alternative way to evaluate the current sensitivity is by using Figure 11. The following equation offers a derivative approximation. It considers the variation of I_d due to variations on V_{IN}:

$$S_{V_{IN}}^{I_d} \approx \frac{V_{INQ}}{I_{dQ}} \frac{\Delta I_d}{\Delta V_{IN}} \quad [-] \tag{20}$$

Table 2 resumes the calculated and simulated results for the current sensitivity.
Consequently, for ±10% variation in V_{IN} around the quiescent value, the mirror currents will change approximately ±3%. Simulations results also point out that for the voltage references circuits discussed next, than V_{eb} voltage will play an important rule and suffers a 1.8 [mV] variation for the entire V_{IN} range, representing a deviation of ±0.13% from the 676 [mV] quiescent value. It indicates a power line rejection rate – PSRR better than 45 [dB] at low frequencies.

Body Temperature: 37°C	
Calculated	Simulated
V_{INQ}=2.2 [V]	V_{INQ}=2.2 [V]
I_{dQ}=5 [μA]	I_{dQ}=4.4 [μA]
-	λ_n=0.096 [V^{-1}]
V_{eb}=680 [mV]	V_{eb}=676 [mV]
-	$V_{th0(N)}$=523 [mV]*
$S_{V_{IN}}^{I_d}$ Eq. (19) = 0.316	$S_{V_{IN}}^{I_d}$ Eq. (20) = 0.331

* The threshold voltage value was indicated by a CMOS process.

Table 2. Id sensitivity: calculated and simulated values

6.2 The start up circuit

As a self biased circuit, the current mirror core needs a start up circuit to ensure the correct operating point. It is implemented by the circuit shown in Figure 12.

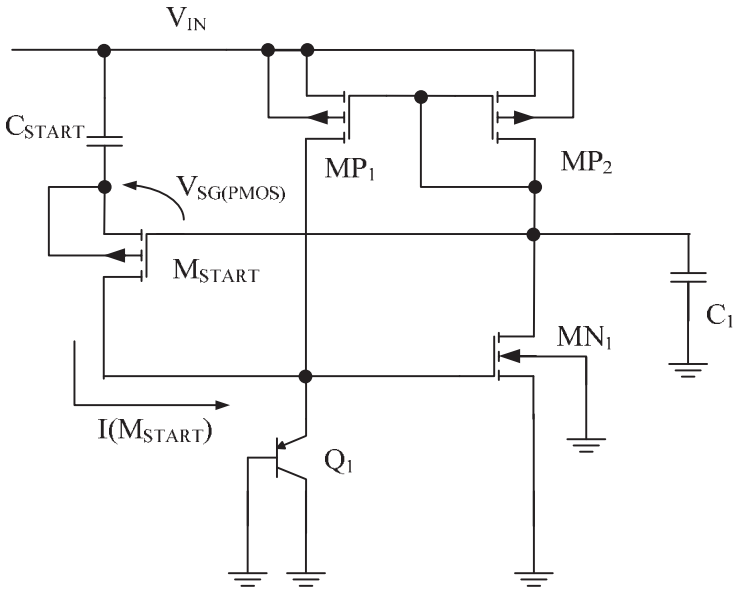

Fig. 12. The start up circuit added into the self biased current mirror.

C_{START} and C_1 are small capacitors (0.5pF) and M_{START} is a PMOS transistor, similar to those used in the current mirror. When the circuit is energized, assuming that the capacitors are discharged, the V_{sg} of M_{START} is greater than its threshold voltage. This will cause a transitory current to flow into Q_1 leading the system to desired operating point. At same time, C_{START} is charged toward V_{IN} reducing the V_{sg} of M_{START} and, consequently, turning it off. Figure 13 shows a simulating that validates the described action. The transitory current spends only 20 [ns] that is very low for a biomedical application.

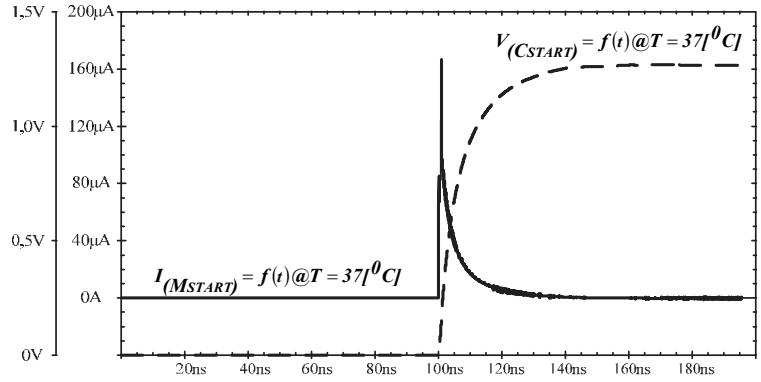

Fig. 13. The Start Up transient current.

6.3 V_{REF} voltage reference

The topology presented in Figure 14 is used to generate the V_{REF} voltage reference. The target value for this reference is 200 [mV] as discussed previously. The current I_d is mirrored to the composite transistor (Ferreira & Pimenta, 2006) formed by MN_{REF1} and MN_{REF2}. The gate bias comes from Q_1 collector and represents only a capacitive charge for the current mirror core since the gate currents are virtually zero. This capacitive effect contributes to improve the V_{eb} PSRR.

It is important to observe that the composite transistor exhibits different modes of operation for each transistor. MN_{REF2} has a nominal V_{gs2} voltage of 676 [mV] leading to strong inversion operation since $V_{th0(N)}$ is approximately 523 [mV]. However, voltage V_{gs1} of transistor MN_{REF1} is subtracted by 200 [mV] (the target output voltage). Thus, the effective value of V_{gs1} is 476 [mV], leading it to operate in weak inversion.

The adopted geometric aspect of MN_{REF2} is similar to current mirror transistor MN_1, W=2µm and L=1µm. It is necessary to evaluate the ideal geometric aspect of MN_{REF1} to guarantee the reference voltage of 200 [mV].

By equating the drain current of both NMOS transistors of the composite topology, then:

$$I_X\left(\frac{W}{L}\right)_{MN_{REF1}} \exp\left[\frac{V_{eb} - V_{REF} - V_{th(N)}}{nU_T}\right] = \beta_n\left(V_{eb} - V_{th0(N)}\right)^2\left(1 + \lambda_n V_{REF}\right) \quad (21)$$

where I_X is the weak inversion characteristic current and n the weak inversion coefficient. In the strong inversion, the term $(1+\lambda_n V_{REF})$ can be approximate to unity. Note that the M_{NREF1} threshold voltage is presented as $V_{th(N)}$ since it suffers from body effect.

Solving the equality for V_{REF}:

$$V_{REF} = V_{eb} - V_{th(N)} - nU_T \ln\left[\frac{\beta_n\left(V_{eb} - V_{th0(N)}\right)^2}{I_X\left(\frac{W}{L}\right)_1}\right] \quad [V] \quad (22)$$

Equation (22) shows that V_{REF} can be adjusted by the geometric aspect of MN_{REF2} considering that all other parameters are assumed constant under the corporal temperature. Using interactive simulation, with V_{IN}=2.2V, the optimized geometric aspect ratio is 173. To improve the reference PSRR, the channel length of this transistor is doubled to 2 [μm].

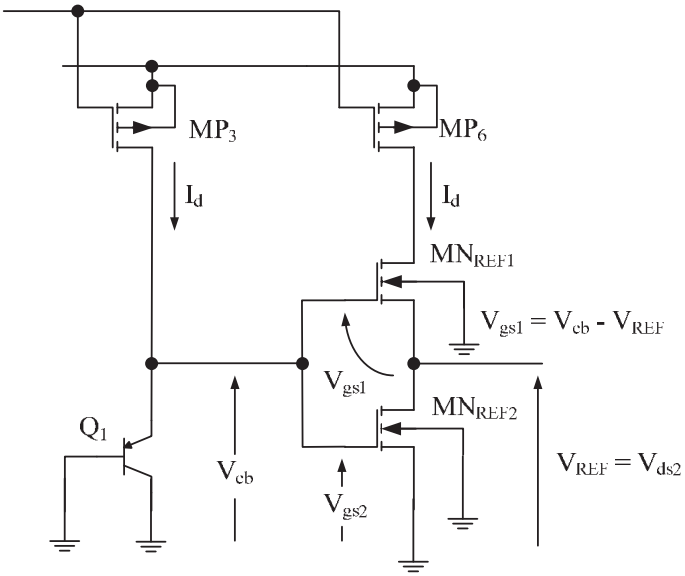

Fig. 14. The topology used to generate de voltage reference V_{REF}

6.4 V_{REF} sensitivity

Using a similar concept discussed in section 4.1, the V_{REF} sensitivity, related to the input voltage V_{IN}, can be expressed as:

$$S_{V_{IN}}^{V_{REF}} = \frac{V_{IN}}{V_{REF}}\bigg|_{Q} \frac{\partial V_{REF}}{\partial V_{IN}}\bigg|_{Q} \quad [-] \tag{23}$$

The derivate term can be evaluated directly from the circuit topology as:

$$\frac{\partial V_{REF}}{\partial V_{IN}} = \frac{U_T \lambda_n}{1 - \frac{2U_T}{\left(V_{eb} - V_{th0(N)}\right)}} \quad [-] \tag{24}$$

Combining equation (23) and (24) and using the known values, the V_{REF} sensitivity is 0.0415. Thus, for a ±10% variation in the input voltage V_{IN}, V_{REF} suffers just ±0.415%. Figure 15 shows the simulation result of those variations. As can be observed, the nominal values for V_{REF} and V_{IN} are, respectively, 200 [mV] and 2.2 [V]. Using this simulation to evaluate the sensitivity, results in:

$$S_{V_{IN}}^{V_{REF}} = \frac{2,2}{200.10^{-3}} \frac{\Delta V_{REF}}{\Delta V_{IN}} = 11 \frac{1,6.10^{-3}}{440.10^{-3}} \approx 0.04 \quad [-] \tag{25}$$

Those results lead to a PSRR better than 40 [dB] at low frequencies.

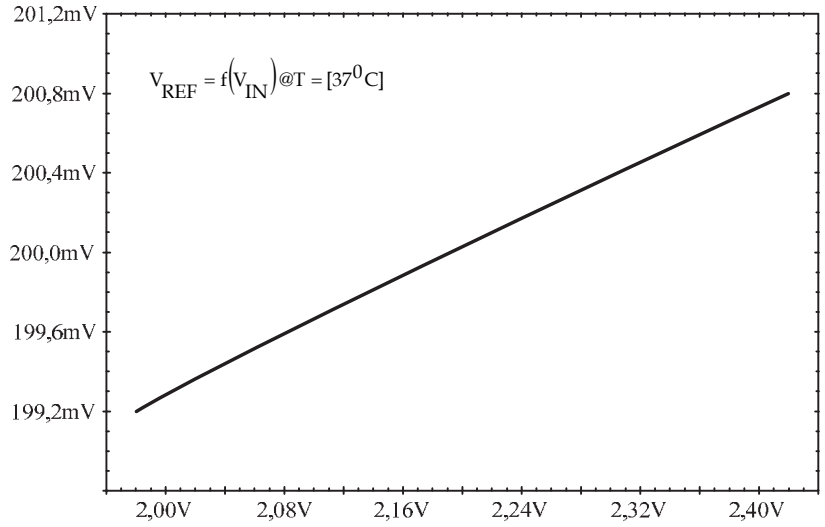

Fig. 15. Simulation of V_{REF} variations due to V_{IN}

6.5 V_{BIAS} voltage reference

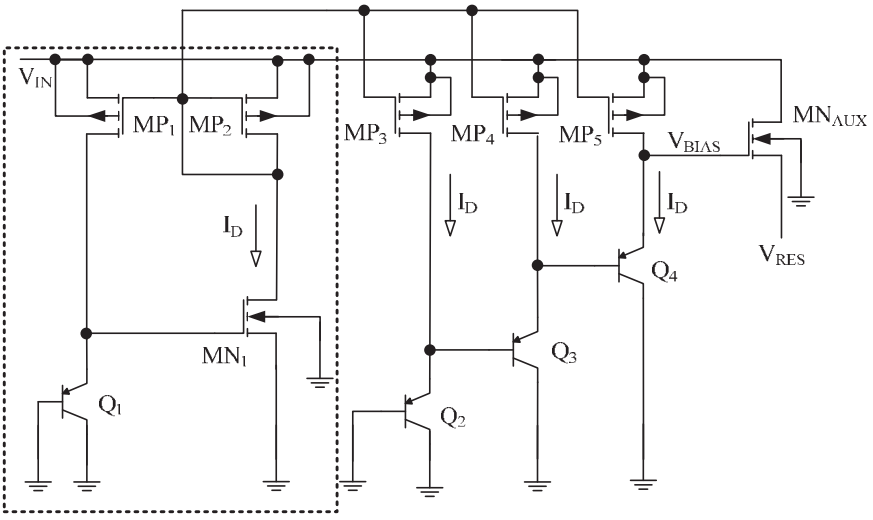

Fig. 16. Three stacked bipolar transistors used to generate V_{BIAS} voltage reference.

The circuit used to generate the V_{BIAS} is illustrated in Figure 16. The use of three stacked bipolar transistors generate a voltage of ≈ 2 [V], i. e. 3 times the quiescent value of V_{eb} (676 [mV]). The bias currents for Q_2, Q_3 and Q_4 are mirrored from the current mirror core with unity gain.

6.6 V_{BIAS} sensitivity

The V_{BIAS} sensitivity can be derived from the circuit topology. It is interesting to evaluate, at first, the V_{eb} for Q_1 transistor. The final result for V_{BIAS} will be three times larger. These formulations are:

$$S_{V_{IN}}^{V_{BIAS}} = \frac{V_{IN}}{V_{BIAS}}\bigg|_{Q} \frac{\partial V_{BIAS}}{\partial V_{IN}}\bigg|_{Q} \quad [-] \tag{26}$$

$$S_{V_{IN}}^{V_{BIAS}} = \frac{V_{IN}}{V_{BIAS}} \frac{3U_T\lambda_n}{1-\frac{2U_T}{V_{eb}-V_{th0(N)}}} \quad [-] \tag{27}$$

For the know values, the V_{BIAS} sensitivity is calculated as ≈0.012, leading to a variation of ±1.2% for a variation of ±10% at the input voltage line V_{IN}.

6.7 PMOS pass transistor and NMOS follower geometric aspect ratios

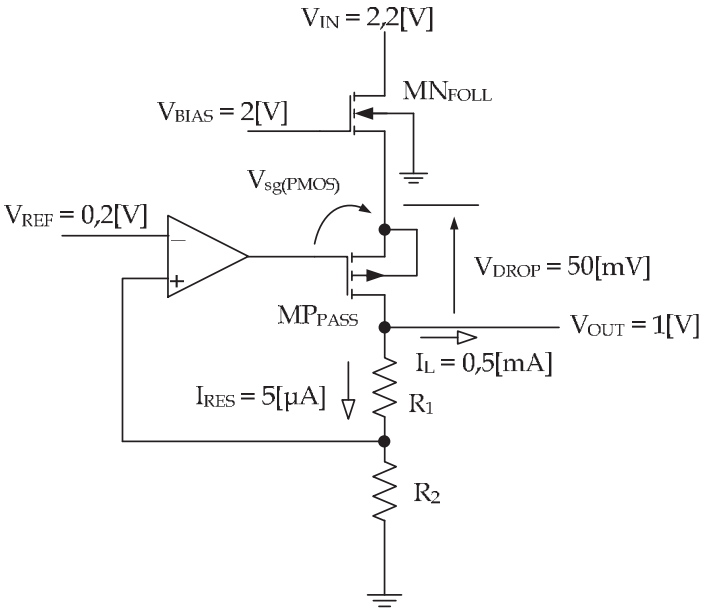

Fig. 17. Circuit used to optimize the MN_{FOLL} geometric aspect ratio.

Figure 17 shows the main current and voltages values used to estimate MP_{PASS} and MN_{FOLL} geometric aspects.
For MP_{PASS} transistor, two considerations are important. First, its geometric aspect must be larger enough to support the total nominal load current plus the sampler current. Second, its operation must be kept in the triode region to guarantee a low r_{ds} value. In the triode region, the resistance is given as:

$$R_{ds}(MP_{PASS}) = \frac{1}{\frac{KP}{2(1+\delta)}\left(\frac{W}{L}\right)\left(V_{sg} - V_{th0(P)} - V_{sd}\right)} \quad [\Omega] \tag{28}$$

The aspect ratio (W/L) design parameter should be raised to lower the drain-source resistance. Figure 17 also shows a suggested 50 [mV] (V_{DROP}) in order to keep the low dropout concept in the LDO circuitry. The V_{ROP} voltage corresponds to V_{sd} voltage in Equation (28).
By replacing MN_{FOLL} transistor by a 5.05 [µA] current source, interactive simulations lead to a MP_{PASS} geometric aspect of 2500/1. In order to evaluate the aspect ratio of MN_{FOLL} it must be noticed first that MN_{FOLL} suffers from body effect and its threshold voltage is corrected by using:

$$\begin{aligned} V_{th(N)} &= V_{th0(N)} + \gamma\left(\sqrt{2\varphi_F + |V_{bs}|} - \sqrt{2\varphi_F}\right) \\ V_{th(N)} &= 0,523 + 0,4\left(\sqrt{0,6+1,05} - \sqrt{0,6}\right) \approx 727 \quad [\text{mV}] \end{aligned} \tag{29}$$

By using this result in the drain current equation, the MN_{FOLL} geometric aspect is given as:

$$\begin{aligned} I_d &= \beta_n\left(V_{gs} - V_{th(N)}\right)^2 \\ 0,505.10^{-3} &= 95,3.10^{-6}\left(\frac{W}{L}\right)\left[(2-1,05) - 0,727\right]^2 \Rightarrow \left(\frac{W}{L}\right) \approx 106 \end{aligned} \tag{30}$$

6.8 PMOS pass transistor and NMOS follower capacitances

Those two transistors (MN_{FOLL} and MP_{PASS}) have a large geometric aspect ratio leading to relative large gate capacitances. The PMOS pass transistor gate capacitance is important since it is responsible to determine the OTA dominant pole.
The NMOS and PMOS S_iO_2 thickness (T_{OX}) can be used to obtain the gate capacitances per unit area as:

$$\begin{aligned} COX_{NMOS} &= \frac{\varepsilon_{OX}}{T_{OX}} = \frac{3,45.10^{-13}}{7,5.10^{-9}}\frac{1}{10^6.10^4} \approx 4,6.10^{-15} \quad \left[\frac{F}{\mu m^2}\right] \\ COX_{PMOS} &= \frac{\varepsilon_{OX}}{T_{OX}} = \frac{3,45.10^{-13}}{7,7.10^{-9}}\frac{1}{10^6.10^4} \approx 4,48.10^{-15} \quad \left[\frac{F}{\mu m^2}\right] \end{aligned} \tag{31}$$

As the PMOS pass transistor operates in the triode region, the gate to source and gate to drain capacitances are:

$$C_{gs} = C_{gd} = \frac{1}{2}(WL)_{PMOS} C_{OX} \approx 5{,}75.10^{-12} \quad [F] \tag{32}$$

7. The Operational Transconductance Amplifier (OTA)

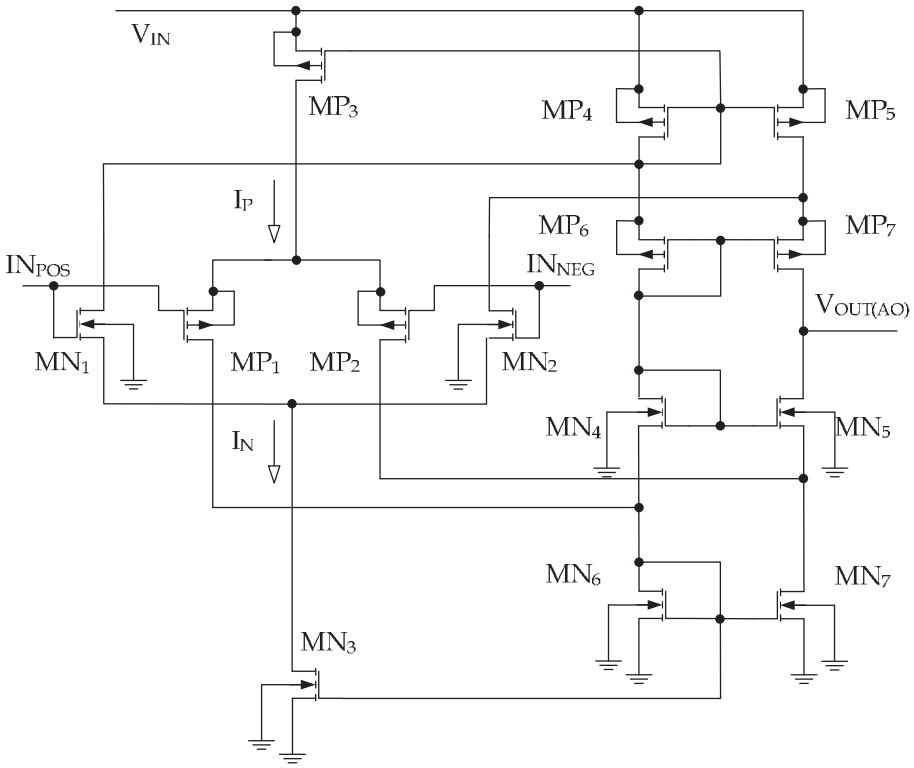

Fig. 18. Operational Transconductance Amplifier (OTA).

There are some features that must be taken into account in order to design the OTA:

1. To validate the closed loop properties, the OTA must have an open loop gain larger than 1000 (60 [dB]);
2. Since the OTA is powered by the input voltage V_{IN}, it must exhibit a good power supply rejection ratio. A target value of 40 [db] is used as a reference;
3. The OTA must have a low offset voltage. The offset voltage has a direct impact in equation (1) and can deviate from the nominal output voltage. A target value of 5 [mV] was adopted. It is very important to observe the matching on the OTA stage to minimize the systematic offset and the use of layout technique to minimize the random offset;

4. The total quiescent bias current must be kept as low as possible to improve the OTA overall efficiency. A target value of 3 [μA] was adopted, representing less than 1% of load current. As the OTA has three currents branches, it is assigned a current of 1 [μA] to each one;
5. The dominant pole discussed in the previous sections is a function of the OTA output resistance;
6. The OTA frequency response must lead to a stable system over the entire band. A margin phase of 70° degrees is a target value.
7. The OTA does not need fast responses due the physiological application. The slew rate and settling time targets are, respectively, 0.1 [V/μs] and 10 [μs].

One recommended topology is the folded cascade. It offers high output resistance and, as in this particular case, the dominant pole is fixed by the capacitive load. This is important to reduce the silicon area and extra power consumption by using additional compensation circuits.

It is used the self biased Operational Transconductance Amplifier – OTA topology (Mandal & Visvanathan, 1997). It provides additional reduction of silicon area and power consumption by using other biasing circuits. The OTA circuit is depicted in Figure 18.

As can be observed, the OTA has a rail-to-rail input stage. It is not absolutely necessary in this project, but it is interesting to have the possibility to generating output voltages near the rail lines V_{IN} and Ground. The OTA can be suitable for other applications that require different input voltage values.

The OTA open loop gain is:

$$AV_{OL} = gm_{ota} r_{ota} = \left(gm_P + gm_N\right) r_{ota} \quad [-] \tag{33}$$

where gm_N and gm_P are the NMOS and PMOS input differential pair transconductance, respectively. In the case of general purpose application, it should be used an additional circuitry to compensate their transconductances since they exhibits different values depending on the region of operation.

In this project, the gm variations, that can be as large as 100%, do not have a significant impact on the LVR stability. The dominant pole is far away enough from the other poles by several orders of magnitude.

7.1 OTA transistors geometric aspect

Figure 19 shows the lower half cascode from Figure 18 and the quiescent output voltage of 1.1 [V].

That voltage is considered split equally between the two NMOS transistor pairs. Observe that it is necessary to consider the total NMOS tail current I_N for $MN_{6,7}$. Using Equation 14:

$$\begin{aligned} 1.10^{-6} &\approx 95,3.10^{-6}\left(\frac{W}{L}\right)_{MN6,7}\left(0,55-0,523\right)^2 \\ \left(\frac{W}{L}\right)_{MN6,7} &\approx 14 \end{aligned} \tag{34}$$

Figure 20 shows the PMOS and NMOS differential voltage considerations.

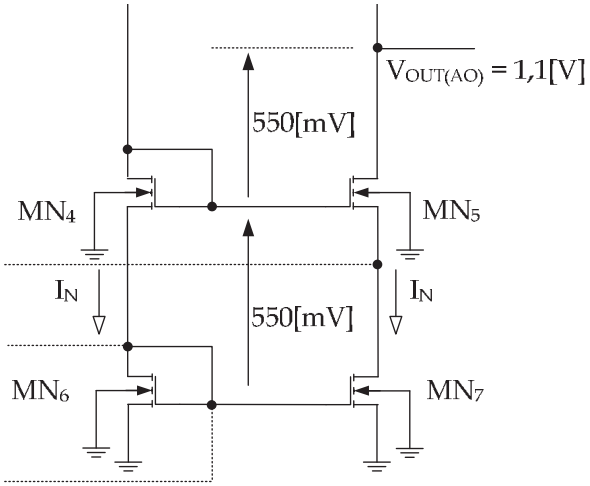

Fig. 19. Lower half used to evaluate the geometric aspect ratios.

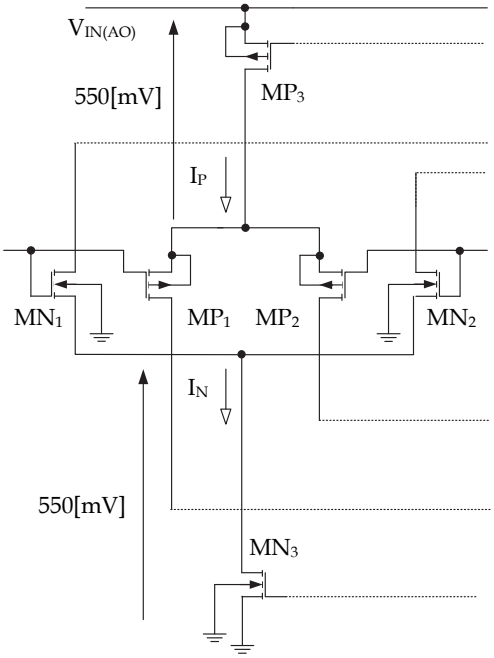

Fig. 20. NMOS and PMOS differential input pairs.

For transistors $MN_{1,2}$ it is necessary to consider the threshold voltage correction since they suffer from body effect and operate in weak inversion.

$$V_{th(N)} = 0,523 + 0,4\left[\sqrt{0,6+0,55} - \sqrt{0,6}\right] \approx 642 \quad [mV] \tag{35}$$

Therefore, by using the current formulation, then:

$$\begin{gathered} I_d = I_X\left(\frac{W}{L}\right)\exp\left(\frac{V_{gs} - V_{th(N)}}{nU_T}\right) \quad [A] \\ 1.10^{-6} \approx 103,1.10^{-9}\left(\frac{W}{L}\right)\exp\left(\frac{0,55-0,642}{45.10^{-3}}\right) \Rightarrow \left(\frac{W}{L}\right) \approx 74 \end{gathered} \tag{36}$$

NMOS transistors $MN_{4,5}$ operate similarly to $MN_{1,2}$. The only difference is they carry half of tail current. Thus, the geometric aspect of these transistors is divided by 2 (37). All PMOS transistors have their geometric aspect ratios adjusted by interactive simulations. Table 3 resumes OTA aspect ratios where the channel length and width are expressed in [µm].

Corporal Temperature: 37ºC	
$(W/L)_{MN1} = (W/L)_{MN2}$	74/1
$(W/L)_{MP1} = (W/L)_{MP2}$	158/1
$(W/L)_{MN3} = (W/L)_{MN6} = (W/L)_{MN7}$	14/1
$(W/L)_{MN4} = (W/L)_{MN5}$	32/1
$(W/L)_{MP3} = (W/L)_{MP4} = (W/L)_{MP5}$	158/1
$(W/L)_{MP6} = (W/L)_{MP7}$	272/1

Table 3. OTA geometric aspect ratios, in [µm]

7.2 OTA simulations results

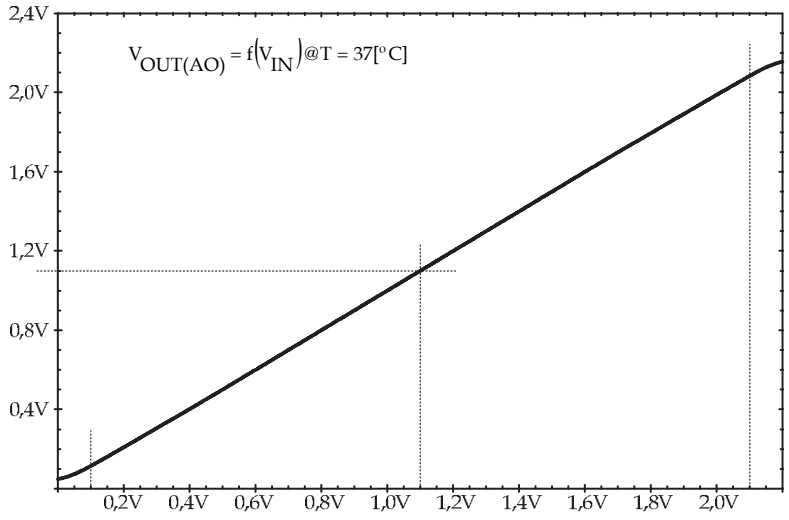

Fig. 21. OTA common mode range indicating a rail-to rail operation.

The following figures show the most relevant OTA parameters simulations. The common mode range – CMR is depicted in Figure 21. The OTA is buffer connected and the input signal is linear over the entire range, thus characterizing a rail-to-rail operation. The OTA analog ground is 1.1 [V] and the simulation shows that the systematic offset is minimum, thus representing a good matching between the OTA stages.
Figure 22 shows a configuration to analyze the OTA frequency response. The auxiliary capacitor and inductor (C_{AUX}, L_{aux}) guarantees a closed loop for DC signal and an open loop for AC signal. Thus the OTA will be properly biased since the DC path configures a buffer connection.

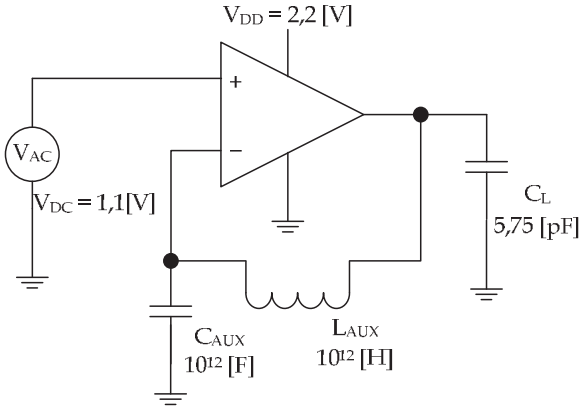

Fig. 21. Buffer configuration used to simulate the OTA frequency response.

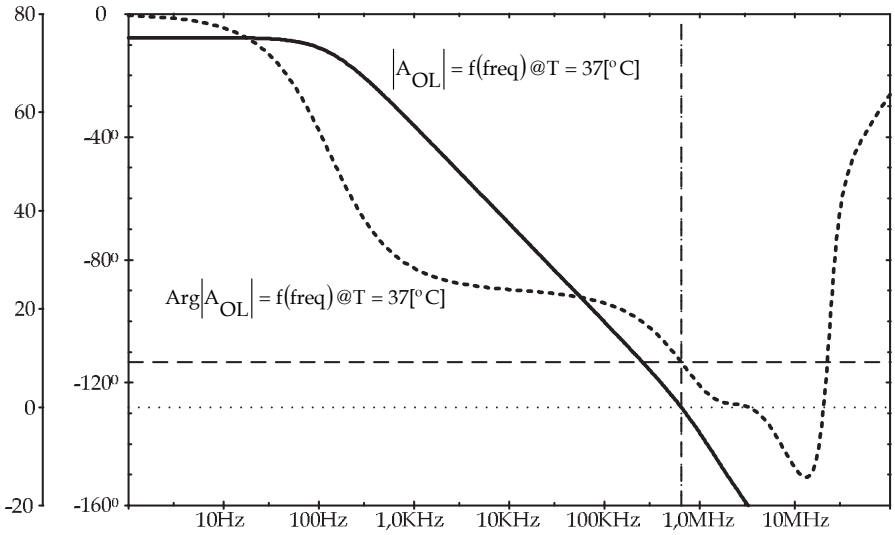

Fig. 22. OTA Frequency response.

The load capacitance C_L is represented by the PMOS pass transistor gate capacitance, evaluated according to Equation (32). The dominant pole (P_2) is located at ≈130 [H_Z] and the unit frequency gain (f_U) is located at ≈640 [KH_Z]. The phase margin (Φ_F) is ≈66°. Figure 22 show these results.
On a buffer configuration, the OTA is excited by a square wave to obtain the transient parameters. Figure 23 shows the resultant simulation considering a fluctuation of approximately ±10% around the 1.1 [V] analog ground. That simulation can be used to obtain the falling and raising slew rates (SR) and the settling time.

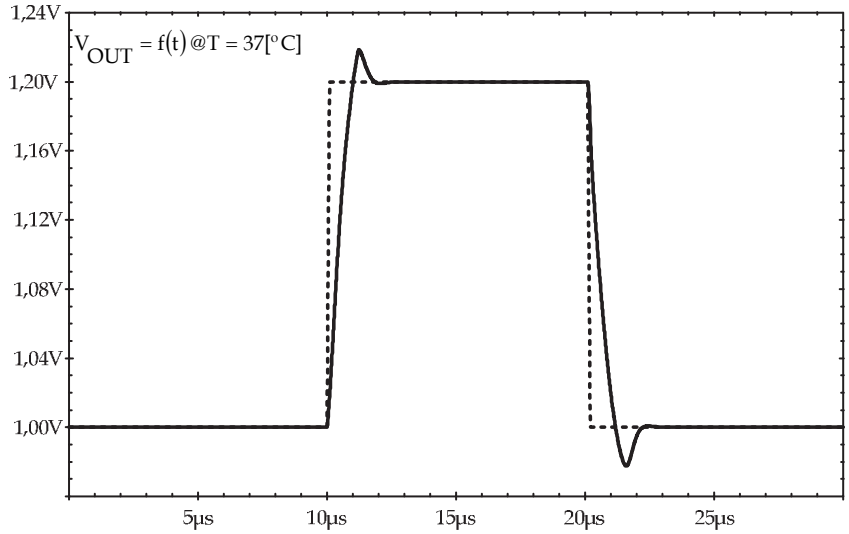

Fig. 23. OTA transient response.

Table 4 resumes the main parameters obtained from the interactive simulations.

Corporal Temperature: 37ºC Input Voltage Supply: 2.2 [V]	
I_{DD} [µA]	3,5
P_D @ I_{DD} [µW]	7,7
CMR	V_{SS}+100 [mV] V_{DD} – 100 [mV]
OTA dominant pole [H_Z]	130
f_{UG} [MH_z]	0,64
Φ_M [º]	66,6
T_{SET} @ 0,1% [µS] raise and fall	3
SR^+ e SR^- [V/µS]	0,2
PSRR @ 100H_Z [dB]	-81
PSRR @ 10MH_Z [dB]	-26,5

Table 4. OTA main parameters.

8. Layout considerations

Even by using the most advanced microfabrication techniques, it is not possible to guarantee that all the devices implemented in the same chip will have the same electrical characteristics. The aspect ratio of two similar devices can be controlled to a precision of approximately ±1% and, in the many cases, it can be better than ±0.1%. Therefore, the layout project of an integrated circuit, mainly analog application fields, must take mismatches into account (Shyu, 1984).

The layout, as a backend step, plays an important rule to fabricate matched devices in the integrated circuit. It is not possible to cancel the mismatch completely; nevertheless there are ways to minimize it.

The objective of component matching is to reduce the error introduced by the deviations in the fabrication process; therefore it is necessary to use layout techniques.

The mismatch can be classified as systematic and random (Ramos, 2007). The main sources of systematic mismatch are the process polarization (difference between the designed dimensions and actual dimensions), contact resistances, non-uniform current flow, interaction between diffusions, temperature gradient and stress gradient.

As an example, the silicon presents stress gradients, meaning that is a piezoresistive material and presents variation in its characteristic resistance due to mechanical stress. This gradient can be represented by isobaric lines along the die that show the different levels of intensity. It is minimum in the central region and maximum along the four corners. Figure 24 shows an example of those isobaric lines.

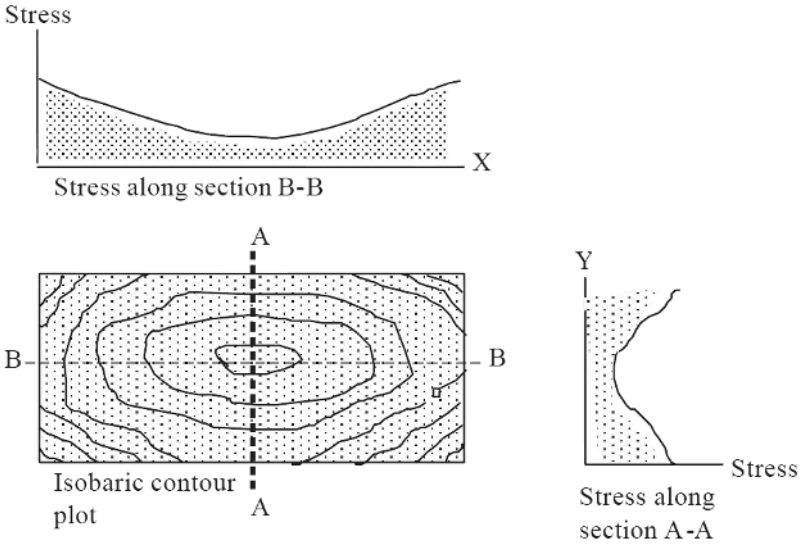

Fig. 24. Example of isobaric lines.

Consequently, it is recommended that components to be matched are placed near to each other to minimize the mechanical stress. The mechanical stress difference between two matched components is proportional to the stress gradient and their distance. For calculations purposes, the location of the component is determined as the average

contribution of each section of the component as a whole. The resultant location is called centroid of the component. It is important that any symmetric axis crosses the centroid of the device or component. Some examples of centroid configurations are depicted in Figure 25.

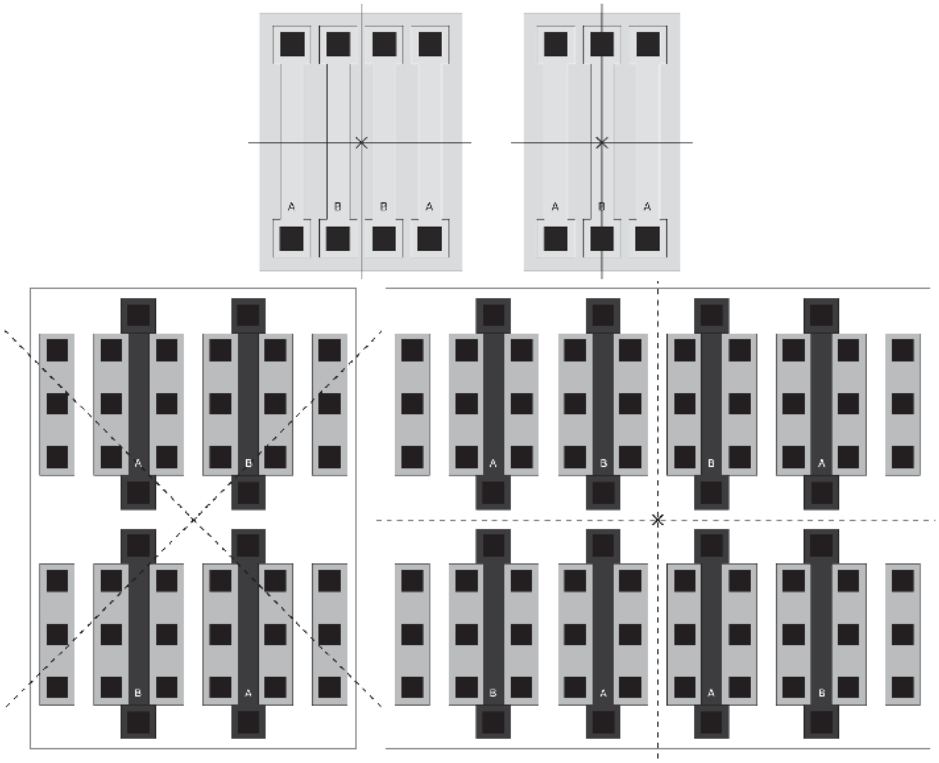

Fig. 25. Examples of centroid layout configurations.

The effects of mechanical stress in integrated resistors are quantified in terms of piezoresistivity, position of the centroids and stress gradients. These effects can be minimized by the proper choice of a low piezoresistivity material or by the resistor orientation in the wafer according to the minimum stress gradients. Other recommendation is the reduction of the distance between the centroids.

The temperature gradients can be analyzed in the same way as the stress gradients. Temperature gradients are obtained by isothermal lines and are separated from each other by a predefined temperature difference (ΔT). These temperature gradients are maximum around the perimeter of the component, and gradually, decrease towards the center.

The temperature effects are minimized in a similar way as the stress gradient: by using low linear temperature coefficient, by using minimal lines of the temperature gradient and by reducing the distance between the centroids.

Mainly for analog integrated circuits, the layout of two matched components is usually implemented by dividing each component into identical sections, placed symmetrically in a matrix array.

The common centroid layout, along with matched components placed in a matrix array in identical and symmetrical sections, is essential to reduce or even eliminate the systematic mismatching. Since the distance between the centroids is null, the mismatching caused by mechanical and temperature stress will be null. As an example, transistors on differential pair are placed in a cross coupled pattern.
In order to properly generate centroid layout, some rules must be observed (Hastings 2001):

1. Coincidence: Matched devices must have a common centroids or as close as possible;
2. Symmetry: The component matrix must be symmetrical in both X and Y axis. Ideally, the symmetry must be a consequence of the components placement and not the symmetry of each one individually;
3. Dispersion: The matrix must offer the greatest dispersion level, in other words, each component must be placed with high possible symmetry along the matrix array;
4. Compression: The matrix should be as compact as possible, ideally close to a square shape.

The random mismatch is different on each device and it is caused by microcospical irregularities in the materials or fabrication process. It can be reduced using the proper geometric aspect of the matched components. This geometric aspect is based in physical and statistical models that are characterized by the fabrication process Patrick & McAndrew, 2003).
Physically, the microscopic irregularities results from the material granularity (ex. polysilicon), photolithography errors, doping injections, thickness and permittivity of the gate oxide, etc. The effect of those errors may decreased as the components geometric aspect increase, since these parameters reach averaged values for large widths and areas.
Two parameters are considered in order to model the random mismatch: the process and the electrical parameters. Process parameters are physically independent and control the device electrical characteristics. In the case of a MOS transistor, the process and electrical parameters that have must be taken into account to matching purposes are listed in Table 5.

Process Parameters	Electrical Parameters
Flat band voltage	Drain current
Mobility	Gate-Source voltage
Substrate Doping Concentration	Transconductance
Chanel length variation	Output resistance
Chanel width variation	
Short channel effect	
Narrow channel effect	
Gate oxide thickness	
Source/Drain sheet resistance	

Table 5. Process and electrical parameters for component matching.

A CMOS process allows also the fabrication of bipolar transistors. Those transistors are also subject to matching rules. A lateral bipolar transistor does not have a good matching when compared with a vertical one. The poor matching of the lateral transistors are due to the surface effects and impossibility using large emitter areas.
Some rules for bipolar transistor matching are:

1. Identical geometric aspects for the emitter and collector since they affect the current flow in lateral transistors;

2. Minimum emitter area for matched transistors, otherwise there will be a degradation in the current gain (β);
3. Guard ring around the base to ensure that electrostatics charges will not influence the current flow in the neutral base;
4. Use of multiple collectors for lateral PNP transistors. A moderate match can be reached when the collectors are identical and out of the saturation condition;
5. The matched transistors should be close to each other in order to minimize the impact of the thermal gradient.
6. The matched transistors should be placed in gradients lines of minimum stress;
7. The transistor must be aligned with the wafer axis;
8. Place as many metal contacts as possible in the emitter (following the emitter geometry) to reduce the contact resistance and to distribute the current flow uniformly;
9. Use emitter degeneration. Lateral PNP transistors are often more benefited with emitter degeneration compared to the NPN vertical counterparts due to the Early voltage and the large emitter area. They are commonly used in current mirrors.

The matching over integrated components reflects the overall performance of the entire circuit or system. Depending on the matching accuracy, the circuits may present:

1. Minimum: In the range of ± 1% (representing 6 to 7 bits of resolution). Used for general use components in an analog circuit, such as current mirrors and biasing circuits;
2. Moderate: In the range of ± 0.1% (representing 9 to 10 bits of resolution). Used in bandgap references, operational amplifiers and input stage of voltage comparators. This range is the most appropriate for analog designs.
3. Severe: In the range of ± 0.01% (representing 13 t0 14 bits of resolution). Used in high precision analog to digital converters (ADCs) and digital to analog converters (DACs). Analog designs that use capacitors ratio reach this range easer then those that using resistors ratios.

Figure 26 shows an example of a PNP vertical bipolar transistor layout.

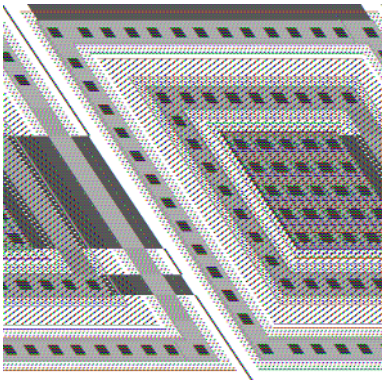

Fig. 26. PNP vertical bipolar transistor example.

9. LVR measurements

The example LVR was diffused in a 0.35µm standard CMOS process. It took an area of approximately 0.25 [mm^2].

Figure 27 depicts the testing structure utilized to measure the main LVR parameters.
It is used a commercial operational amplifier (LM318) as a buffer to isolate the chip. The load current can be adjusted by potentiometer P_1 and the total load capacitance, considering the all parasitic, was measured as 30 [pF].
Before any LVR measure, the LM318 offset voltage was compensated through the procedure provided by the manufacturer. All the power supply lines are decoupled by 10 [µF] capacitors.

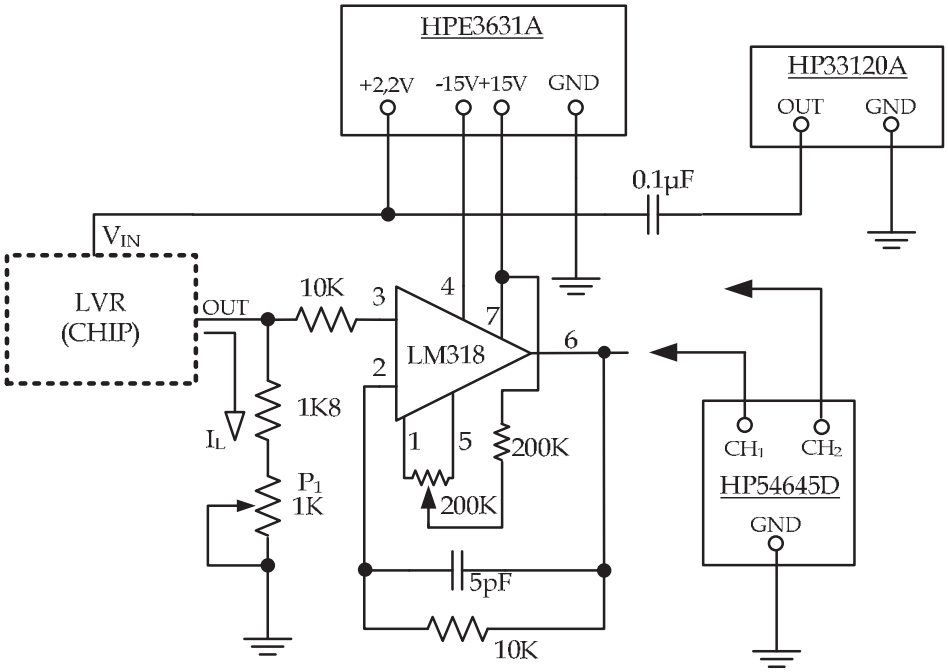

Fig. 27. The test structure to measure the LVR parameters.

Parameters	Simulated	Measured
T_{NOM}	37[ºC]	37[ºC]
V_{IN}	2.2[V]	2,218[V]
$I_{L(NOM)}$	0.5[mA]	0.5[mA]
$P_{D(NOM)}$	1.17[mW]	1.186[mW]
V_{OUT}	1[V] @ I_L = 0.5mA	1.038[V] @ I_L = 5[µA] 1.004[V]@ I_L = 0.5[mA]
I_Q	30[µA]	39[µA]
PSRR @ 10MHz	-42.6dB	-38dB
E_{FF} related to V_{IN}	42.8[%]	42.3[%]
T_{SET} @ 0,1%	14.87[µs]	18.6[µs]
OTA dominant pole	130[Hz]	126[Hz]

Table 6. Main LVR simulated and measured parameters.

Figure 28 shows the LVR response to a voltage step input and reveals a BIBO (bounded input – bounded output) system, in other words, the system is unconditionally stable and there is no need of any extra external component.
Table 6 is a comparison between the simulated and measured parameters.

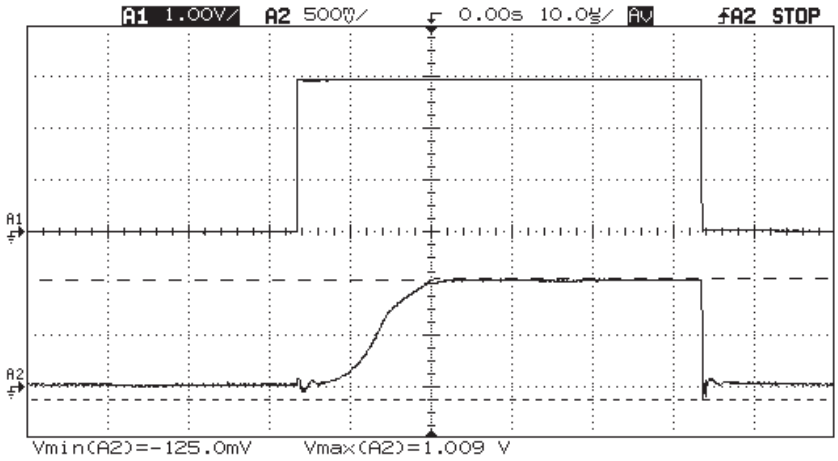

Fig. 28. LVR step response indicating a BIBO system.

The measured values show a good conformity with the simulated ones indicating proper design considerations.

10. Conclusions

We are witnessing the great revolution that has been imposed since the manufacture of the first bipolar transistor in the late 50s of the twentieth century. Electronics solutions are going to microelectronics and microelectronics is evolving to nanoelectronics. All these developments bring with them the yearning of the human being to access more efficient equipment. So, in virtually all branches of activities we will find what is called "High-Tec".
Medicine and its related sciences could not stay apart from this explosion of technology and intelligently sought the partnership with this powerful tool for circuit design.
Some solutions point to implantable systems (which would reduce the use of invasive techniques) that can be taken up on an outpatient basis and connected into a means of communication for a distance evaluation by a health professional.
The main objective of this chapter was the development of a voltage regulator for implantable applications. Some boundary conditions allow classic Figures of Merit, such as the temperature dependence, to be less severe, since the body temperature is kept constant. Another key issue was to search for solutions that avoid the presence of any external component. This is an essential boundary condition since the topology of classical LDO regulators depends on the presence of a capacitor (usually electrolytic and therefore too large for this application) connected in parallel with the load. Other regulators reported in the literature uses complex circuits or circuits that requires large silicon area.

The circuit described is a compromise of additional power dissipation in the source follower stage and unconditional stability. Even with the additional dissipation, the total power of the regulator (about 1.2 [mW]) is within a safe limit.

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With the increased adoption of RFID (Radio Frequency Identification) across multiple industries, new research opportunities have arisen among many academic and engineering communities who are currently interested in maximizing the practice potential of this technology and in minimizing all its potential risks. Aiming at providing an outstanding survey of recent advances in RFID technology, this book brings together interesting research results and innovative ideas from scholars and researchers worldwide. Current Trends and Challenges in RFID offers important insights into: RF/RFID Background, RFID Tag/Antennas, RFID Readers, RFID Protocols and Algorithms, RFID Applications and Solutions. Comprehensive enough, the present book is invaluable to engineers, scholars, graduate students, industrial and technology insiders, as well as engineering and technology aficionados.

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