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A 0.13um CMOS 6-9GHz 9-Bands Double-Carrier OFDM Transceiver for Ultra Wideband Applications

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1. Introduction

Since 2002, ultra wideband (UWB) technology has ignited the interests of academia and industry for its potential of achieving high-speed wireless communication in short distance with low power. It is actively investigated today due to the wide available bandwidth for very high data rate up to 480Mb/s and low power service over short distances in 10m range. According to FCC (Federal Communications Commission), the frequency spectrum allocated for UWB is 3.1-10.6 GHz, and the spectrum shape of modulated output power and maximum power level are limited to -41.3dBm/MHz, which ensures that UWB can coexist with existing spectrum users like GSM(Global System of Mobile communication), WLAN(Wireless Local Area Network) and Bluetooth.

Based on MB-OFDM(Multi-Band Orthogonal Frequency Division Multiplexing), WiMedia released the initial version of Physical Layer (PHY) Specification in September 2005. In this proposal, the UWB frequency spectrum from 3.1 GHz to 10.6 GHz is divided into 14 channels with 528MHz for each channel. These sub-bands are grouped into five band groups. It is seen that by increasing the signal bandwidth significantly, ultra-wideband achieves a high channel capacity and becomes an attractive solution to the ever-increasing data rate demands in wireless personal area networks (WPAN). In December 2005, European Computer Manufacturer's Association (ECMA) proposed the standard ECMA 368/369 on high-speed UWB physics layer and media access control layer based on MB-OFDM scheme. This has pushed the industrialization of UWB technology to a new stage again.

In China, UWB technology has also become a hot topic according to the issue of the UWB standard by Chinese Government in 2008. A new UWB scheme named dual carrier-orthogonal frequency division multiplexing (DC-OFDM) has been proposed and applied in China. In China standard, only the band from 6.2GHz to 9.4GHz and the band from 4.2GHz to 4.8GHz are available for UWB applications. These bands are partitioned into 14 sub-bands of 264MHz bandwidth which means the bandwidth is halved in China's DC-OFDM standard compared with the ECMA 368/369 standard. Thus the sampling frequency of the DACs(Digital-to-Analog Converter) and ADCs(Analog-to-Digital Converter) are halved too. The power consumption of the system can be reduced greatly. Moreover, in DC-OFDM

UWB, two bands locating around two different carriers are utilized at the same time to form a bandwidth of 528 MHz for maintaining high-speed communication. In this way, the spectrum usage is more flexible and the spectrum efficiency is enhanced. However, the requirements of less than 9-ns hopping time of the carrier frequency as well as simultaneous dual-carrier outputs challenge the design of dual-carrier frequency synthesizer. Fig.1 shows the frequency spectrum for WiMedia and China UWB standard.

A fully integrated transceiver for DC-OFDM UWB system in the 6-9GHz band is present in this chapter. This chapter will describe the realization of a DC-OFDM UWB transceiver covering 6-9GHz bands in a low cost 0.13um CMOS process. Firstly, the RF receiver design will be described in section 2. Section 3 and 4 introduce respectively the designs of the RF transmitter and the 9-bands frequency synthesizer. The detailed measurement results are demonstrated in section 5, which is followed by the conclusions in section 6.

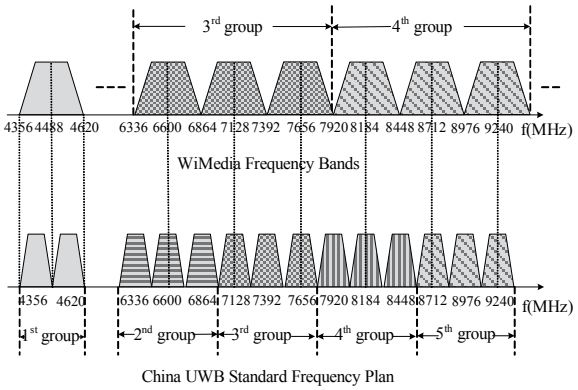

Fig. 1. Frequency spectrum for WiMedia and China UWB standard

2. RF receiver design

Fig.2 shows a block diagram of the proposed UWB receiver. Signals are received and filtered by the off-chip antenna and the RF(Radio Frequency) filter firstly. And then the received signals are amplified and converted to IF(Inter-media Frequency) baseband signal by RF front-end building blocks. After further filtering and amplifying, the analog baseband signals should be large enough to drive the ADC for digital signal processing. The receiver's local oscillator (LO) should be a fast-hopping frequency synthesizer that generates carrier tones according to the band plan in Fig.1. Performances such as in-band phase noise and reference spur are specified as -80 dBc and -40dBc respectively, which are not so stringent. And the I/Q mismatch is designed as 2.5 degree and 0.2 dB.

Normally the noise figure of channel select filter is around 30 dB, thus the conversion gain of RF front-end building blocks should be larger than 30 dB to suppress the noise from LPF(Low Pass Filter). But in that case, the linearity of the receiver will get worse. In order to improve the linearity of the receiver, the conversion gain of the RF front-end building blocks is set to be around 24 dB(average) with variable gain of 12 dB. The NF(Noise Figure) of the LPF is designed to be less than 18 dB to guarantee low noise of the receiver. The LNA(Low Noise Amplifier) utilizes a fully differential structure and presents an input matching to

50ohm for the off-chip antenna. It should provide a maximum gain of 18 dB to suppress noise from mixer and baseband circuits. As LNA sets the baseline for the noise figure of the receiver, the NF of the LNA should be optimized to lower than 5 dB. Following is a quadrature mixer with a fixed gain of 6 dB. The 5th-order Chebyshev type band-selection LPF is implemented after the mixer. Unlike normal channel select filter, the proposed LPF should provide a maximum gain of 30 dB, with a NF less than 18 dB at maximum gain mode.

According to the Friis Equation, the noise of the LPF nearly doesn't contribute to the total input referred noise of the receiver, leading to a very low noise figure. As the back-end block of the receiver, the filter tackles with slightly large signals, leading to stringent linearity requirement for the filter. Since the filter suppresses adjacent channel interferers to some extent, the linearity of the filter is proportionally improved. Sharp rejection of out-of-band signal is also required. Considering the difference between the sub-band's bandwidth of two standards, the cut-off frequency of the filter is switchable between 264 MHz and 132 MHz. Finally, the PGA(Programmable Gain Amplifier) amplifies the signal from the LPF and delivers constant-magnitude signals to the ADC.

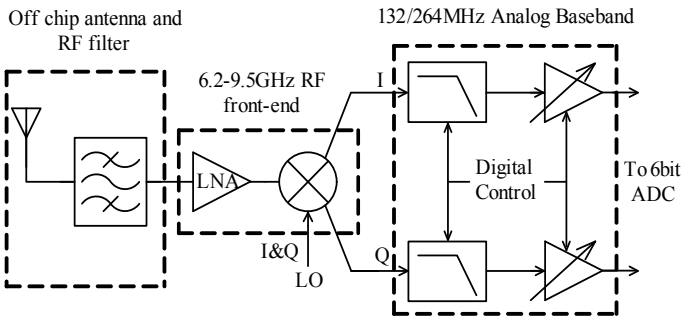

Fig. 2. Architecture of the proposed receiver

2.1 RF front-end design

Attaining an input impedance match for the wide band receiver is particularly difficult because parasitic may dominant the input impedance network. Fig.3 gives a presentation of the LNA for the proposed UWB receiver. A resistive shunt feedback topology is adopted in the LNA design, which achieves a wideband matching with a good balance between area cost and performances. Although there is a slight degradation of the noise figure comparing to other techniques like LC ladder (Bevilacqua A. et al., 2004) and transformer feedback matching (Shin D. H., et al., 2007), quite a large number of inductor coils are avoided. Bonding wire inductance $L_{bonding}$ and the ESD(Electro-Static Discharge) capacitance together with the PAD capacitance C_{pad} are co-designed with other on-chip components. The load stage is an R-L-C tank. The load inductor LL can be replaced by a differential inductor to get a smaller area. However, we split it into two symmetrical inductors for convenience of cascading with mixer in the layout. A fully differential topology is utilized in LNA design to have the input impedance match independent of the bonding wire inductance from the source of M1 to ground. Fig.4 shows the simulated S11 with different bonding wire inductance.

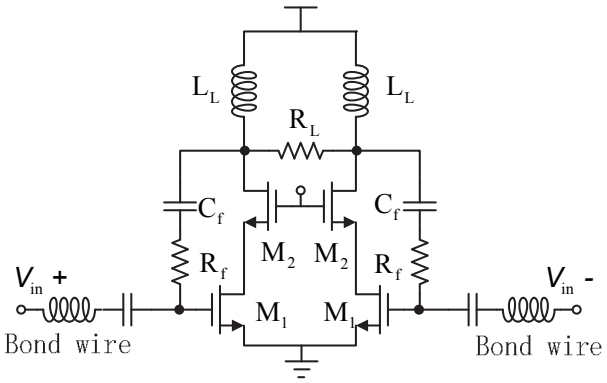

Fig. 3. Schematic Diagram of Low Noise Amplifier

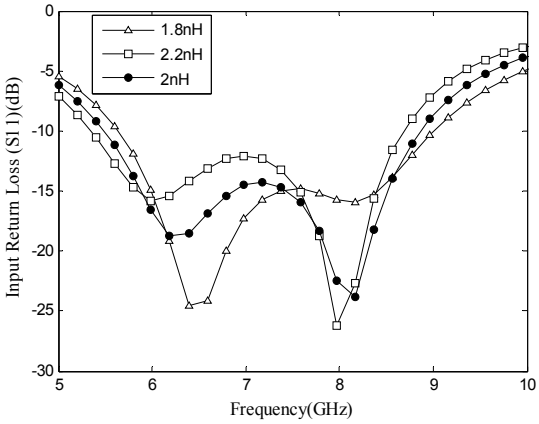

Fig. 4. Simulated S11 with different bonding wire inductance

Fig.5 shows the folded quadarture down- conversion mixer for the UWB receiver. A fully differential Gilbert-cell based structure with I/Q branches sharing the same RF input stage is implemented in the mixer, which eliminates the mismatch present in down conversion topology with separate I/Q mixers. Exploring merged architecture (Sjöland H, et al., 2003) for the quadrature mixer can also minimize the capacitive load to the LNA. Compared with the traditional structure of mixer, the folded structure utilized in this work separates the input stage and switching stage. Thus different bias current can be applied to the input stage and switching stage, better performances are achieved. The bias current of the input stage is bigger to guarantee good performance on conversion gain and noise figure. On the contrary, small current in the switching stage can lower the 1/f noise and dc-offset, which is significantly important in zero-IF receivers.

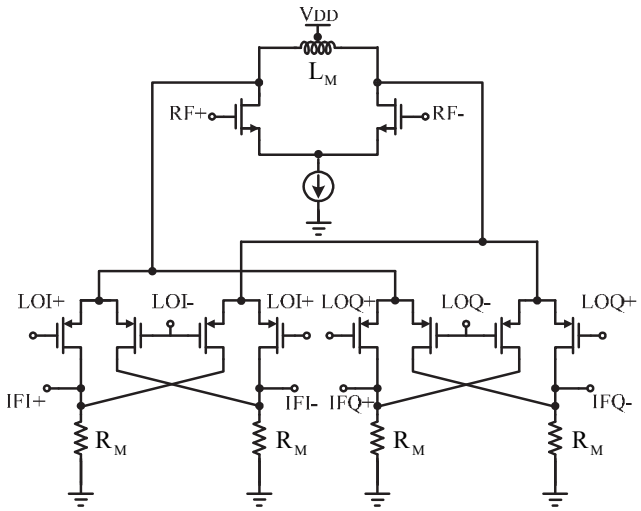

Fig. 5. Quadrature down conversion mixer circuit

2.2 Analog base-band design

The main difference between the two standards is that the intermediate frequency is 4.125MHz-264MHz and 1MHz-132MHz for WiMedia MB-OFDM and China UWB standard respectively. In order to support both standards, the cut-off frequency of the band-select filter should be switchable between 132MHz and 264MHz. Using two different filters to support each standard may be a possible solution, but will sacrifice a lot of die area. Furthermore, as the first stage of IF stage, the NF and linearity of the filter should be optimized. Thus the LPF should provide variable gain to suppress noise substantially at maximum gain mode and meet the linearity requirement when set as minimum gain. In this work, a fifth-order Chebyshev type programmable Gm-C filter is implemented.

The fifth order low pass filter is realized by a cascade of a first order RC filter and two biquads. The proposed architectures of the low pass filter and the biquad are illustrated in Fig.6. Note that the down-conversion mixer's load resistors are utilized to form the first passive RC filter stage. As a result, simulations covering both the mixer and the filters should be taken to make sure that the overall frequency response and gain are optimized.

The modified Nauta Gm cell (as shown in Fig.7) is implemented as the OTA(Operational Transconductance Amplifier) in the filter. The transconductances of the all the OTA are controlled by the digital data.

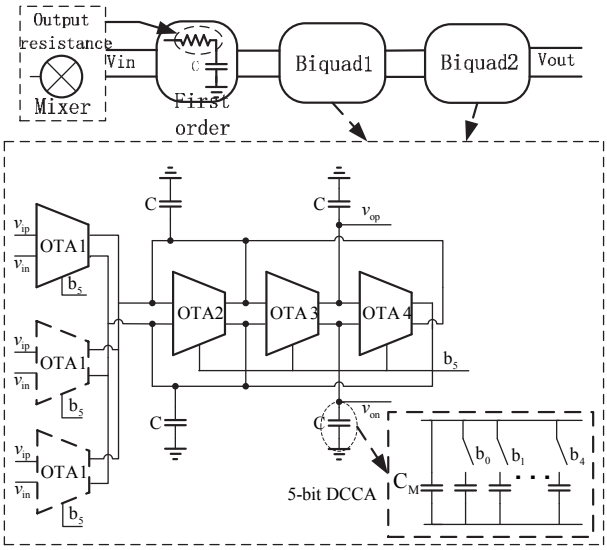

Fig. 6. Structure of the Low Pass Filter

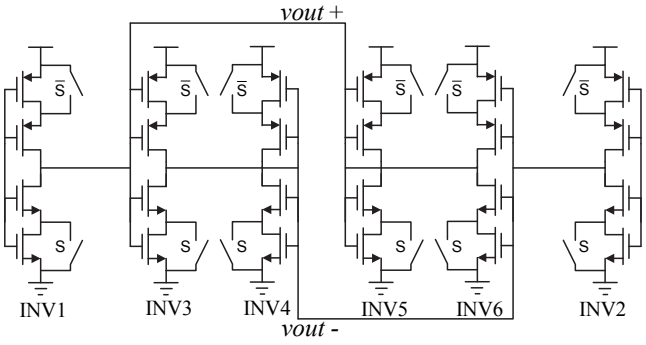

Fig. 7. Modified Nauta OTA

The topology of the PGA (Programmable Gain Amplifier) is based on a source degenerated structure as illustrated in Fig.8. A switched resistor array is implemented to achieve variable gain from 0dB to 18dB with 2dB/step. High-gain amplification easily causes the following stages into saturation due to DC-offset and DC offset also leads to second-order harmonic distortion (HD2) of the received signals, resulting in SNR(Signal-to-Noise Ratio) degradation. Thus the DC-offset cancellation circuits are also included in the PGA design. The amplitude response of the PGA is designed to be flatness within the frequency range of 264MHz.

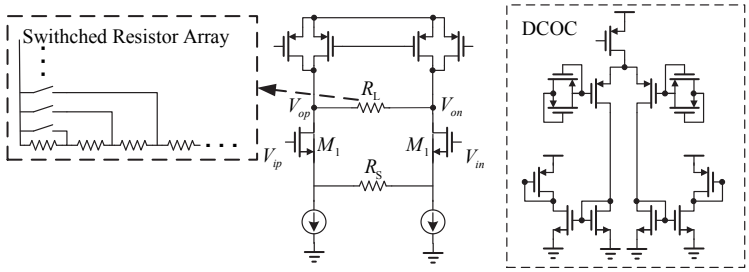

Fig. 8. Topology of the PGA

3. RF transmitter design

The proposed transmitter utilizes the direct conversion architecture for its easiness of integration and low cost. As shown in Fig.9, it consists of a dual-mode I/Q LPF with mode-switch circuits, an I/Q up-conversion mixer with high-linear voltage-to-current (V2I) units, a two-stage power driver amplifier (PA). Besides, the trans-impedance amplifiers (TIAs) are integrated to measure the AC transfer character of the LPF.

The main signal flow of this transmitter is as follows. The ABB(Analog Baseband) voltage signals from the DACs are applied at the inputs of the I/Q LPF. With the correct mode-switch bit as well as the Digital Control Capacitor Array (DCCA) control word, the image signals of the DACs and the unwanted high frequency spurs are all filtered out in both 264-MHz and 132-MHz modes. After the output voltages of the LPF are converted into ABB currents by V2I units, they are up-converted into RF voltages by the switches in the up-conversion mixer at the rate of LO. Lastly, the differential RF voltages are amplified by PA(Power Amplifier) and are converted into single-ended one via the 6-9 GHz off-chip balun, to drive the antenna.

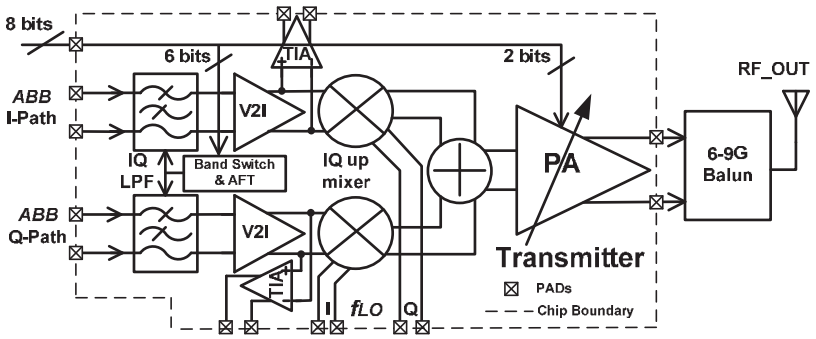

Fig. 9. Block diagram of the proposed transmitter

3.1 Dual-mode I/Q LPF design

The main requirements of this LPF are the attenuation of the out-band signals, the in-band ripple, the dual-mode operation with accurate cut-off frequency controlling and accommodation to the large input ABB voltages. According to the sampling rate of a common UWB DAC, the LPF should have an attenuation of about 45 dB from 264/132 MHz

to 600/300 MHz at 264/132-MHz mode. Moreover, an in-band ripple of 0.5 dB is required. To obtain comparably good phase linearity, the 5th-order Chebyshev gm-c LPF is proposed. Besides, to deal with the ABB voltage as large as 300mVpp, the passive sub-filter is placed as the 1st-stage and the high-Q biquad is as the last stage. Also, to improve the linearity of the LPF under low supply voltage with low power, the trans-conductors are built with the Nauta's structure (Nauta B, et al., 1992).

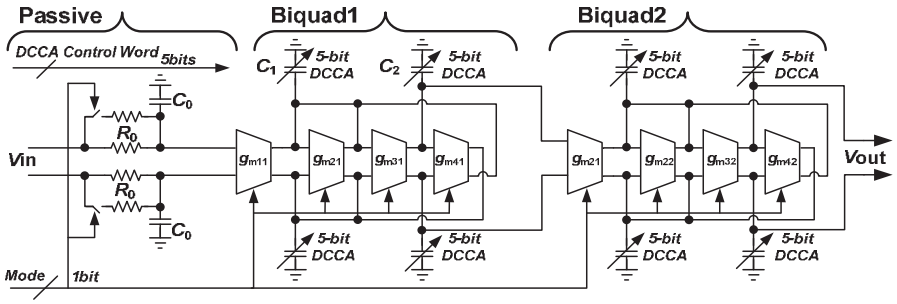

Fig. 10. Architecture of the 5th-order Chebyshev LPF with mode-switch circuits

3.2 Up-conversion mixer design

The simplified I-path schematic of the up-mixer is shown in Fig.11. It utilizes two double balanced Gilbert cells with their outputs summed to realize single-sideband (SSB) up-mixing. Since the I/Q up-mixer acts as I/Q modulator and up-conversion mixer in direct conversion transmitter, the performances of the transmitter are mainly determined by this circuit.

Low spurs, high linearity and wide bandwidth are the main challenges for the design of this up-conversion mixer. The main spurs in the output spectrum of the transmitter are the LO leakage and the sideband signal. The power of the LO leakage is determined by the offset of the I/Q ABB path. In order to reduce the power of LO leakage, an AC coupling is utilized between the V2I unit and the switches of the up-mixer as shown in Fig. 11. Besides, the linearity of the up-mixer is mainly affected by the V2I unit while the impact of the switch stage is of less importance (Zheng Renliang, et al., 2009). Many techniques (Willy Sansen, 2006) have been proposed to improve the linearity of the V2I unit. Although the complete OPAMP-assisted V2I possess better linearity, its application is restricted by the power consumption to achieve sufficient GBW(Gain Bandwidth) of the OPAMP for UWB ABB as well as the limited voltage swing because of the low supply voltage. Instead, the simple OPAMP-assisted V2I unit is preferred. As shown in Fig.11, the V2I unit consists of the input PMOS transistor M1, the source degeneration resistor R1, the current-mirror transistor M2, M3, the AC coupling capacitor CB as well as the bias resistor for eliminating the DC-offset in V2I. The feedback loop is composed of M1, R1, M2, I1 and I2, where M2 acts as the simple single-transistor OPAMP. When applied at the gate of M1, the input ABB voltage is directed transferred to the terminals of R1, because any voltage changes at the gate will be transferred to the source of M1 to maintain a fixed V_{GS} as required by the current source I1 and I2. Thus the input voltage is converted linearly into its current counterpart with a gain of 1/R1. The converted current Δi circulates in M2. Then it is mirrored into the up-mixer by M3. A 400-Ω R1 is used to improve the linearity at the cost of the gain loss in V2I. To

compensate it, a 6-dB gain is set at the current mirror. Furthermore, a broadband operation of the mixer is achieved by employing a differential inductor Ld to peak with the parasitic capacitance Cpar and two series resistors Rs to reduce Q of the overall load network.

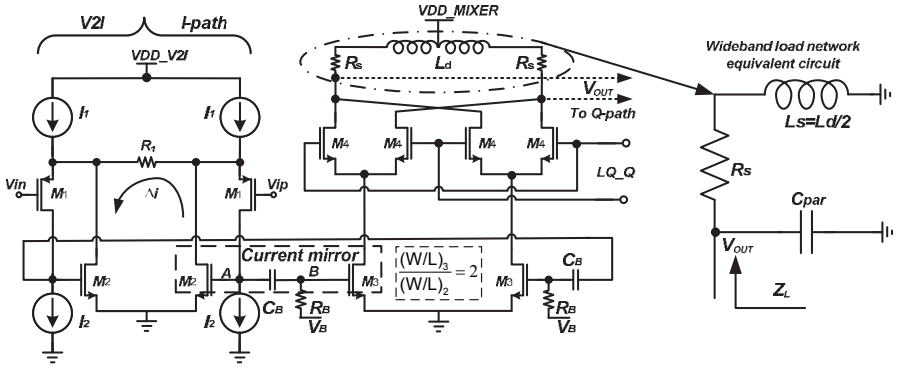

Fig. 11. Simplified I-path schematic of the up-mixer and its wideband load network

3.3 Power driver amplifier

Since the PA is the last stage of the transmitting chain, its linearity determines the output IP3(Input 3rd order Intercept Point) of the transmitter according to the Friis' formula. Moreover, the PA should possess sufficient gain to boost the output power of the up-mixer as well as to reduce the impact of former stages on the linearity of the transmitter. A flat gain of the PA is desired, too. Besides, considerations of the rejection to common-mode interferences should be taken because the tail current sources are eliminated to fit the low supply voltage.

As shown in Fig.12, the 1st stage of the PA is a combination of source follower (M1) and common source (M2) amplifier (Chang-Wan Kim, et al., 2005). The phase shift of the signal passing through the two amplifiers is 0° and 180° respectively. When the input signal Vin is applied at the two amplifiers, the common-mode signals in Vin become out-of-phase and their amplitudes are subtracted at node X/Y while the differential-mode signals in Vin become in-phase and their amplitudes are added at node X/Y. In this configuration, the input differential signals are amplified with the common-mode signals rejected. Therefore, the 1st stage increases the common-mode rejection ratio (CMRR) of the transmitter. In order to obtain a high CMRR, the gain of the two appliers, i.e. the source follower and the common source amplifier, should be equal. The transistors M1 and M2 have the identical size. Under this condition the ideal CMRR is infinite and the differential voltage gain is 6 dB. However, the post simulation of this circuit indicates that the CMRR is improved by 12 dB and the differential voltage gain is about +2 dB because the inherent unbalances between the two amplifiers. Moreover, as the impact of the parasitic capacitors the gain drops at high frequency.

The 2nd stage of the PA amplifies the RF signals to drive the off-chip balun. As the main amplification stage in this PA, its gain and linearity are important. Thus a class-A common source amplifier (Ma) is employed. A differential inductor (LPA) with center tap is used as the load of this stage to resonate with the capacitance including the parasitic capacitance of Mc as well as the PAD. Because the effective 50-Ω input resistors of balun-2 are part of the

load network, its Q value is low and the gain is relatively flat. The value of the LPA is optimized according to the PAD capacitance Cpad and the bonding inductance Lb to ensure the peak of the gain is around 9 GHz instead of the middle of 6-9 GHz. Thus it compensates the gain drop of the 1st stage at high frequency. Besides, in this PA the cascode transistors, i.e. M3 and Mc, ease the Miller Effect to reduce the effective loading capacitance to the former stage and avoid the breakdown of the transistors during large signal period. 2-bit digital signals are used to select the required bias voltage for Ma; an 8-dB variable gain is realized.

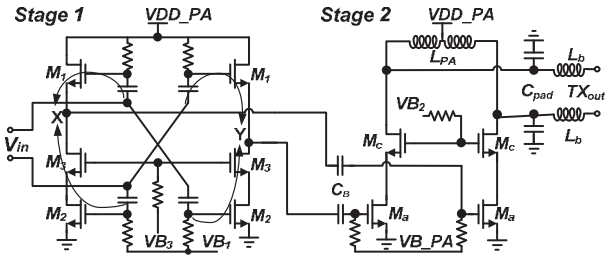

Fig. 12. Simplified schematic of two-stage PA

4. 9-bands frequency synthesizer

According to the band partition for UWB communication system shown in Fig.1, the SSB mixer-based generator for the frequency generations from group2 to group5 is proposed in Fig.13. It is based on the band generation plan (shown in Fig.14), which is designed with the objective of attaining a synthesizer solution that uses a minimum number of components while reducing the generation of spurs.

A PLL(Phase-Locked Loop) with quadrature voltage-controlled oscillator (QVCO) and an external reference of 48 MHz is implemented to generate 8448 MHz I/Q outputs as the fundamental LO frequency. The 8448 MHz in-phase and quadrature phase (I/Q) signals are applied to the quadrature SSB (QSSB) mixer to mix with another input whose frequency is switchable. These switchable input frequencies for QSSB mixer can be derived either from divided-by-2 dividers' output or from a combination of a SSB mixer1 and a divided-by-2 divider. The final output phase accuracy largely depends on the quadrature input signals of the QSSB-mixer. Since divided-by-2 dividers are used to produce I/Q signals for some synthesized frequencies for high phase accuracy. The divider's phase sequence and spectral purity may impact the mixer's phase accuracy. A double balanced quadrature-input divided-by-2 (DBQID) frequency divider is implemented to suppress the third harmonic with high precise quadrature phase sequence.

Two frequency multiplexers are used to choose the right internal frequency for each channel. The band selection is accomplished by switching the capacitor bank of the QSSB mixers to the desired frequency and simultaneously switching its input to the desired frequency and phase. Fast switching can be achieved since they operate simultaneously. To suppress the sidebands caused by nonlinearity and mismatch at the output, the number of SSB mixers has been minimized. The synthesizer's output frequencies are given as f_{fs_out}=8448+/-264*m where m=0,1,2,3. and f_{fs_out}=8448-264*n where n=4,5,6,7,8. The I/Q vectors of the internal frequencies travel through different traces and inevitably suffer from

phase and gain mismatches when they reach the QSSB mixers. A Clock buffer is inserted before the QSSB mixer to calibrate the phase and gain mismatches of the input signals coming from different paths.

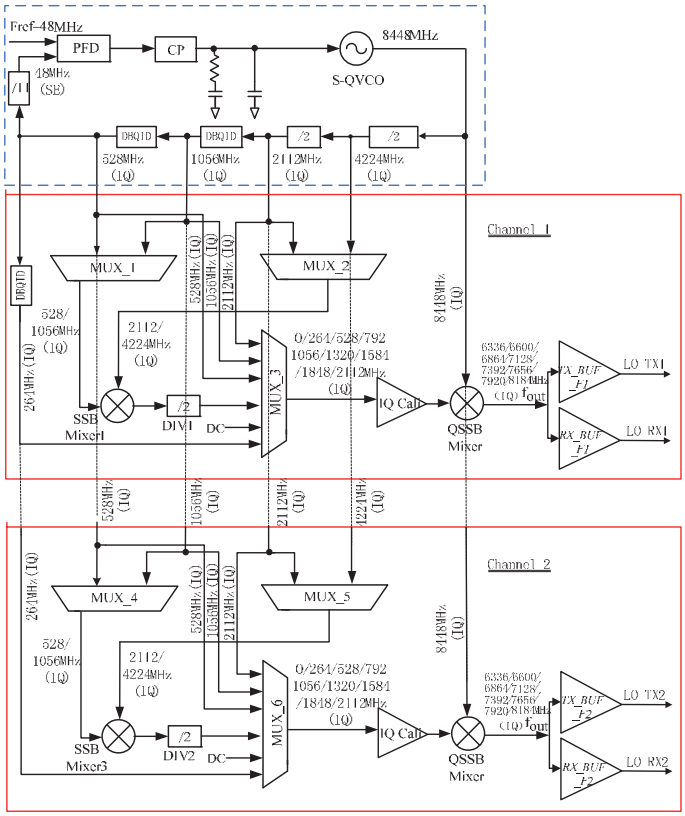

Fig. 13. Architecture of the proposed frequency synthesizer

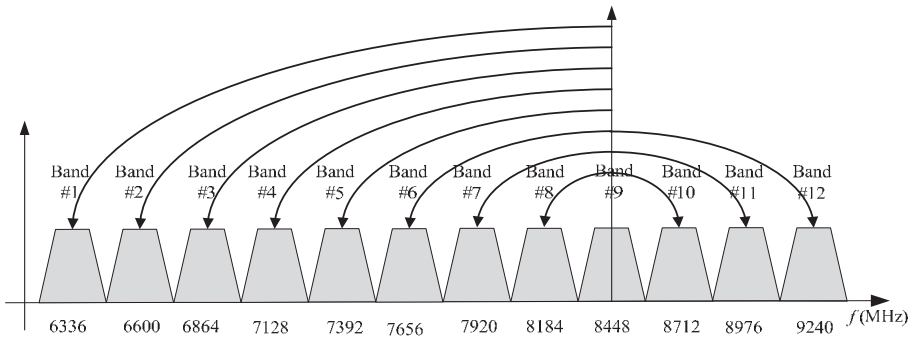

Fig. 14. Frequency plan of the proposed frequency synthesizer

4.1 QVCO design

The QVCO is the most important circuit in a PLL and its phase noise greatly determines the overall PLL output noise performance. Quadrature coupling transistors in parallel quadrature voltage-controlled oscillator (P-QVCO) make a large contribution to the phase noise. A cascode structure can greatly reduce the noise from the cascode device. Better phase noise performance can be achieved by series connection between coupling and switching transistors (Andreani P, et al., 2007).

In the case of P-QVCO, through changing the ratio of the width of coupling transistor to the width of switching transistor, phase noise and phase error can be deal with for each other. The phase error cannot be improved by increasing phase noise for the series quadrature voltage-controlled oscillator (S-QVCO). The phase error of S-QVCO depends on the amount better phase error but worse phase noise performance. To suppress the sideband caused by phase error, top-series QVCO(TS-QVCO) is adopted to generate quadrature LO signal. The width ratio of coupling transistor to switching transistor is 1/2.

As shown in Fig. 15, a linearization technique is used to lower effective K_{VCO} whereas maintain a same tuning range (Kuo C, et al., 2006). By employing this linearization, nearly the whole supply voltage range can be exploited. The varactors biased at different voltages connect with metal-insulator-metal capacitors in series as dc blockers. The dc bias voltages are generated by a resistor ladder. The resonators are both made of a differential inductor, an array of 7 bits two binary weighted switched capacitors and thick oxide MOS varactors. The tuning voltage ranges from 0 to 1.2 V. A small K_{VCO}=60 MHz/V is adopted to achieve low AM-FM noise conversion. To filter the flicker noise from the tail current transistors, a large MOS capacitor is used at the gate of the current mirror.

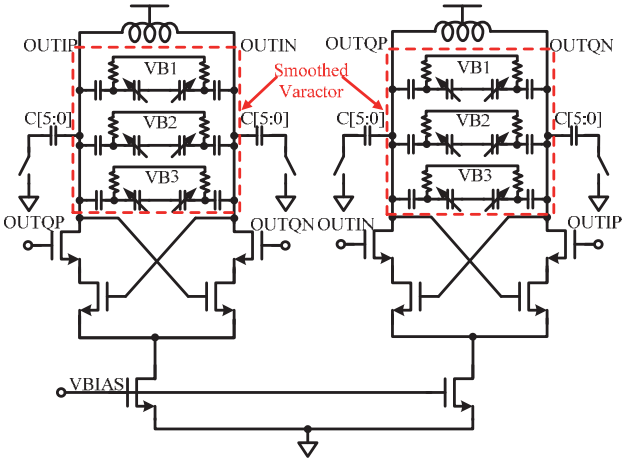

Fig. 15. Schematic of TS-QVCO

4.2 Multiplexer

The multiplexers (MUX) are based on several differential pairs sharing a common resistance load. Their activation or deactivation is through a signal enable or disable the tail current. The port leakage and third harmonic rejection are the key issues. If the unselected input frequency is leaked at the output, it will generate unwanted center frequency, which

poisons the output frequency even more than those frequencies not at the center of the bands. For the third MUX, it has as many as six inputs. Thus the port leakage must be solved. There are several methods to suppress the port leakage such as cascode structure. But it is not well suited in a low voltage application.

In this design, a couple of dummy transistors are added to a conventional current-steering MUX to eliminate the unwanted coupling. Fig.16 shows the circuit of the in-phase path of MUX1. Take transistors M1 and M5 for illustration, their input signals are same, but their drains are connected to the opposite output nodes. When Vin1I is not selected and M5 is omitted, Vin1I will couple to the output through the parasitic capacitance of M1. But with the presence of M5, Vin1I will couple to the opposite output node as well. The common response will be suppressed by the differential circuit. Therefore, good isolation is achieved between different inputs. The dummy input pairs consume no extra power. The tail current source of the dummy pairs is zero and the gate of the corresponding transistor is connected to the ground. Fig.17 shows the output spectra of multiplexers with and without the dummy input pairs. The two circuits are simulated with the same operation frequency and power consumption. It shows a port leakage suppression of 46dB better with the dummy input pairs than without them.

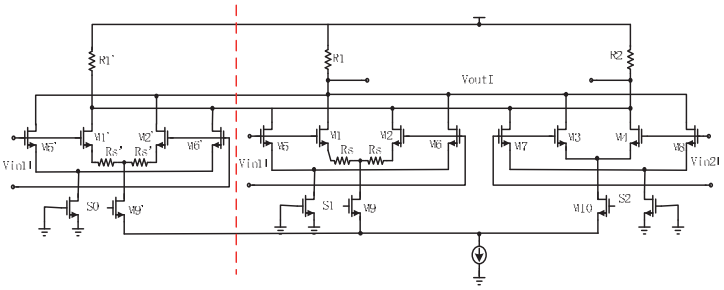

Fig. 16. Schematic of the multiplexer

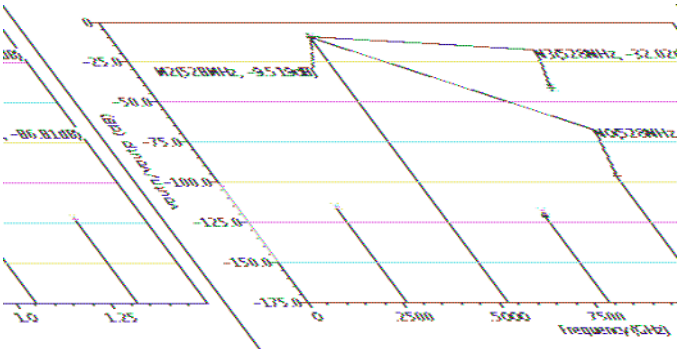

Fig. 17. Simulation result of the MUX with and without the dummy pairs

The output of the MUX is feed to a latter SSB mixer, which functions as up or down conversion according to the input phase sequence. A common way to select up or down conversion is to add a controllable in-phase/opposite-phase buffer before the SSB mixer. In

this design, the phase changing is merged in the MUX. As shown in Fig.16, the part in the left of the line is a replication of the right part, excepting the output which is connected to the opposite side. Hence, S0 and S1 change the phase sequences of Vin1, which helps to change between up and down conversion. As a result, such a configuration minimizes the hardware requirement, power consumption, and undesired sidebands.

4.3 IQ calibration

Phase and gain mismatch at the input would cause image signal at the output of the SSB mixers. In order to counterbalance these mismatch, an IQ calibration module is interpolated before the second SSB mixer. Fig.18 shows the circuit of this module. Two identical buffers driven by the in-phase (0°) and quadrature-phase (180°) signals produce two outputs, normally equal to 45° and 135°, respectively. Here, one of the outputs is adjustable, while the other is fixed. These two outputs are quadrature in ideal. If th,

An interesting phenomenon using this method could be found. That is, the phase mismatch at the input will be transformed into the gain mismatch at the output; and the gain mismatch at the input will be transformed into the phase mismatch at the output. This could be illustrated by Fig.19, wherein In,i and In,q represent the input in-phase and quadrature-phase signal, Out,i and Out,q represent the output in-phase and quadrature-phase signal. It can be easily seen that the phase and amplitude error will be transformed into each other at the end. Hence Vbcon which adjusts the output phase will be used when there are some amplitude mismatches at the input, while Icon which adjusts the output amplitude will be used when there are some phase mismatches at the input. This IQ calibration module should be capacitor coupled to the latter stage, since the output common voltage will be changed as the tail current is adjusted. When Vbcon or Icon changes, the tail-current-source transistor should stay in the saturation region. Hence the drain voltage of M7 should be high enough to cover all the changes. Besides that, the Vdsat of M5 should be high enough, because it will determine the range of the phase adjustable. As a result, the Vgst of the input transistor M1 is inevitably small. This will result in a severe third harmonic. A distortion cancellation technique is used here to ease the situation. An additional pair of transistors M3 and M4 is added to the input. They are cross coupled to the output as to the main input pair M1 and M2. The Vgst of the main pair and the additional pair is set to be 1.6:1 while the tail current is set to be 4:1. The third harmonic could be effectively suppressed in this way, with the cost of a degenerated output voltage.

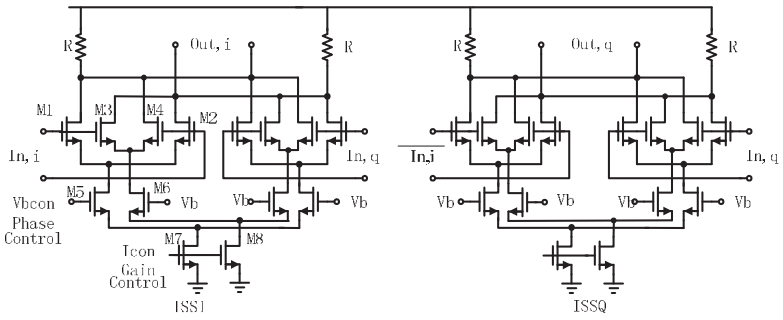

Fig. 18. Schematic of the IQ calibration

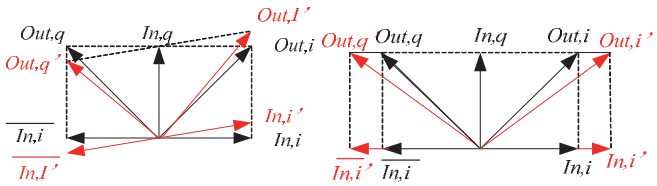

Fig. 19. Illustration of the phase and gain mismatch translation

5. Measurement results

The proposed 6-9GHz DC-OFDM UWB transceiver is fabricated in the 0.13-μm RF CMOS process. Fig.20 shows the die microphotograph. Total employed area including pads is 3.6 mmx4.5 mm.

In order to support both WiMedia MB-OFDM and China UWB standard, the receiver's intermediate frequency is required to be switchable between 4.125-264MHz and 1-132MHz. Fig.21 shows the frequency response of the receiver for two standards with LO signal at 7.656GHz. The receiver achieves variable gain of 18dB to 80dB with 2dB/step for both standards. Gain flatness of less than 3dB is normally achieved. The spectrum mask of the transmitter with 40MHz QPSK modulation signal is shown in Fig.22. The integrated power is calculated at -10dBm.

The measured tuning range of QVCO is from 7.6 to 9.5 GHz. With an external reference of 48MHz, the synthesizer is locked at 8448 MHz with a phase noise is －90 dBc/Hz at 100 kHz offset and －105 dBc/Hz at 1 MHz offset as shown in Fig. 23. A normalized phase noise floor of -226.7 dBc/Hz is achieved. The measured integrated phase noise from 10 kHz to 50 MHz is 1.93˚. The reference spur level is -72 dBc seen from the Agilent E4440 spectrum analyzer. Experimental results reveal that the worst-case sideband occurs at 6336 MHz, which is about -30 dBc without I/Q calibration, as shown in Fig. 24, and is suppressed to below -45 dBc when the calibration is on. The band switching behavior is shown in Fig. 25. The bands are switched periodically and the synthesizer output is monitored. The longest switching time approximately equals to 1.4 ns, much less than 9.5 ns which is specified in dual-carrier MB-OFDM UWB systems.

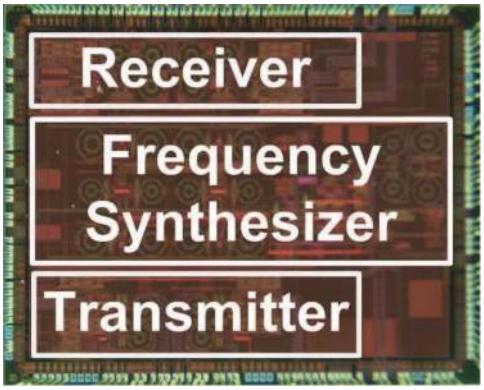

Fig. 20. Die microphotograph of Dual-band 6-9GHz Transceiver

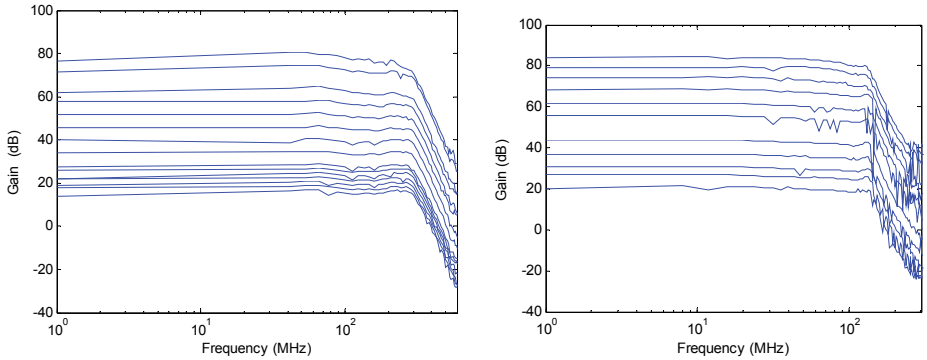

Fig. 21. Receiver frequency response, (left) At cut-off frequency of 264MHz; (right) At cut-off frequency of 132MHz

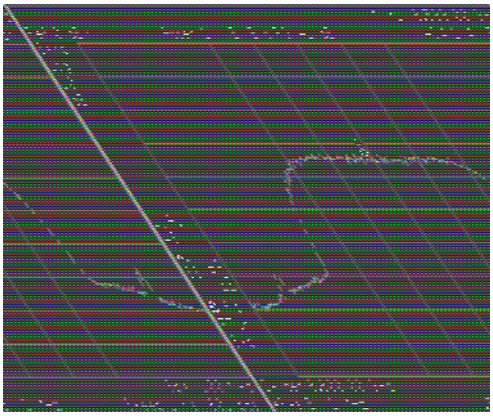

Fig. 22. Spectrum mask of the transmitter with 40MHz QPSK modulation signal

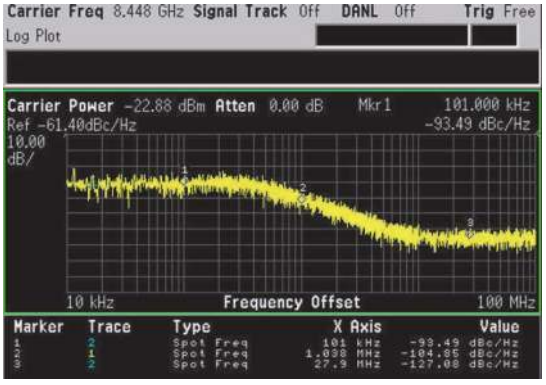

Fig. 23. Measured PLL phase noise and integrated phase noise

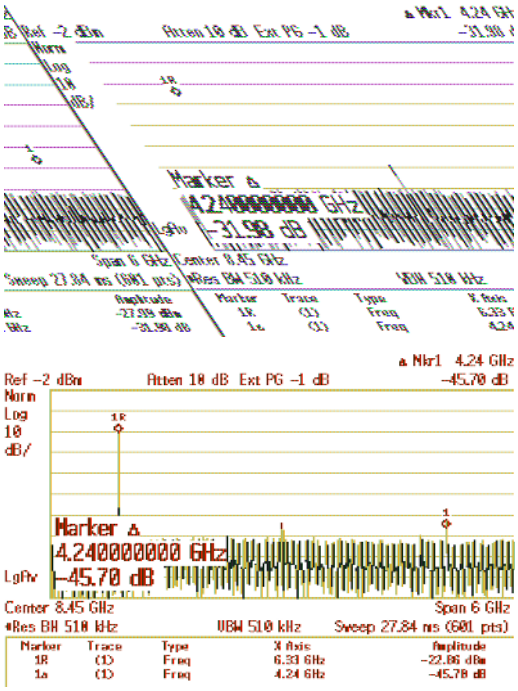

Fig. 24. Output spectrum of 6336 MHz (up) without calibration and (down) with calibration

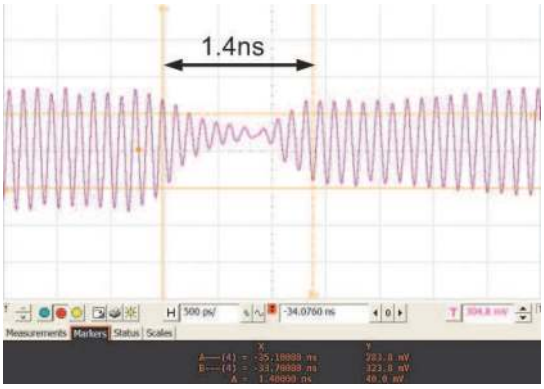

Fig. 25. Measured band switching behaviour

6. Conclusion

A 0.13um CMOS 6-9GHz 9 Band Double-Carrier OFDM Transceiver for Ultra Wideband Application is proposed, which consists of a dual-carrier frequency synthesizer, two 6-9 GHz receiver cores, two 6-9 GHz transmitter cores and the digital control logical circuits, and so on. Only one PLL and two single-sideband mixer have been used in this dual-carrier frequency synthesizer. The VCO in the PLL oscillates at 8448 MHz. All the desired frequencies are generated by mixing the output of the divider chain with that of the VCO. Two carries can be output simultaneously with independent frequency setting and totally 9 carrier frequencies from 6336 MHz to 8712 MHz with a frequency gap of 264 MHz are available. The receiver core is composed of a 6-9 GHz LNA, IQ down-conversion mixer, LPF as well as VGA. The total gain of the receiver chain has been achieved about 80 dB with a minimum NF of 4.5 dB. The transmitter core consists of the IQ LPF, IQ up-conversion mixer and the power driver amplifier. The output IP3 of the transmitter is around +10 dBm and the output 1-dB compression point is about +0 dBm, which reveal high linearity of the transmitter. Besides, the power of LO leakage and sideband signal are less than -35 dB respect to the power of the desired RF signal. The chip size of the DC-OFDM transceiver is 3.6 mm×4.5 mm including the ESD-PADs. The power consumption is around 400mA from 1.2-V supply. The future research will focus on performance optimization, power consumption, and so on.

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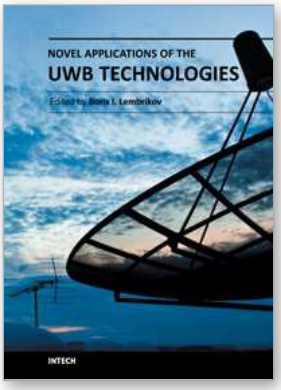

Novel Applications of the UWB Technologies

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Ultra wideband (UWB) communication systems are characterized by high data rates, low cost, multipath immunity, and low power transmission. In 2002, the Federal Communication Commission (FCC) legalized low power UWB emission between 3.1 GHz and 10.6 GHz for indoor communication devices stimulating rapid development of UWB technologies and applications. The proposed book Novel Applications of the UWB Technologies consists of 5 parts and 20 chapters concerning the general problems of UWB communication systems, and novel UWB applications in personal area networks (PANs), medicine, radars and localization systems. The book will be interesting for engineers and researchers occupied in the field of UWB technology.

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