

Integration of 60-GHz Microstrip Antennas with CMOS Chip

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1. Introduction

New emerging wireless systems that operate at millimeter wave frequencies, such as high data rate 60-GHz transceivers for wireless personal area networks (WPAN), use integrated antennas. The small wavelength at 60-GHz enables the antenna to be integrated either in the package or on the chip. However, on-chip integrated antennas for 60-GHz systems, built on a conductive substrate, such as complementary metal-oxide-semiconductor (CMOS) or silicon germanium (SiGe), results in poor radiation efficiency. Therefore, antennas for these systems are commonly implemented on in-package solutions. The integration of antenna-in-package can be achieved by using wire bonding or flip-chip bonding interconnections. Although bonding wires are typically employed to connect passive devices to chip modules since they are robust, inexpensive and tolerant of chip thermal expansion they increase reflections, impedance mismatches and power loss at millimeter wave frequencies. The flip-chip bonding of antenna to chip module can significantly reduce these effects as it uses metallic bumps for device connections which are kept small compared to the length of the bond wire that results in better impedance matching and reduced interconnection losses.

In this chapter two types of antenna integration methods are presented; a microstrip antenna for flip-chip integration and a coplanar waveguide (CPW) fed antenna for wire bonding. The flip-chip integrated antenna compatible with CMOS technology achieves good performance and is mounted on the CMOS chip using standard printed circuit board and flip-chip bonding technology. This approach is compact and inexpensive. The microstrip patch is printed on one substrate layer with a CPW feeding line through the ground patch that permits direct attachment of the patch to the die. The use of low dielectric constant and low dissipation loss substrate material improves antenna radiation efficiency and input impedance bandwidth. The flip-chip approach does have some limitations. The flip-chip interconnection parameters, such as bump height and diameter, vary with the fabrication and cannot be accurately predicted in the design stage. The supporting under fill layer between the antenna and chip influences antenna performance. In this chapter we also investigate the effects of flip-chip interconnection on microstrip antenna performance and explore the relationship of the flip-chip interconnection parameters on bandwidth, radiation efficiency and gain. Our design methodology shows that microstrip antenna bandwidths of 15% can be achieved with careful flip-chip interconnection design and fabrication.

The second integrated antenna described is a coplanar waveguide fed antenna with wire bond interconnections. The use of bonding wires for antenna integration with a semiconductor device suits coplanar antenna structures since the bonding wires can directly connect the coplanar output pads of the device. In our approach, the coplanar bonding wires are modeled as transmission lines. This permits us to use the wire bond interconnections in the CPW-fed antenna design at mm-wave frequencies. This chapter describes the techniques that utilise wire bond interconnection in the CPW-fed patch/slot antenna design as a part of the antenna circuit avoiding the need for tuning capacitors or reconfiguration of the packaging structure. In this method reactance of the bonding wires is accounted for in the design, hence lessens the reduction of antenna matching bandwidth. The described technique permits for bonding process variation to be accounted for in the design stage. The CPW-fed antennas have a 10 dB return loss bandwidth of 10% and a measured gain varies from 6-7.8 dBi across the impedance-matched bandwidth. These results indicate that the CPW-fed slot/patch antenna type and wire bonding technology can be adequately used for integrated 60 GHz transceivers.

The techniques described in this chapter have been used to implement integrated antennas. The use of standard bonding technologies to achieve low cost packaging systems is feasible if the antenna-chip interconnections are properly accounted for in the design process and the successful integration and acceptable performance at mm-wave frequencies can be achieved using both, flip-chip or wire bond antenna integration methods.

2. Microstrip patch antennas

2.1 Patch Antenna on CMOS chip

The previous research verified the use of flip-chip technology for the integration of antenna with a CMOS transceiver at 60-GHz frequency band (Felic & Skafidas, 2008). The antenna and flip-chip interconnection configurations are seen in Fig. 1. It shows a single patch antenna and the flip-chip interconnection between the CMOS die and antenna input pads.

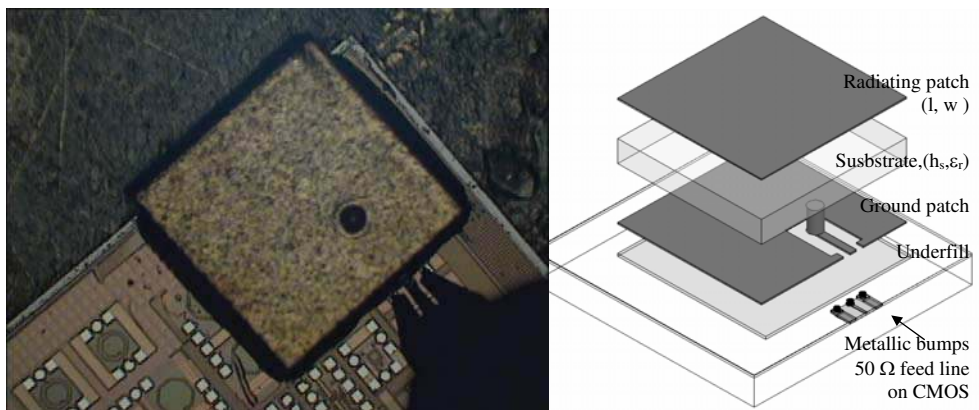


Fig. 2.1. Patch antenna structure on CMOS chip (photograph and geometry of fabricated antenna). (Parameters: $l=1.65\text{mm}$, $w=1.67\text{mm}$, $\epsilon_r=2.2$, $y'=0.435\text{mm}$, $h_s=0.254\text{mm}$)

The shape of the patch is nearly square with the feed location selected along the diagonal starting at the lower right corner of the ground plane. This type of connection allows the antenna to be fabricated by using standard PCB and flip-chip bonding technology. The radiating patch is connected to the input signal by via and coplanar waveguide feeding network in the ground patch. The interconnection between the antenna and microstrip line on CMOS die consists of three gold stud bumps which connect ground and signal conductors. Gold stud bumps are placed on the CMOS die pads through a modification of the "ball bonding" process used in conventional wire bonding. In order to mechanically support the antenna structure the underfill layer is placed in the gap between the antenna and die. Figure 2.2 displays the geometry of the flip-chip antenna transition and the photograph of the fabricated prototype.

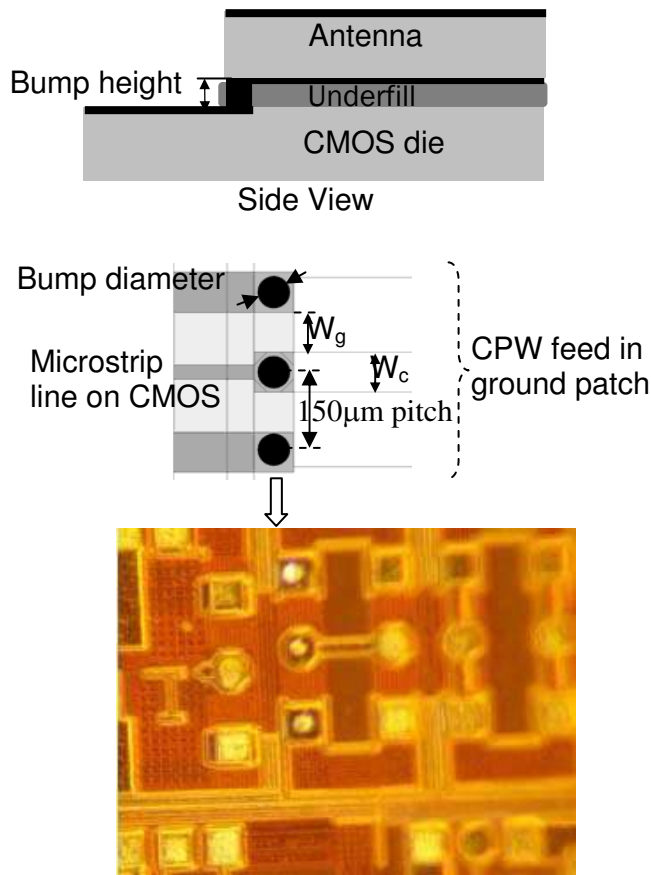


Fig. 2.2. Geometry of flip-chip transition (side and top view of the transition) and photograph of flip-chip gold bumps on CMOS chip. (Parameters: $W_g=W_c=75 \mu\text{m}$)

The optimized design of the antenna includes interconnections. The design value for bump diameter is 60 μm , the permittivity of underfill layer is 4.1 (Epotek, U300) and bump height is 20 μm . However, 20 μm bump height was not achievable in our manufacturing process (stud bump technology) and final fabricated bump height was 40 μm (+/- 5 μm tolerance). The main parameters for this study are the bump height, bump diameter and permittivity of underfill layer. Other parameters such as the bump pitch and parameters of microstrip line on CMOS are predetermined by the chosen technology and required 50- Ω output impedance of the chip design (Felic & Skafidas, 2008). Although the values of the bump pitch can be selected in the early stage of chip-package co-design, in this antenna-chip configuration the minimal bump pitch was limited by the capabilities of PCB manufacturing technology.

2.2 The effects of flip-chip parameters on antenna performance

In particular the effects of flip-chip bump parameter variations on the antenna input impedance bandwidth and gain are examined in (Felic, G. & Skafidas, S. 2009). The wide bandwidth can be achieved with very short bumps and thin underfill layer at the expense of decreased efficiency and gain. Bump diameter variations provided they are within acceptable tolerance don't affect the bandwidth, gain or efficiency. The low permittivity of underfill layer increases gain and efficiency but only slightly reduces the bandwidth. This investigation shows that standard and inexpensive flip-chip bonding process can be used to achieve antenna-die integration provided that careful consideration is given to flip-chip parameters (e.g. bump size and tolerance) during the antenna design stage. By selecting flip-chip bonding, antenna integration is compatible with standard CMOS technology. Moreover, flip chip mounting enables a low loss connection between the coplanar waveguide formed on the ground plane to a microstrip transmission line or other type of connection as may be formed upon a CMOS die upon which the antenna element is flip chip mounted.

2.3 Experimental validation

The input impedance matching was measured on a probe station using a GSG probe. Figure 2.3 shows the simulated and measured magnitude of the reflection coefficient (input impedance matching) of the fabricated antenna with flip-chip interconnection (Fig. 2.1).

In the frequency band from 60 GHz to 69 GHz, measured reflections lower than -10 dB were achieved (15% bandwidth). Simulation results show that when the bump height increases from 20 to 40 μm the -10dB bandwidth decreases by 1.5 GHz. This is due to the increased impedance (reactance) of extended bump length which increases input impedance mismatch. To fully cover the 57-66 GHz band this reactance can be compensated by redesign of the antenna with larger patch size. Figure 2.4 shows the measured gain, simulated gain and efficiency.

The gain was measured at angle of $\theta=0^\circ$ and $\phi=0^\circ$ (Fig. 2.1). The measurement set-up was calibrated using coaxial calibration kit and V-band horn antennas (Balanis, 1997). Then, one port is connected to GSG probe (calibrated at the tips) and test antenna and the other port to the horn antenna. Fabricated antenna achieves gain of 2-4 dBi inside the -10 dB impedance bandwidth at $\theta=0^\circ$. This level of gain is low, however, an array can be formed by a number of these antenna elements to enhance the radiation and compensate the path loss for 60-GHz radio.

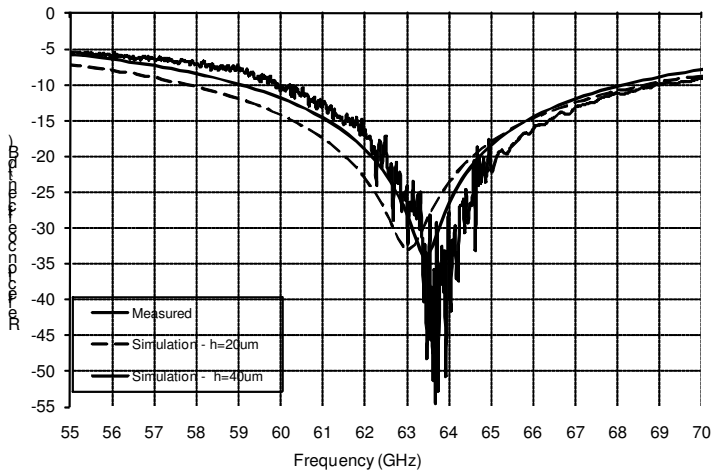


Fig. 2.3. Matching impedance performance of an integrated antenna with flip-chip interconnect. (Simulation parameters: $\epsilon_r=4.1$, bump diameter=60 μm)

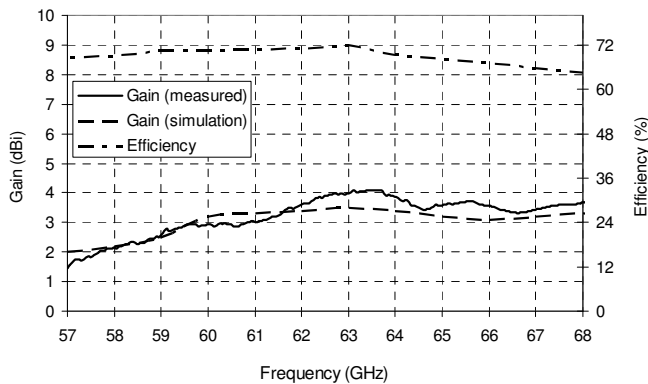


Fig. 2.4. Gain and radiation efficiency of an integrated microstrip antenna with flip-chip interconnect. (Simulation parameters: $h=40 \mu\text{m}$, bump diameter=60 μm)

2.4 Patch Array on CMOS chip

As it can be determined from Fig. 2.4 the realised gain of on-chip mounted antenna is low and an array must be formed to enhance the radiation and compensate the path loss for 60-GHz radio. In order to meet the link budget of a 60GHz system over a range of 10 m using 16QAM modulation (Wicks, B. N., Ta, C. M., Zhang, F. et al., 2009) one requires an antenna gain exceeding 12dBi at both Tx and Rx. There are several ways of achieving such gains and the implications and engineering tradeoffs that come into play when designing the antenna array should be taken into account. Fig. 2.5 shows a possible solution with 2x4 antennas array on a substrate designed for on-chip mounting. The array is built on the three layers of

Taconnic substrate with relative permittivity of 2.2. The patch array is designed to suit the flip-chip integration with CMOS shown in Section 2.1. The antenna elements are patch type and they can be connected to CMOS chip with via connections and metallic bumps as it is shown in Fig. 2.1. The simulated radiation pattern show that the on-chip mounted 2x4 array can achieve maximal gain of 14 dBi.

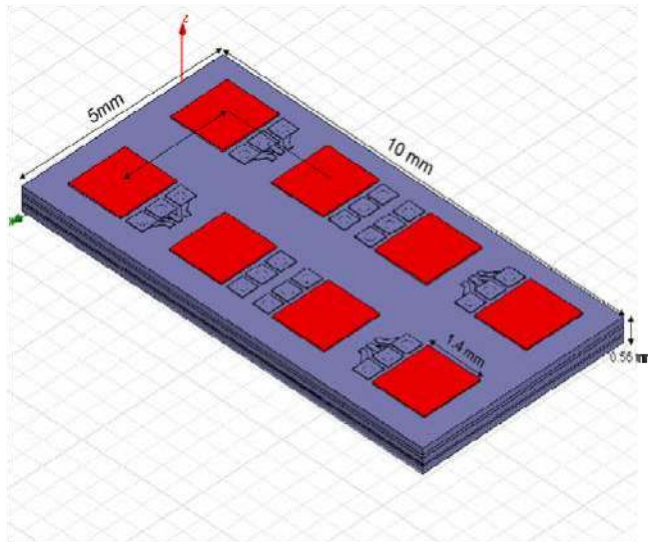


Fig. 2.5. Patch array test structure for CMOS chip mounting. (Overall dimensions: $l=10$ mm, $w=5$ mm, $\epsilon_r=2.2$, $h=0.56$ mm)

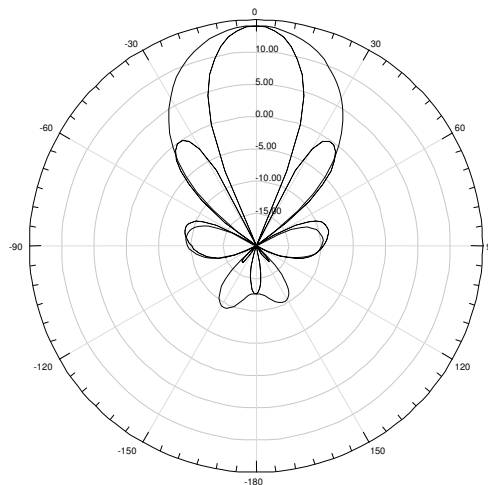


Fig. 2.6. Radiation Patterns, realised gain [dBi] in E-plane (----) and H-plane (—) at 60 GHz.

3. CPW patch antennas

3.1 The use of wire bonding for antenna integration

Bonding wire is typically employed to connect passive devices to chip modules since it is robust, inexpensive, and tolerant of chip thermal expansion. However, this integration approach has undesirable consequences of increasing impedance mismatches and power losses at mm-wave frequencies and the requirement for impedance compensation networks. To improve the performance of wire bond interconnects and enable the use of longer bonding wires the design techniques applied to mm-wave frequencies focus on two main methods; the inclusion of low pass filters on chip (Budka, 2001) and design of specific compensation networks (Karnfelt et al., 2006). The first method requires the co-design of the chip and package, and it is not suitable for connecting a radio chip to the antenna when a DC blocking capacitor is required between them. The second method includes the compensation network (impedance transformer and double stub) on the package that takes a large package area. Recently, a novel bond wire compensation structure was proposed in (Zhang et al., 2009) that uses a compensation capacitor. A series connected capacitor to the antenna tunes the inductance of the wire bond wire to a resonant condition, thus compensating the high inductance of the bond wire at the resonant frequency. This method is specifically suitable for CPW-fed coplanar antenna structures on package. The compensation structure (capacitor) is implemented on package between the wire bond pad and CPW transmission line (signal trace) at the antenna input. Although this does not enlarge the package surface area, it requires an additional dielectric substrate layer for implementation of the compensation capacitor.

The use of bonding wires for antenna integration with a semiconductor device suits coplanar antenna structures since the bonding wires can directly connect the coplanar output pads of the device to the coplanar antenna input. The other interesting aspect of coplanar bonding wires is that they can be thought of as transmission line (Goosen, 1999). This consideration opens the opportunity for exploitation of wire bond interconnection in the CPW-fed antenna design at mm-wave frequencies.

A CPW-fed loop slot antenna for integration with a mm-wave CMOS transceiver chip has been presented (Felic & Skafidas, 2009). A distinguishing feature of this design is that the chip-antenna interconnections are achieved using standard bonding wires. The designed antenna including wire bond interconnections is verified with measurements and as part of an operational 60 GHz wireless transceiver system fabricated on CMOS (Wicks et al., 2009). Although many papers have been published for mm-wave antennas, only (Zhang et al., 2009) and (Felic & Skafidas, 2009) reported the results accomplished using wire bond antenna-chip integration.

This section elaborates on the exploitation of wire bond interconnection in the CPW-fed antenna design to avoid the need for a compensation network, tuning capacitors or reconfiguration of the packaging structure. This technique is based on the transmission line model of the bonding wires and the compensation of its reactance by the antenna design. As the reactance of the bonding wires is compensated by the design, the reduction of antenna matching bandwidth is less significant.

3.2 CPW-fed patch/slot antenna

A number of papers have been published dealing with the parameters that affect the design and matching of these antennas. A brief summary follows.

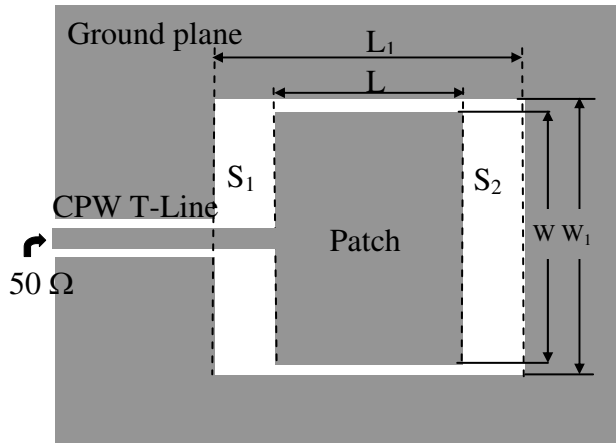


Fig. 3.1. A CPW-fed patch/slot antenna for wire bond integration (Greiser, 1976)

The original coplanar waveguide (stripline) patch/slot antenna structure was first introduced in (Greiser, 1976), Fig. 3.1. This design was based on the concept of an open ended coplanar waveguide resonator which operates in the fundamental mode, when its circumference is approximately one wavelength. However, in (Tong et al., 2004) it is reported that coplanar waveguide antenna structures behave more like microstrip patch antennas with the resonant frequency primarily determined by the patch length (which is approximately equal to half guided wavelength) and not by the circumference of the slot. A parametric study of a similar coplanar waveguide antenna structure is introduced by (Chen, 2003) to achieve wide impedance matching bandwidth. By tuning the spacing between the tuning stub and ground plane and having the length of the tuning stub equal to about half of the slot length, an impedance bandwidth of more than 50% has been achieved. This can be increased by selecting the width of the tuning stub to be about 0.59 to 0.9 times the slot length. A coplanar waveguide slot antenna with wideband feeding mechanism in the form of a radial tuning stub is also presented by (Rao, 2006). The design of this antenna structure is based on the optimal length of the radial stub protrusion which should be in the range of 0.45-0.6 times the slot's width. Further, the impedance matching is achieved by increasing the width of printed stub. In addition, the edge treatment of the stub has an impact on the bandwidth improvement. Transmission line (T-line) models for the design of microstrip patch antennas are studied and used in (Balanis, 1997) and (Watson et al., 1999). In the same way, a transmission line model for CPW-fed patch antennas is used in (Watson, 2001) to design the essential antenna elements: radiating patch, slots in ground plane and input feed line. The radiating patch is represented by a uniform length of transmission line in communicating the energy from the input edge to the distal edge of the patch. The feeding T-line element transfers the energy from the input port (50Ω connector) to the radiating element (patch edge). It also serves as an impedance transformer since it alters the relatively low impedance of the transmission line at the input to the higher impedance at the edge of the patch. The slot region between the antenna input and the edge of the patch and the distal slot region are represented by lumped admittances (capacitance and conductance). Thus for the selected size of ground plane, good input impedance matching can be obtained

by selecting the lengths of the patch and slot that enhance the coupling between the patch and ground plane. Further improvement of impedance matching can be achieved by adjusting the patch width.

3.3 Utilisation of wire bond Interconnection in antenna design

The antenna with wire bond interconnections can be designed without a wire bond compensation network if the wire bond interconnection is understood as a high impedance T-line extension of the antenna structure and is then included in the design. Therefore, the input impedance seen at 50 Ω input (source) is:

$$Z_{in} = Z_0 \frac{Z_A + jZ_0 \tan \beta l}{Z_0 + jZ_A \tan \beta l} \quad (1)$$

where Z_A is the antenna input impedance, Z_0 is the characteristic impedance of the T-line (wire bond interconnection), $\beta = 2\pi/\lambda$, and l is the length of the T-line. The assumption is that the T-line is lossless. As the overall electrical length of the antenna-feed line structure is now increased by $\beta \lambda$, the input impedance resonance moves to lower frequencies. The reflection coefficient at the wire bond antenna junction is:

$$\Gamma_A = \frac{Z_A - Z_0}{Z_A + Z_0} \quad (2)$$

while the overall reflection at 50 Ω source input is:

$$\Gamma = \frac{Z_{in} - 50\Omega}{Z_{in} + 50\Omega} \quad (3)$$

Under the view of conjugate matching the maximum power transfer from 50 Ω source is achieved when $R_{in}=50 \Omega$ and $X_{in}=0$. Therefore, for a fixed wire bond interconnection (Z_0) the reflections defined in (2) and (3) and impedance matching can be improved by adjusting the input impedance Z_{in} and antenna impedance Z_A . These impedances can be adjusted by decreasing the length of the patch or by increasing the length of the slot. Moreover, by properly selecting the length of the patch and the length of the slot, a wide bandwidth operation can be achieved.

The antenna structure without wire bond interconnection shown in Fig. 3.1 is designed for 50 Ω input impedance matching of better than -10 dB from 57 to 66 GHz. The antenna uses a single layer of Rogers RT/Duroid 5880 substrate with relative permittivity equal to 2.24 and dissipation factor equal to 0.004 (at 60 GHz). The thickness of the dielectric layer is 508 μm . The ground plane reflector is placed at the back of the substrate to obtain a uni-directional radiation pattern. The top ground plane dimensions are 3 mm \times 3 mm. The patch of length $L=1$ mm and width $W=1.7$ mm is connected to the CPW feed line. The rectangular radiating slot dimensions, $W_1 \times L_1$ are 1.83 mm \times 1.14 mm. The length of the slot between the input feed line and radiating edge, S_1 is 50 μm . The CPW feed transmission line is designed with strip and gap width of 50 μm , corresponding to a characteristic impedance of $Z_0=72 \Omega$. The CPW strip and gap size of 50 μm matches with the coplanar wire bonds and pads on CMOS die (pitch of 100 μm). The input impedance matching results (HFSS) for the antenna (antenna without wire bond) are shown in Fig. 3.2.

The next step is to model the bonding wires for electromagnetic simulations (HFSS). The bonding wires are wedge/wedge type made of aluminium (Al), the diameter of the wires is $24.5\ \mu\text{m}$ (1mil) and the length of the wire is $450\ \mu\text{m}$. The centre wire-wire spacing, s is $100\ \mu\text{m}$ and substrate-wire gap, h is $30\ \mu\text{m}$. Figure 3.3 shows the approximated geometry of a wedge/wedge bond for electromagnetic simulation.

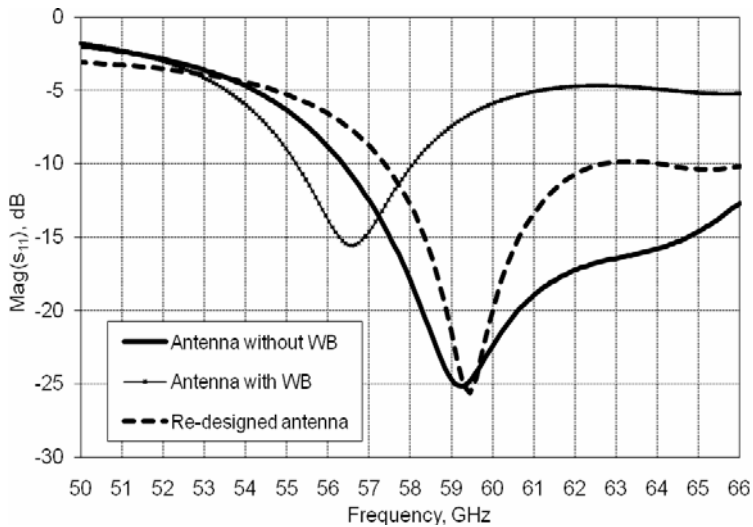


Fig. 3.2. Magnitude of reflection coefficient (simulation) for antenna without wire bond, antenna with wire bond and re-designed antenna.

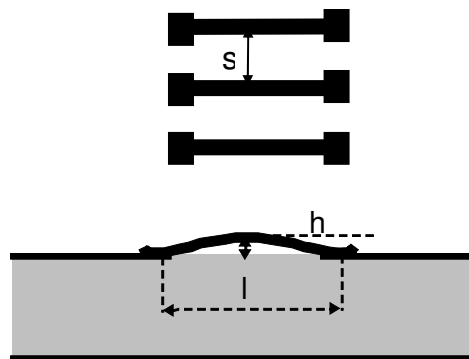


Fig. 3.3. Geometry of wire bond transition implemented for EM simulation (top and side views of the transition), $s=100\ \mu\text{m}$, $h=30\ \mu\text{m}$, $l=450\ \mu\text{m}$.

Although this type of wire bonding, with nearly flat wires (low loop) has lower impedance than ball-wedge type wire bonds which have larger loop height, they can still be seen as an additional high impedance T-line (numerically estimated characteristic impedance is 137Ω). The numerically estimated input impedances of the antenna with the wedge-wedge bonds and the antenna without wire bond are shown in Fig. 3.4.

After adding the wedge type wire bonds, the resonance frequency shifts from 60 GHz to around 56.5 GHz (Fig. 3.4) and the input impedance matching deteriorates.

The final step is to modify the antenna structure. The input impedance matching can be adjusted by decreasing the patch length, L . When the patch length is decreased from 1 mm to 0.9 mm the input impedance of the antenna (including wire bond) decreases and improves the 50Ω impedance matching as is evident in Fig. 3.2 (re-designed antenna). The magnitude of S_{11} is now lower than -10 dB from 57.5-62 GHz, indicating improved matching to the 50Ω source (CMOS chip).

It is also possible to achieve input impedance matching by increasing the length of the slot, L_1 while the patch size and all other parameters are kept constant. This decreases the capacitance of the distal slot, S_2 and shifts the resonance to a higher frequency. Figure 3.5 shows the input impedance matching for the antenna without bond wires and re-designed antenna ($L_1=1.2$ mm).

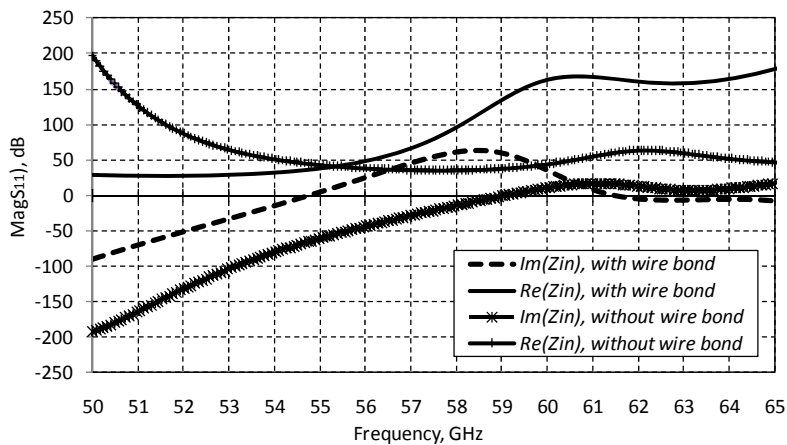


Fig. 3.4. Real and imaginary components of input impedance (antenna with and without wire bond).

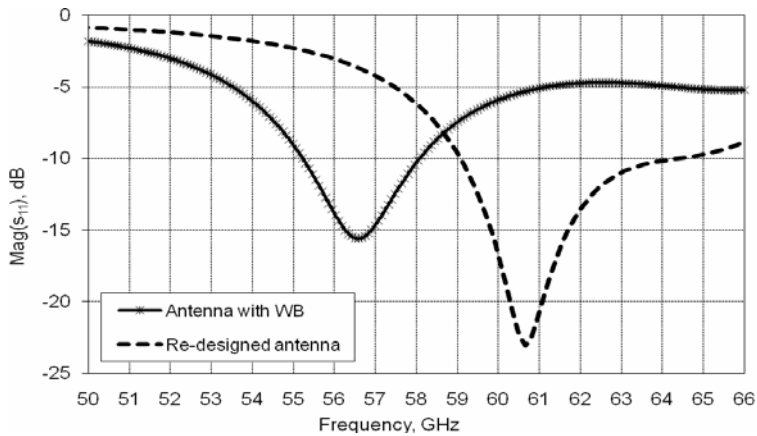


Fig. 3.5. Reflection coefficient for the antenna with wire bond and re-designed antenna.

3.5 Experimental validation

To validate the proposed antenna design technique by measurements the antenna including wire bond interconnections with an attached CPW line is fabricated (Fig. 3.6). The measurements were conducted on a probe station using coplanar microprobes (200 μm pitch). Figure 3.7 shows the simulated and measured input impedance matching. The simulation results are obtained for the prototype antenna and for the integrated antenna. In the frequency band from 57.3 GHz to 65 GHz, measured return losses lower than -10 dB were achieved (reflection coefficient S_{11} lower than -10dB). The simulation results are obtained for

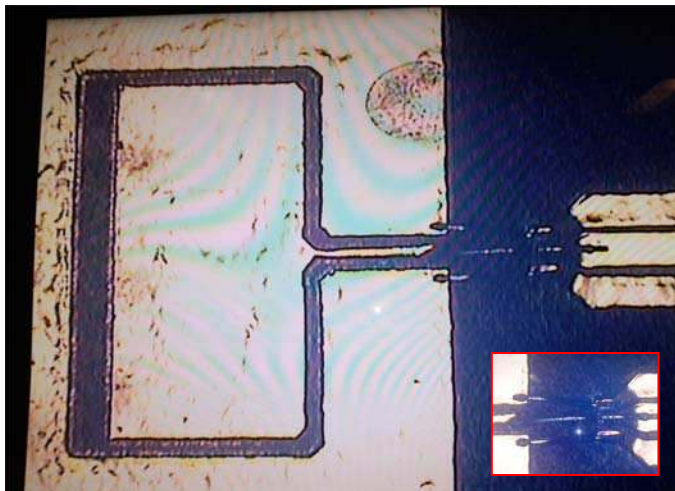


Fig. 3.6. Prototype of the antenna including wire bond interconnections.

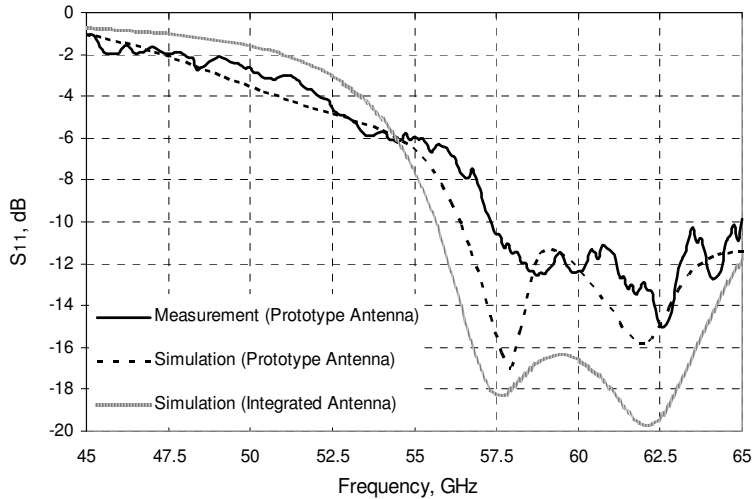


Fig. 3.7. The measured and simulated magnitude of reflection coefficient for the re-designed antenna (wire bond with $s=90 \mu\text{m}$, $l=450 \mu\text{m}$, $h=30 \mu\text{m}$).

the parameters of the fabricated sample ($s=100 \mu\text{m}$ and $l=450 \mu\text{m}$). The discrepancy between the measurement and predicted results is most likely due to the variation of fabricated bond wire-wire spacing which is not uniform over entire length and less than $100 \mu\text{m}$ at the bonding point at CPW line.

The gain measurement set-up was calibrated using a V-band coaxial calibration kit and two identical WR-15 V-band horn antennas. The gain measurement followed the procedure described in (Balanis, 1997). The measured maximum antenna gain varies between 6-7.5 dBi within the -10 dB impedance matching bandwidth (Fig. 3.8). The estimated efficiency of the antenna at 60 GHz is 91%.



Fig. 3.8. Measured and simulated peak gain versus frequency.

3.5 Integrated antenna

Figure 3.9 shows the antenna integrated with 60-GHz direct-conversion transceiver on 130-nm CMOS. The 130-nm CMOS transceiver demonstrates very high level of integration incorporating transmitter, receiver and digital control interface on a single silicon die (Wicks, B. Et al., 2009). The successful implementation of this transceiver is an important step to move the mm-wave circuits onto the low cost CMOS chip.

As it is illustrated in Fig. 3.9, the antenna CPW input is connected to the coplanar pads on CMOS die with wedge-wedge type wire bonding. To further compensate for the inductive component of the wire bond interconnection, in the integrated configuration, an additional matching stub which is printed on the substrate under the wire bond structure is introduced and directly connected to the antenna patch. The printed stub serves to add distributed capacitance, with respect to the ground, to cancel the distributed inductance of the signal bond wires. The dimensions of the rectangular stub ($230\mu\text{m} \times 80\mu\text{m}$) were determined with HFSS simulations. The bonding wires are made of gold (Au) and the diameter of the wires is $24.5\mu\text{m}$ (1mil). The pitch of the coplanar wires varies from $100\mu\text{m}$ to $125\mu\text{m}$.

The CPW-fed receiving and transmitting antennas are directly connected to the coplanar outputs of the CMOS transceiver device by using wedge-wedge type wire bonding. Additional set of wire bonds connect the ground pads on CMOS with top antenna ground plane.

The above results demonstrate the effectiveness of a design approach that understands the wire bond interconnections as extended antenna feed lines. The antenna for wire bond packaging can be designed without a wire bond compensation network. Furthermore, this work confirms the feasibility of low cost standard wire bonding technology at mm-wave frequencies, provided that the wire bonding interconnections are appropriately exploited in the design process. It also offers an easy and convenient integration for planar components on the top of the substrate.

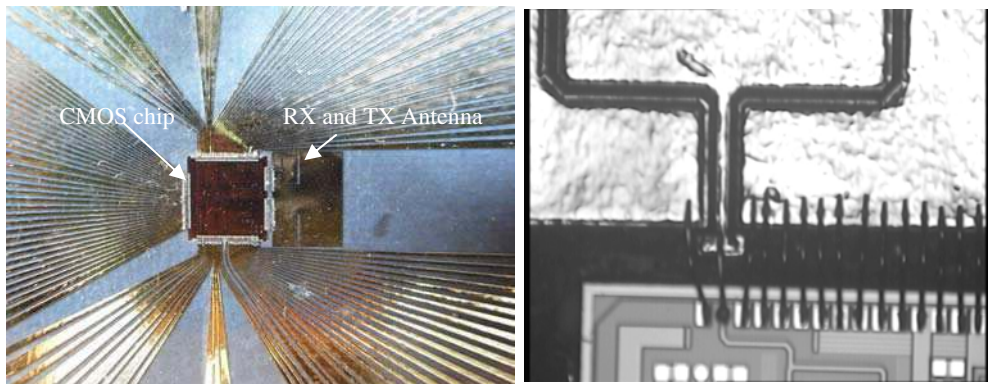


Fig. 3.9. Micrograph of the antenna integrated with CMOS transceiver on the PCB test board.

4. Conclusion

The techniques described in this chapter have been used to integrate antennas with CMOS chip at mm-wave frequencies. The use of standard bonding technologies to achieve low cost packaging systems is feasible if the antenna-chip interconnections are properly accounted for in the design process and the successful integration and acceptable performance at mm-wave frequencies can be achieved using both, flip-chip or wire bond antenna integration methods. At mm-wave frequencies interconnections are seen as integral part of antenna design and the antenna for wire bond packaging can be designed without an additional compensation network. Although the wire bonds are robust, inexpensive, and tolerant of chip thermal expansion this integration approach requires the antenna feed (CPW-fed) located on the top of substrate and particular on-side connection to the CMOS chip. Furthermore, a low cost standard flip-chip technology for antenna integration with CMOS chip is more flexible since both, the coplanar and microstrip antenna feeds are available with flip-chip interconnections.

5. References

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In the last 40 years, the microstrip antenna has been developed for many communication systems such as radars, sensors, wireless, satellite, broadcasting, ultra-wideband, radio frequency identifications (RFIDs), reader devices etc. The progress in modern wireless communication systems has dramatically increased the demand for microstrip antennas. In this book some recent advances in microstrip antennas are presented.

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