Chapter

Silicon-Based Micromachining Process for Flexible Electronics

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Abstract

In this chapter, we introduce silicon-based micromachining process and devices for flexible electronics application. Silicon-based flexible electronics have the unique advantage over other polymer-based process that leverage the traditional standard CMOS process and can be integrated with scalable IC technology. While integrating with CMOS process, special considerations must be taken into account, such as release process, transfer process, and process integration, in order to produce silicon-based flexible electronics. Several efforts and process developments will be illustrated in this chapter with the highlights of imager and wearable electronics application.

Keywords: silicon-based flexible electronics, silicon-on-insulator (SOI), deep reactive-ion etching (DRIE), release process, chemical mechanical polishing (CMP), atomic layer deposition (ALD), complementary metal-oxide semiconductor (CMOS), through-silicon via (TSV), frontside-release process, backside-release process

1. Introduction

Over the past decade, an enthusiastic pursuit for flexible electronics, employing both organic and inorganic semiconductor materials, with continuously improved performance has been observed [1]. The material like polymer, carbon nanotubes (CNTs), and silicon (Si) membrane are popular candidates for flexible electronics. Compared with other materials, monocrystalline Si nanomembrane released from silicon-on-insulator (SOI) emerges as one of the best choices due to its high carrier mobility, commercial availability at relatively lower cost, and mature fabrication techniques [2]. Recently, nanostructured silicon has been widely used to produce flexible electronic devices like flexible solar cells, thermal electricity, and piezoelectric generators.

Functional part of flexible electronics based on silicon can be fabricated in a standard complementary metal-oxide semiconductor (CMOS) technology. A standard CMOS technology includes photolithography, etch, deposition, and doping. Moreover, frontside- and backside-release process, transfer process, and bonding process for flexible substrate are developed to generate flexible silicon membrane with functional part. For frontside-release process, deep reactive-ion etching (DRIE), buffered oxide etcher (BOE), or xenon difluoride (XeF_2) etching are used to release membrane structures, while for backside-release process, lapping, chemical mechanical polishing (CMP), or XeF_2 etching are employed to thin the Si substrate. After fabricating thin Si membranes with functional devices, special transfer process is up required to stick released devices on a flexible substrate like PDMS or Kapton® tape. After the release process, the released Si membrane is transferred and bonded to a flexible substrate (**Figure 1**).

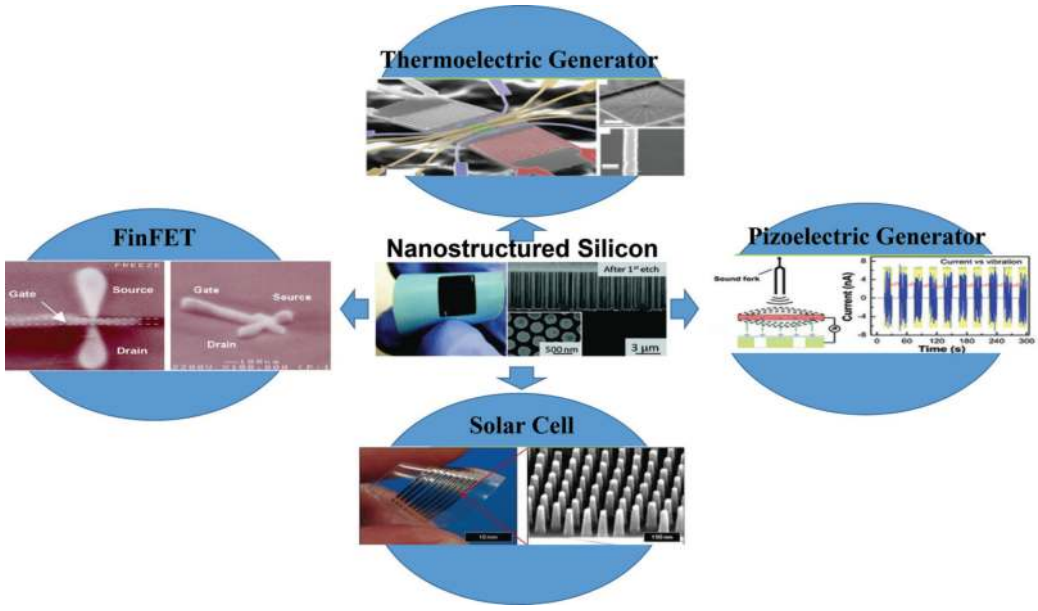

Figure 1.
Schematic diagram of Si-based nanostructures that are served as flexible thermoelectric generator, solar cells, ICs, and piezoelectric generators. As shown in the middle, Si nanowire array on plastic substrate and its cross section under scanning electron microscopy (SEM) are flexible. Images at the bottom: Reproduced with permission [3]. Copyright 2012, American Chemical Society. Images in the middle: Reproduced with permission [4]. Copyright 2011, American Chemical Society. Images in the middle right: Reproduced with permission [5]. Copyright 2011, American Chemical Society. Images in the middle left: Reproduced with permission [6]. Copyright 2011, American Chemical Society. Images at the top: Reproduced with permission [7]. Copyright 2008, nature publishing group [8].

2. Silicon-based micromachining process

Many researchers have demonstrated flexible electronics based on polymers [9, 10] and CNT [11, 12]; however, the micromachining process with those materials is largely limited by the process temperature and compatible chemicals. Moreover, the devices are typically not scalable or almost impossible to integrate with current advanced IC technology. Compared to polymers and CNT, Si-based flexible electronics can employ the matured CMOS fabrication techniques such as photolithography, atomic layer deposition (ALD), physical vapor deposition (PVD), chemical vapor deposition (CVD), Hydrofluoric Acid (HF) etching, reactive-ion etching (RIE), etc. However, in order to produce flexible electronics using traditional Si-based COMS process, development of release process, transfer process, and bonding process are essential for the production of flexible thin silicon membrane. To realize flexibility the oft used processes are DRIE, XeF_2 dry etching, transfer through polymer stamp, process for bonding to flexible substrate, etc. On the whole, the fabrication of silicon-based flexible electronics consists of two major steps: the fabrication of functional part like photodiode, metal-oxide semiconductor field-effect transistor (MOSFET), fin field-effect transistor (FinFET), ferroelectric RAM (FeRAM), etc. and the thinning of device to realize the flexibility. In this chapter, micromachining processes are introduced and described.

2.1 Traditional silicon CMOS process

CMOS process is a standard process used to produce integrated circuits (ICs) and form electronic circuits and system in large scale. CMOS process involves various basic fabrication processes such as wafer manufacturing, oxidation, photolithography, doping, deposition, etching, and CMP.

2.1.1 Wafer manufacturing

Silicon wafers are produced from raw material sand by purifying and crystallizing. The purified silicon is held in molten state at about 1500°C, and after dipping a seed crystal into the melt, the silicon ingot can be produced by gradually extracting the rod. In addition, the silicon can be lightly doped by inserting doping material into the crucible. The fabricated silicon material is used to produce the CMOS device such as MOSFET and FinFET. **Figure 2a** shows the fabricated traditional bulk Si wafer. Nowadays the most advanced transistors are FinFET or fully depleted silicon-on-insulator (FD-SOI) planar transistor technology that is developed at the scale smaller than 25 nm. In the fabrication of FD-SOI transistor, instead of the traditional bulk Silicon wafer, the new more expensive material called SOI wafer is employed. The SOI wafer is fabricated by either separation by implantation of oxygen (SIMOX) process or Smart-Cut process [13]. **Figure 2b** shows SOI wafer for FD-SOI transistor. The thickness of the silicon film is in the ranges from 10 nm to 30 nm; while the standard thickness of BOX is approximately 145 nm and the thickness of ultra thin BOX ranges from 10 nm to 30 nm [14].

2.1.2 Oxidation

In the CMOS fabrication, silicon dioxide layer is used as an insulating material between different conducting layers or acts as a mask or protective layer against diffusion and high-energy ion implantation. The oxidation is performed by a chemical reaction between oxygen (dry oxidation) or water vapor (wet oxidation), and the silicon slice surface is heated in a high-temperature furnace at about 1000°C [15]. Dry oxidation is often used to produce thin and robust oxide layers, while wet oxidation is used to produce thicker and slightly porous layers.

2.1.3 Photolithography

With the help of mask, the photolithography is employed to create patterned layers of different materials on the silicon wafer. Photolithography involves several steps. At first, a photosensitive emulsion (photoresist) film is coated on wafer surface using spin coat. Following that, the wafer is exposed to a pattern of intense light with the help of mask. For positive photoresist (PR), the exposed regions are soluble in the developer, while for negative photoresist, the unexposed regions are soluble in the developer. Tetramethylammonium hydroxide (TMAH) is a widely used developer to remove unwanted photoresist regions. After development, the etching is performed to remove the unwanted regions that are not protected by photoresist. In projection systems, the resolution is limited by the wavelength of the light and the ability of the reduction lens system to capture enough diffraction orders from the illuminated

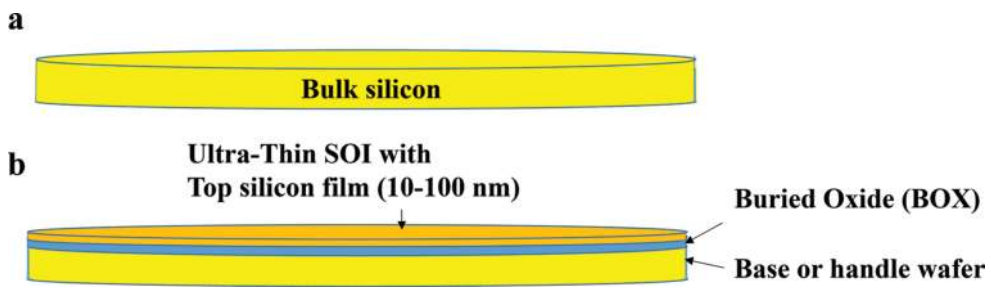

Figure 2.
(a) Traditional bulk silicon wafer. (b) FD-SOI starting wafer.

mask. Nowadays, the most advanced CMOS photolithography is at the scale of about 7 nm, but for flexible electronics photolithography at the scale of about 1 μm is enough for most application such as imager, temperature sensor, and humidity sensor.

2.1.4 Doping

Doping is used to produce electronic components such as diode and various transistors. After masking some area of the silicon surface, doping can be done in exposed regions. Doping can be performed by either diffusion method or ion implantation. There are two basic steps for diffusion method: predeposition and drive-in. In the predeposition step, the wafer is heated in a furnace to a certain temperature (about 1000°C), and carrier gas such as nitrogen and argon with the desired dopant such as phosphine PH_3 or diborane B_2H_6 flow to the silicon wafer. The diffusion of dopant atoms takes place onto the surface of the silicon, and in this step we can control the dose of dopant atoms. In the drive-in step, the wafer is heated in an inert atmosphere for few hours to distribute the atoms more uniformly and to a higher depth [15]. For ion implantation method, charged dopants (ions) are accelerated in an electric field and penetrated into the wafer. The penetration depth can be precisely controlled by reducing or increasing the voltage that needed to accelerate the ions. Following ion implantation, a drive-in step is also performed to achieve uniform distribution of the ions and increase the depth of penetration. **Figure 3** shows two phosphorous doping processes for SOI wafer, in which secondary ion mass spectrometry (SIMS) was used to analyze the doping profiles under two implantation conditions: one has energy/dose of 12 keV/1 × 10^{16} cm^{-3}, and the other has 150 keV/4 × 10^{15} cm^{-3} [1].

2.1.5 Deposition

For MOS Fabrication, various deposition methods are used to form conducting insulating and passivation layers with a variety of materials. There are three

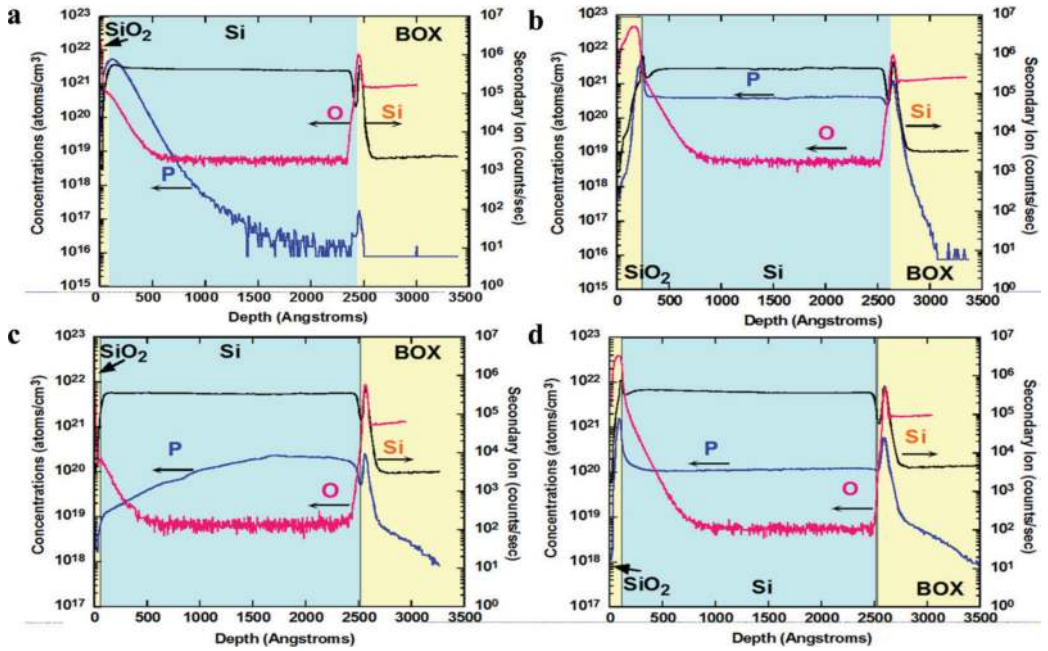

Figure 3.
SIMS results of phosphorous doping profiles of two implantation conditions: 12 keV/1 × 10^{16} cm^{-3} (a) before and (b) after annealing; 150 keV/4 × 10^{15} cm^{-3} (c) before and (d) after annealing. Reproduced with permission [1]. Copyright 2012, IOP.

main deposition processes: PVD, CVD, and ALD. CVD is widely used to deposit conducting layers such as polysilicon and insulating layers such as SiO_2 and Si_3N_4. ALD is used to deposit gate dielectrics with high-k material such as hafnium dioxide HfO_2 and tantalum pentoxide Ta_2O_5 that are necessary for FET at scale smaller than 25 nm. PVD is an established method of depositing metal contacts, barriers, and interconnects used in ICs [16]. In the advanced CMOS, a 3D stack chip structure is used to further improve the integration by using solder flip chip and through-silicon vias (TSVs). For the fabrication of TSVs, the depositions of passivation layer such as silicon nitride (SiN) and metal layer such as copper (Cu) are necessary. But some deposition processes are not more suitable for TSVs with aspect ratios more than 10:1; the capability of several deposition processes to coat the sidewalls of TSVs is limited as shown in **Figure 4**. Compared with ALD, the deposition coverage of CVD decreases below 20% for aspect ratios exceeding 10:1, and for aspect ratios larger than 2.5:1 the deposition coverage of PVD is already less than 20%. Moreover, molecular vapor deposition (MVD) is an alternative deposition process that is suitable for TSVs with aspect ratios larger than 10:1 [17].

2.1.6 Etching

Etching process is used to remove unwanted material and to create desired pattern. There are two types of etching methods: wet etching and dry etching. For wet etching, the wafer is immersed in a suitable etching solution, which can remove the exposed material leaving the material beneath the protective layer intact. For example, potassium hydroxide (KOH) is used to etch silicon, while hydrofluoric acid (HF) is used to etch SiO_2. In addition, the etching mask should not dissolve or at least be etched much slower in the etchant. For example, SiO_2 and Si_3N_4 can serve as mask for Si etching in KOH, while Si_3N_4 and metal are usually used as SiO_2 wet etching mask. Dry etching, usually called plasma etching or reactive-ion etching (RIE), is used to remove the materials by chemical reactions (using chemical reactive gases or plasma) and by purely physical methods (e.g., sputtering and ion beam-induced etching) or with a combination of both chemical reaction and physical bombardment (e.g., RIE). For instance, SF_6 and CF_4 can be utilized to etch silicon anisotropically, while XeF_2 etches silicon isotropically with pure chemical reaction. Depending on the selectivity and how much materials need to be etched, PR, SiO_2, or metal can be used as the mask for silicon etching [19, 20].

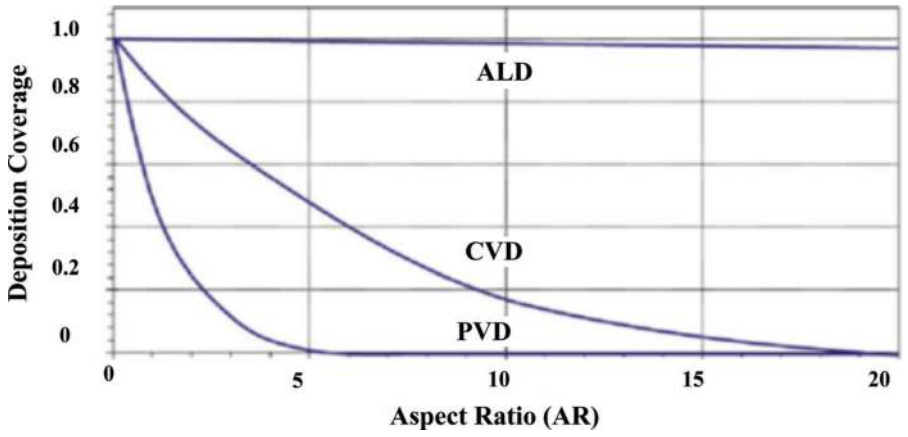

Figure 4.
Schematic graph of deposition coverage in comparison of PVD, CVD, and ALD deposition processes. Reproduced with permission [18]. Copyright 2016, springer international publishing Switzerland.

Etching can be isotropic or anisotropic and therefore can form different etching profiles. Isotropic etching has the same etch rate in all directions and, anisotropic etching has different etch rates in the lateral and vertical directions. For example, silicon can be etched anisotropically by using CF_4 or SF_6 and can be etched isotropically using XeF_2 or $HF:HNO_3:H_2O$.

2.1.7 Chemical mechanical polishing (CMP)

CMP process is a combination of mechanical and chemical actions, and it has been widely used to polish and thin silicon substrate. A CMP process could be significantly influenced by many factors such as abrasives, pH, and polishing temperature [21]. The schema of CMP tool and process to polish wafer are shown in **Figure 5** [22]. A wafer is firstly held by the polishing head using a vacuum and then the polishing head starts to rotate, resulting in the rotation of held wafer on the polishing pad [22]. The slurry used in the CMP process is dispensed through a slurry arm with the help of polishing pad conditioner, and the polishing pad surface is refreshed for each polishing process so that global planarization and polishing can be achieved [22]. During CMP process, the wafer is polished through abrasive and chemistry, and the complicate interaction between pad asperity, slurry, and wafer surface is described in **Figure 5** in a microscale observation [22]. For CMP process, readers are directed to Refs. [21, 22] for more details.

2.2 Frontside-release process for flexible silicon membrane

Frontside-release process utilizes SOI wafers and, in general, consists of active device fabrication, frontside-release hole, or structure patterning, releasing protection coating and release etching. Two release etching strategies are usually employed: one way is to remove BOX layer in SOI and fully release the device layer. RIE or DRIE is used to etch the Si device layer depending on the required etching depth and expose the BOX layer to HF etchant for releasing.

The other approach is to remove bulk silicon carrier in SOI and fully release the structures consisting of both device and BOX layers. Therefore, Si isotropically etching is required for releasing, and XeF_2 is mostly employed. Pure SF_6 plasma can also etch silicon isotropically.

Different from CMOS process, the thickness of FD-SOI device layer for MOSFET is approximately in the order of 100 nm, and the thickness of SOI device layer for flexible electronics can be as thick as 10 μm in many applications. Therefore DRIE is essential to form high aspect ratio trenches for exposure of BOX or silicon substrate to etchant. Following DRIE, the release can be achieved by either removing BOX or undercutting silicon substrate from frontside. HF etchant is used to remove BOX

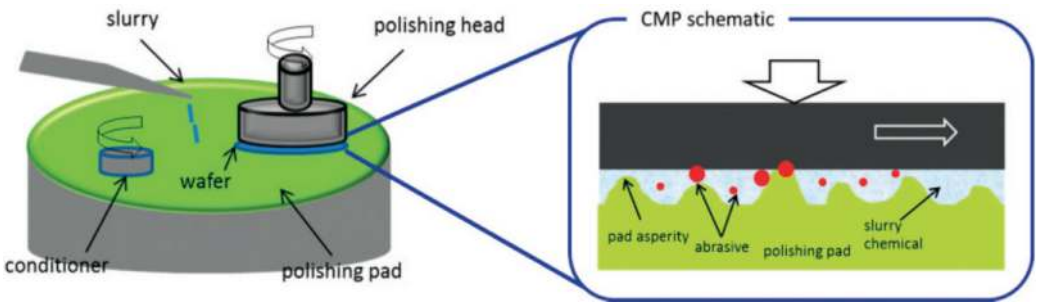

Figure 5.
The schema of conventional CMP process [22]. Copyright (2018) with permission from IntechOpen.

and XeF_2 is used to undercut silicon. Moreover, for release by undercutting silicon below BOX layer, a protective layer is necessary to protect other silicon parts from etching. Deposition of the protective layer onto the sidewall of trenches must be performed. Compared to PVD and CVD, ALD method can deposit high conformal and continuous protective layer inside the trench. The protective layer can be made of silicon oxide or alumina. In the following sections, we first introduce DRIE and XeF_2 RIE processes, and then we will describe how these two technique are utilized in the frontside-release processes.

2.2.1 Deep reactive-ion etching and XeF_2 RIE

2.2.1.1 Deep reactive-ion etching

DRIE is an extension of the traditional RIE process and is a highly anisotropic etch process. Different from traditional RIE, DRIE can be used to create vertical (90°) etch profiles, deep penetration, and holes with high aspect ratios. So far it has been used to fabricate capacitors for deep trench DRAM, TSVs, and microphotonic structures. With the help of novel thermal budget and by-product redeposition management, DRIE can pattern more than 5 μm silicon or even thru the wafer with cycling of two processes:

1. Plasma-induced deposition of a polymeric layer as passivation layer using C_4F_8 as working gas [18].

2. Anisotropic removal of passivation layer on the bottom followed by an isotropic Si chemical etch, and SF_6 is usually employed as working gas for etching of Si [18].

The DRIE process is shown in **Figure 6** and consists of six steps. At first, the polymeric passivation layer is coated overall to protect the sidewalls from chemical attack in the etching step (**Figure 6a**). Following that is the etching step; first the passivation layer on vertical surface (trench bottom) is removed through electrical field-accelerated ions (**Figure 6b**), and after the removal of passivation layer on trench bottom, the trench bottom is isotropically etched (**Figure 6c**). This isotropic etching usually lasts a few seconds, and the working gas mostly is a fluorine-based gas such as SF_6. Followed by the etching step, a deposition step is performed for a few seconds to coat the overall polymeric passivation layer (**Figure 6d**), which is similar to the first step. Then the etching step is repeated (**Figure 6e**), which is similar to step 2 and step 3 [18]. The removal of passivation layer on vertical surfaces is much faster than on horizontal, since the ions are accelerated in vertical direction. After the removal of passivation layer on the trench bottom, the further etchants start etching the trench bottom, and simultaneously polymeric passivation layer of the sidewall slows the lateral etch rate [18]. To achieve the desired depth of TSVs, these etching and deposition steps are repeated several times (**Figure 6f**) [18]. The DRIE process involves six steps, and the performance of each step is controlled by a significant number of parameters such as gas flows, the power of the inductively coupled plasma or the platen source, time, etc. [18].

There are quite a few parameters that can significantly influence the DRIE process profile, such as gas flows, the power of the inductively coupled plasma or the platen source, time, etc. For 1 μm line and hole, scallops were deeper in the top (~40 nm) and none in the middle (<5 nm) and minimal (~20 nm) in the bottom for both holes and lines for the optimized recipe [23]. **Figure 7** shows how the process parameters influence the DRIE process properties. Scallops in top and in the bottom

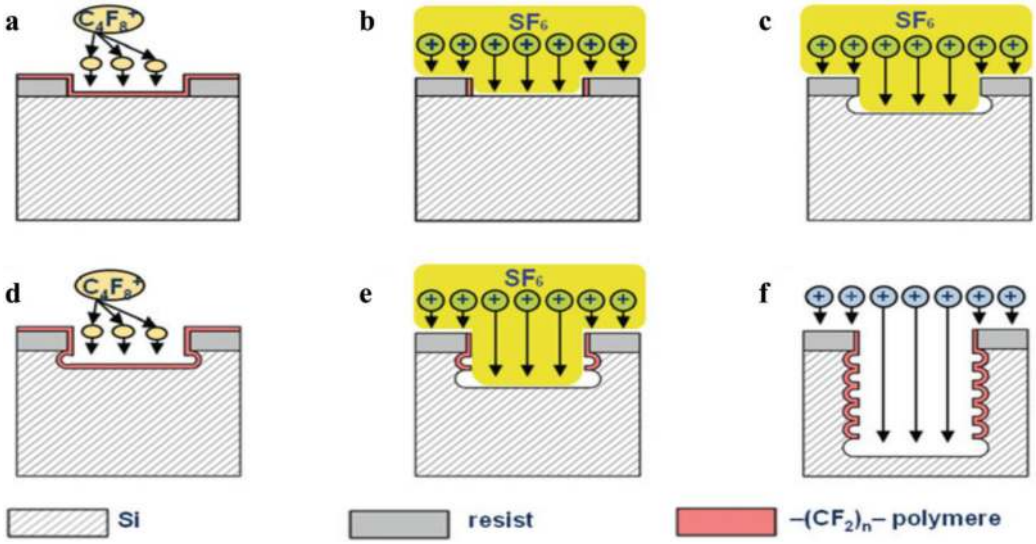

Figure 6.
Bosch process scheme. (a) Deposition of a conformal C_4F_8 passivation layer, (b) directed removal of the passivation layer by ions, (c) isotropic etching with SF6, (d) deposition of a conformal C_4F_8 passivation layer, (e) passivation removal and isotropic etching, and (f) alternating steps (b)–(e). reproduced with permission [18]. Copyright 2016, springer international publishing Switzerland.

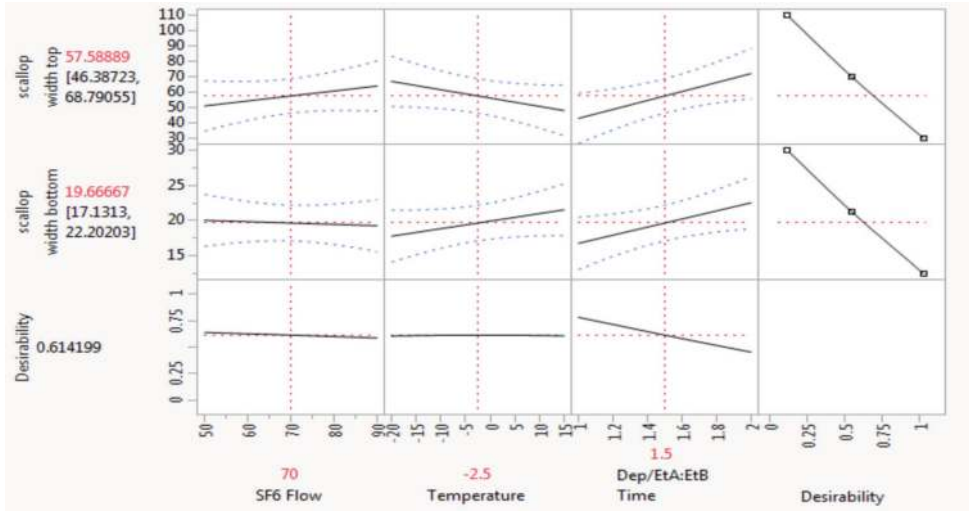

Figure 7.
DRIE profile scalloping prediction and desired profiles [23].

showed that a lower etch time results in less scalloping. Those etches are isotropic, so lowering the time lowers the etch distance in all directions. It also appears to be a weak but somewhat significant evidence for dependence on temperature. However, these trends are in the opposite directions, so there is no optimal temperature for the minimal scalloping. SF_6 flow shows no measured statistical significance to the scalloping or undercut.

2.2.1.2 XeF_2 RIE

Xenon difluoride (XeF_2), bromine trifluoride (BrF_3), chlorine trifluoride (ClF_3), and fluorine (F_2) are widely used to etch silicon [24]. Compared to other silicon etchants, XeF_2 has unique advantages like gas-phase isotropic etching, high selectivity for silicon, and ease of operation [24]. At room temperature and atmospheric

pressure, XeF_2 is white and in solid state [24]. However, when XeF_2 is at a pressure smaller than 4 torr, the XeF_2 solid will transform into a gas state [24]. Since the gas etching process is simple to operate, XeF_2 etching process is widely performed by using the pulse etching system [24]. The XeF_2 pulse etching process can be controlled by process parameters such as XeF_2 pressure, etching time for a single cycle, and the number of etch cycles [24]. **Figure 8** shows the micromachining mechanism of XeF_2 etching.

2.2.2 Release through removal of BOX

In this release process, the SOI BOX layer is patterned and exposed using RIE or DRIE, followed by HF wet etching and critical point dry to fully release the structures above the BOX layer.

This release process involves three steps. In the first step, trenches are formed through RIE or DRIE to expose BOX (**Figure 9b**). When the silicon layer is thicker than 10 μm and aspect ratio is more than 10:1, DRIE is essential to expose BOX. For thin SOI, the exposure can also be performed by RIE. The second step is the deposition of a protective layer (**Figure 9b**). The Protective layer can protect other parts of silicon oxide from damage by etching, and the materials such as Si_3N_4 and PR can be used as a protective layer in this process. In the last step, the wafer is immersed in a HF-contained solution, which removes the exposed BOX. **Figure 9c** shows that the BOX is already partially removed, and **Figure 9d** shows that the BOX is fully removed through HF-contained solution. After the release process, the wafer will be transferred to a flexible substrate, and a bonding process will be performed to bond wafer to flexible substrate.

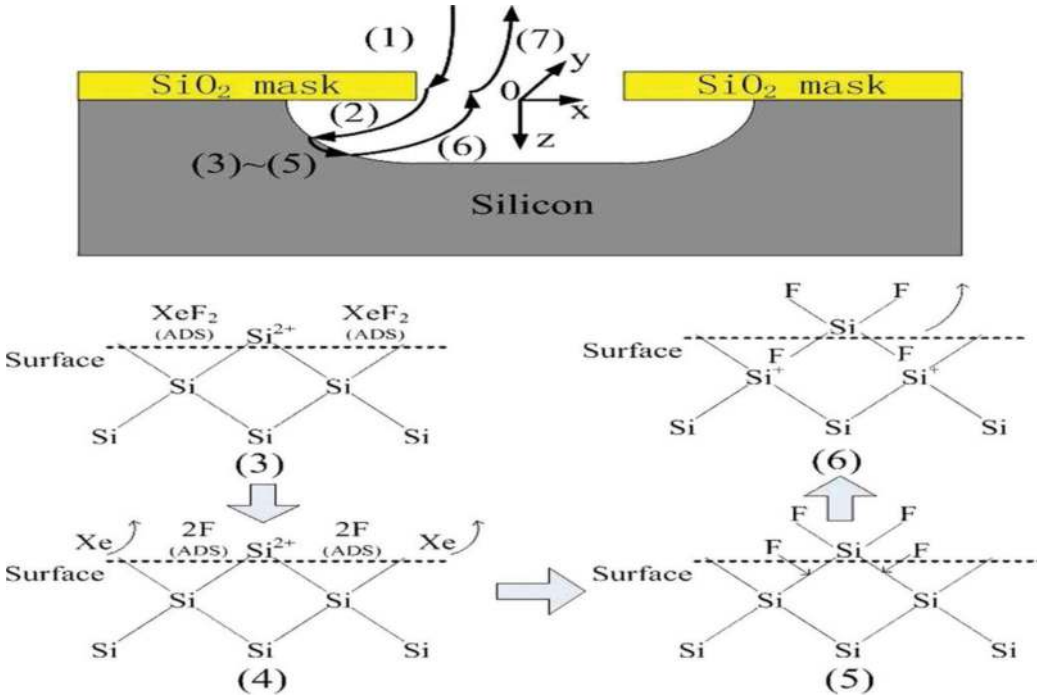

Figure 8.
Schema of interaction between XeF_2 and Si by using XeF_2 RIE to etch Si. (1) XeF_2 gas diffused from the reactor to the external surface of the etching window. (2) XeF_2 gas diffused from the etching window through the etched Si cavity to the silicon surface. (3) adsorption of XeF_2 at the silicon surface. (4) dissociation of XeF_2 molecule into fluorine atoms (F) and xenon (Xe) gas. (5) formation of Si-F bond and adsorption of SiF_4 at the silicon surface. (6) SiF_4 at the external surface is desorpted from Si surface. (7) the products are transferred from the wafer surface to the reactor. Reproduced with permission [24]. Copyright 2012, IEEE.

Zhou et al. utilized this release process to release their strained nanomembrane. In their paper for fast flexible electronics with strained silicon nanomembrane, the strips are released in a 4:1 diluted HF (49% HF) solution in which the BOX layer is selectively etched away [25]. **Figure 10** shows the process for release of silicon nanomembrane from Si handling substrate.

2.2.3 Release through undercut of silicon

This release process is achieved by undercutting silicon substrate under the BOX through XeF_2 isotropic etching. DRIE is usually used to pattern top silicon device layer followed by protective coating and removal of BOX layer in RIE.

This process involves four steps, and we use **Figure 11** to describe this release process. At first, an oxide film such as PECVD SiO_2 is deposited atop the device as an etching buffer layer (**Figure 11a**). Following that, with the help of a PR mask, the exposed oxide layers are removed through RIE, and then the exposure of silicon

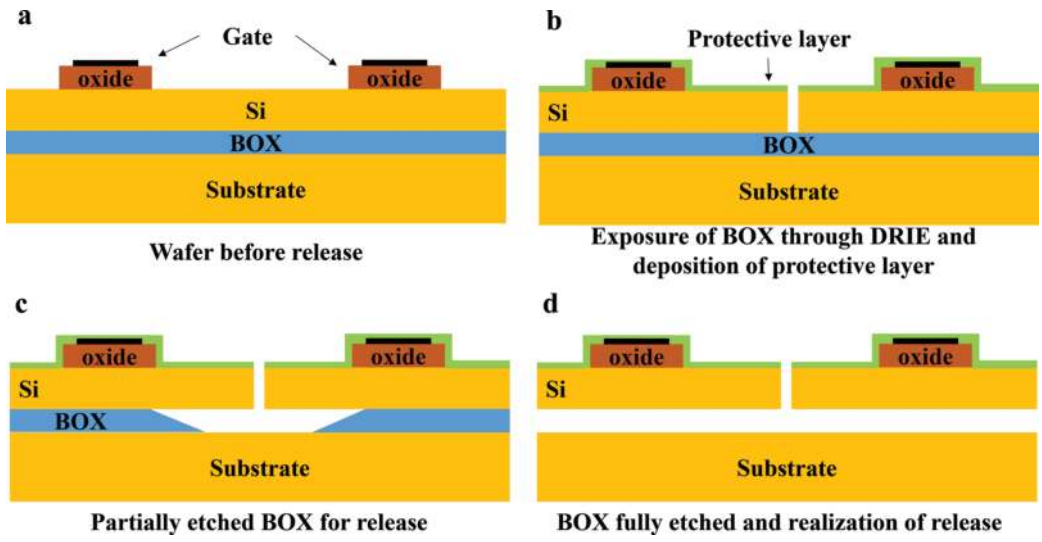

Figure 9.
The process flow for release through removal of BOX.

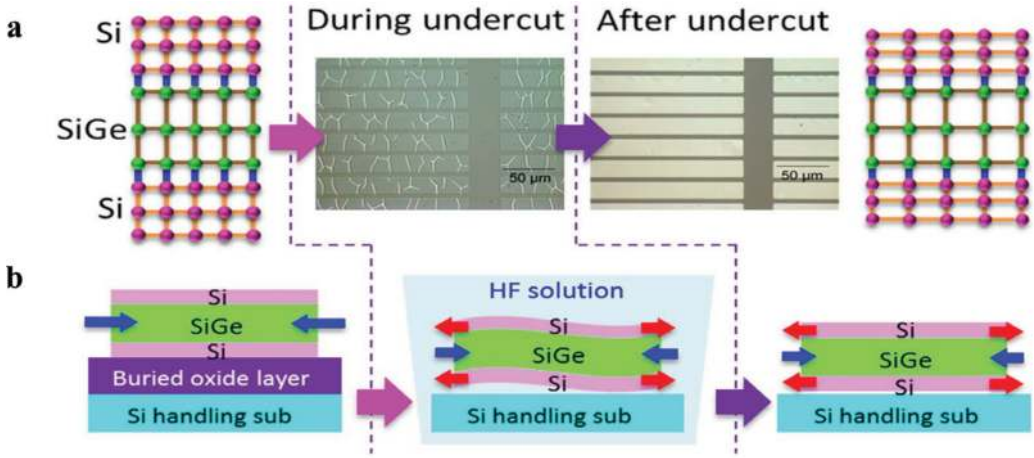

Figure 10.
(a) Atomic lattice schematic diagram showing the strain sharing principle. Optical images show the strained NM during release and after finishing release. (b) Process flow to implement the strain sharing principle and the release. Reproduced with permission [25]. Copyright 2013, nature publishing group.

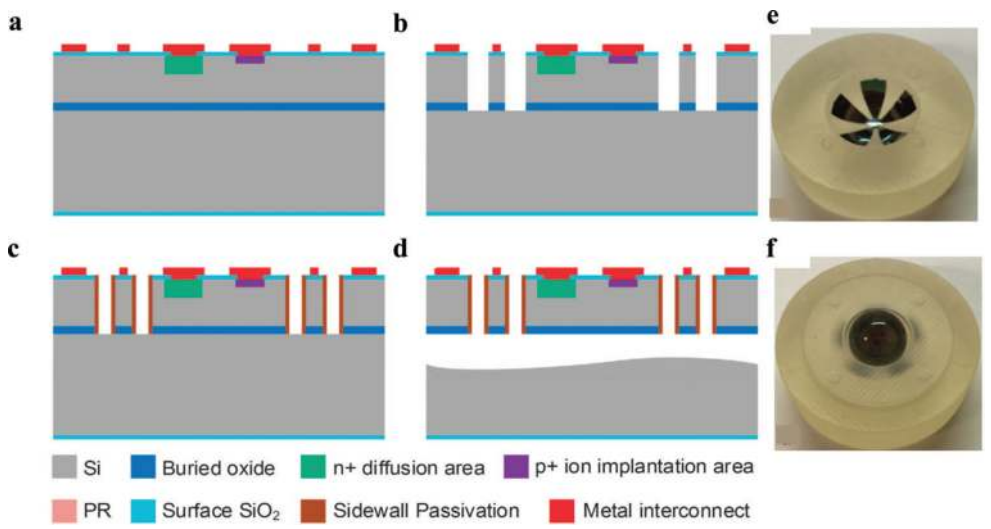

Figure 11.
DRIE process flow and fabricated monocentric imager: (a) after fabrication of photodiode circuitry, (b) pattern tessellated structures thru Si device and buried oxide layers, (c) sidewall passivation, (d) released device by XeF_2 etching, (e) a released and curved device transferred into a hemispherical fixture, and (f) a mounted monocentric imager. Reproduced with permission [35]. Copyright 2016, nature publishing group.

under the BOX is performed by using DRIE or RIE (**Figure 11b**). Following exposure septs, protective layer is coated overall to protect other parts of silicon from damage through etching (**Figure 11c**), and the materials such as Al, PR, GaN, and SiO_2 can be used as protective layer in this process. After that, a RIE etching is performed to remove the protective layer at the bottom of the trenches. At last, the wafer is placed in XeF_2 RIE to etch the silicon under the BOX. Once the undercuts meet with each other, the SOI and the BOX is completely released from the bulk substrate (**Figure 11d**). After the release process, the wafer will be transferred to flexible substrate, and a bonding process will be performed to bond wafer to flexible substrate.

Wu et al. (2016) employed this release process to fabricate a silicon-based flexible imager [26–33], and **Figure 11** shows the process flow to release an imager from the carrier substrate and the fabricated mounted monocentric imager. Sevilla et al. used this release process to fabricate a silicon-based flexible FinFET. **Figure 12** shows the basic steps to release FinFET from the carrier substrate, the fabricated FinFET, and the flexible FinFET wafer [34].

2.3 Backside-release process for flexible silicon membrane

Instead of etching the BOX and undercutting silicon substrate under the BOX, backside-release process etches the silicon substrate from the backside. Lapping, CMP, and RIE can be employed in this release process. The mechanisms of CMP and XeF_2 RIE are already introduced in this chapter, and in this section the comparison between CMP, XeF_2 RIE, and lapping is described. Following that, the process flow is described through the example in which lapping, CMP, and RIE are employed to thin the silicon substrate.

2.3.1 Comparison between CMP, RIE, and lapping

CMP, RIE, and lapping are used to realize backside-release, and we compare these tree fabrication processes to know how to choose suitable fabrication process.

The mechanisms of CMP and XeF_2 RIE are already introduced in previous sections, and lapping is a mechanical process in which a pad is used with polishing liquid to remove excess silicon from a wafer substrate. Lapping takes place between

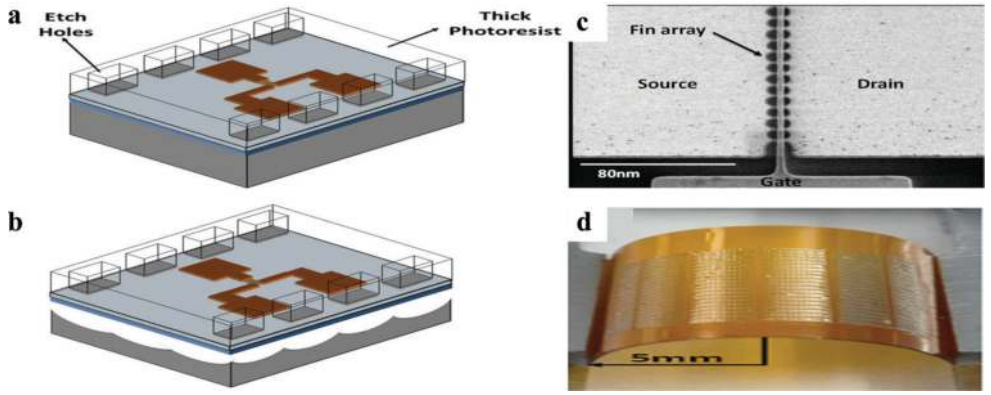

Figure 12.
(a) Spin coat of thick (7 μm) photoresist and hole patterning, (b) cavern formation beneath BOX due to XeF_2 etchant, (c) top view of fins after the gate etch process, which is a complex task performed with a combination of reactive-ion etching and wet cleans, and (d) FinFET silicon fabric at minimum device scale bending radius (5 mm). Reproduced with permission [34]. Copyright 2014, John Wiley & Sons, Inc.

two counter-rotating cast iron plates and either an abrasive film or slurry. To adjust the penetration of the film/slurry, the wafers either spin faster or experience a heavier load to fit the target specification.

The surface roughness of silicon is about 50 nm by using CMP, and through lapping the surface roughness of silicon can achieve 1 μm. The surface roughness of silicon by using RIE is worst about 10 μm. The cost of RIE is the most expensive, because this process needs also a working gas and vacuum environment. The CMP process is more expensive compared to lapping, because CMP consumes chemicals while lapping involves mechanical polish only. For thinning substrate, man can chose suitable process depending on the surface roughness and the cost.

Figure 13 shows three present backside thinning processes by using CMP, RIE, or lapping. For thinning through lapping and XeF_2 RIE (**Figure 13a**), at first the substrate is reduced to exact thickness (usually about 50 μm) by lapping for cost saving, and after that the resulting surface micro-crack damages induced during the lapping process are removed by XeF_2 etching processes with the buried oxide layer as the etch stop layer. Thinning process through anisotropic RIE (**Figure 13b**) possesses advantage high etch rate about 20 μm/min and disadvantage high surface roughness. At first the wafer is turned upside down, and then the substrate is thinned through RIE. The thickness of substrate is controlled by a measurement. Besides RIE and lapping, backside-release can be also performed through CMP, and **Figure 13c** shows this thinning process. Compared with RIE and lapping, the etch rate of CMP is much lower about 0.5 μm/min, and the surface roughness is best at about 50 nm. Usually for cost saving, before CMP process, the substrate can be thinned through lapping, and after lapping process expensive and more precise CMP is performed to further thin the substrate.

2.3.2 Process flow of backside-release process

2.3.2.1 Backside-release process using lapping and XeF_2 RIE

Lapping and XeF_2 etching can thin the SOI wafer from the backside all the way to the BOX layer with a clean surface finish due to high selectivity between SiO_2 and Si in XeF_2 RIE. This process involves three steps. At first the wafer is coated by protective layer to protect the parts of wafer that shall not be etched from damage through isotropic XeF_2 RIE. Following that, the substrate can be thinned to certain thickness by lapping. At last, the rest of Si substrate is removed by XeF_2 RIE, and

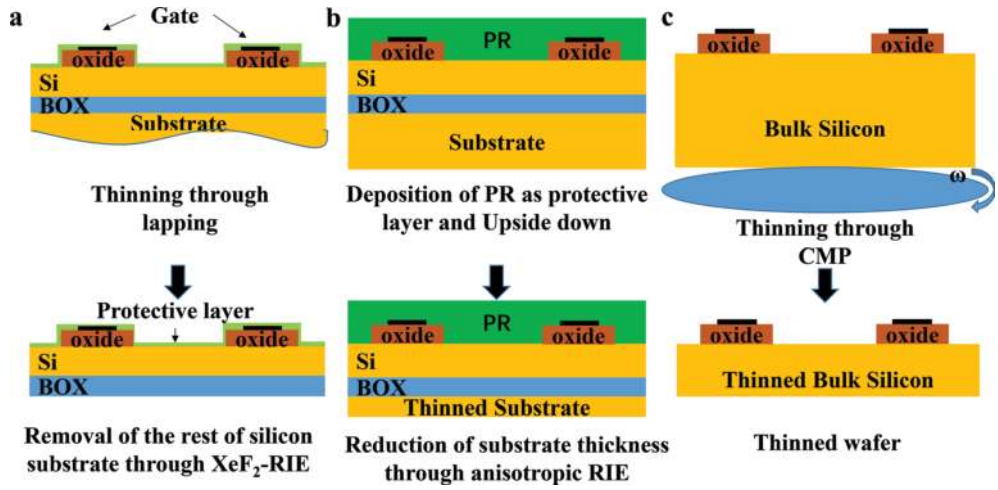

Figure 13.
The schema for three present backside thinning processes by using CMP, RIE, or lapping. (a) Thinning through lapping (first step) and XeF_2 RIE (second step), the BOX serves as stop layer for XeF_2 RIE, (b) thinning through RIE by using working gas such as CF_4 and SF_6, and (c) thinning through lapping (first step) and CMP (second step).

the BOX serves as stop layer for XeF_2 RIE. With the help of XeF_2 RIE and stop layer, the resulting surface micro-crack damages induced during the lapping process can be removed. After thinning process, the wafer is transferred to a flexible substrate, and a bonding process will be performed to bond wafer to flexible substrate.

Hsieh et al. used this process to fabricate a biocompatible flexible IC. At first a wafer lapping machine is used to thin the Si wafer substrate, and the thickness is reduced to ~50 μm [28]. Following lapping, a dry XeF_2 etching process with BOX as etch stop layer is performed to remove the surface micro-crack damages that are caused by the lapping process [28]. Liu et al. employed this process to fabricate a spherical flexible CMOS retina chip. They thinned the backside Si to a thickness of around 50 μm by mechanical lapping, and after that a dry etching such as XeF_2 or RIE is used to etch the Si substrate down to around 10μm thickness and remove the surface micro-crack damages induced during the lapping process [33].

2.3.2.2 Backside-release process using RIE

Instead of lapping and XeF_2, RIE can be directly used to thin the backside bulk silicon substrate, although it results in high roughness.

This backside-release process consists of deposition of photoresist to protect wafer during etching and RIE etching with thickness measurement of the substrate. In this process, the substrate can be traditional bulk substrate or SOI substrate, because the thickness is controlled by a measurement instead of a stop layer. Moreover, the protective layer against etchant is not needed for this process, because an anisotropic RIE is used to thin substrate. The PR is coated to protect the ultrathin wafer from mechanical damage such as scrape and fracture. Working gases such as CF_4 and SF_6 are used to etch the silicon in RIE.

Sevilla et al. have used this approach to fabricate a flexible nanoscale high performance FinFET [36]. **Figure 14a** shows wafer with FinFET before the release process. First step for this process is deposition of PR that servers as protect layer against mechanical damage (**Figure 14b**). After deposition of PR, the wafer is turned upside down, and the substrate is thinned through RIE (**Figure 14c**). The thickness of substrate is controlled by measurement; when the thickness is the same to the plan, the thinning is finished. Otherwise, the wafer is placed in RIE again for further reduction of substrate. **Figure 14d** shows the thinned wafer, and

at last the PR layer is removed (**Figure 14e**). If the SOI is not very thin and the surface is hard, this PR layer is not anymore necessary for this release process.

2.3.2.3 Backside-release process using CMP

Besides RIE and lapping, backside-release can be also performed through pure CMP process. The etch rate of CMP is much lower than RIE and lapping, but the surface roughness is the best and in the order of 10 nm or less. Since CMP process is very slow, it usually starts with a thin substrate, for example, 100–200 μm or after a lapping process with reduced thickness for cost saving purpose.

Dumas et al. use CMP to fabricate curved focal plane detector array for wide field cameras. To spherically curve the device, they used CMP to thin the substrate. In their experiment, the process is designed to obtain a component thickness of 50 μm [37]. They have demonstrated that 10 × 10 mm^2 silicon samples thinned down to 50 μm could be curved in concave and convex shapes, down to a bending radius of 40 mm [37]. The curved detector is showed in **Figure 15**.

2.4 Transfer processes and bond technique

After the release, the released membranes are transferred to flexible substrate and then bonded to flexible substrate. Now we introduce transfer process and bond technique for silicon-based flexible electronics.

2.4.1 Transfer through polymer stamp

In this transfer process, a photoresist or similar polymer layer is deposited, and then a flat piece of polymer such as poly(dimethylsiloxane) PDMS serves as stamp, which conformally contacts the top surface of the wafer. When the stamp is in contact with the PR, it is carefully peeled up with the released thin membrane. The interface between stamp and photoresist must be strongly bonded, and the wafer is transferred on a flexible substrate. The flexible substrate can be polyimide substrate or liquid crystal polymer (LCP) substrate, and the polyimide adhesion

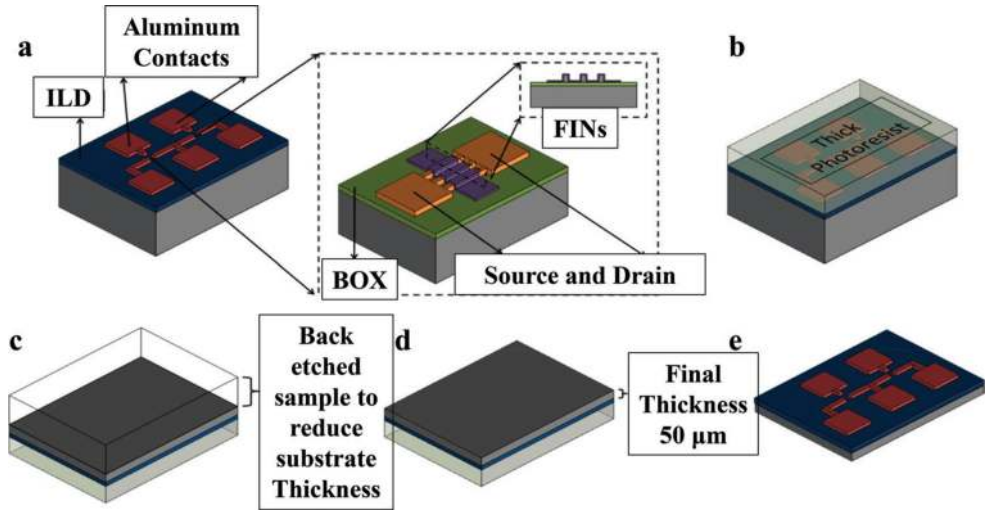

Figure 14.
Process flow for the fabrication of flexible FinFET: (a) produced FinFET devices on SOI substrate (90 nm SOI with 150 nm BOX); (b) deposition of PR to protect chip from damages induced by back etch process; (c) FinFET devices etched from backside using RIE process; (d) Si substrate thinned to 50 μm; and (e) removal of PR. Reproduced with permission [36]. Copyright 2014, American Chemical Society.

promoter is spin coated on substrate; once the wafer is brought to polyimide, the wafer is baked to cure polyimide adhesion promoter. At last the PR and stamp are striped. This transfer process is the same to the process shown in **Figure 16a**.

Figure 16a shows a transfer process developed by Menard et al. In this process, bendable single crystal silicon thin film transistors are printed on plastic substrates. At first they brought a flat piece of PDMS that served as stamp into conformal contact

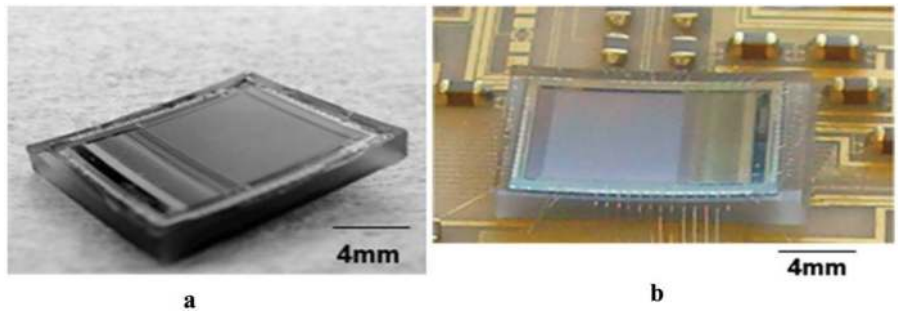

Figure 15.
(Color online) Pictures of curved microbolometer. (a) The thinned curved component on a glass holder. (b) This curved bolometer is bonded onto an electrical board. Reproduced with permission [31]. Copyright 2012, The Optical Society.

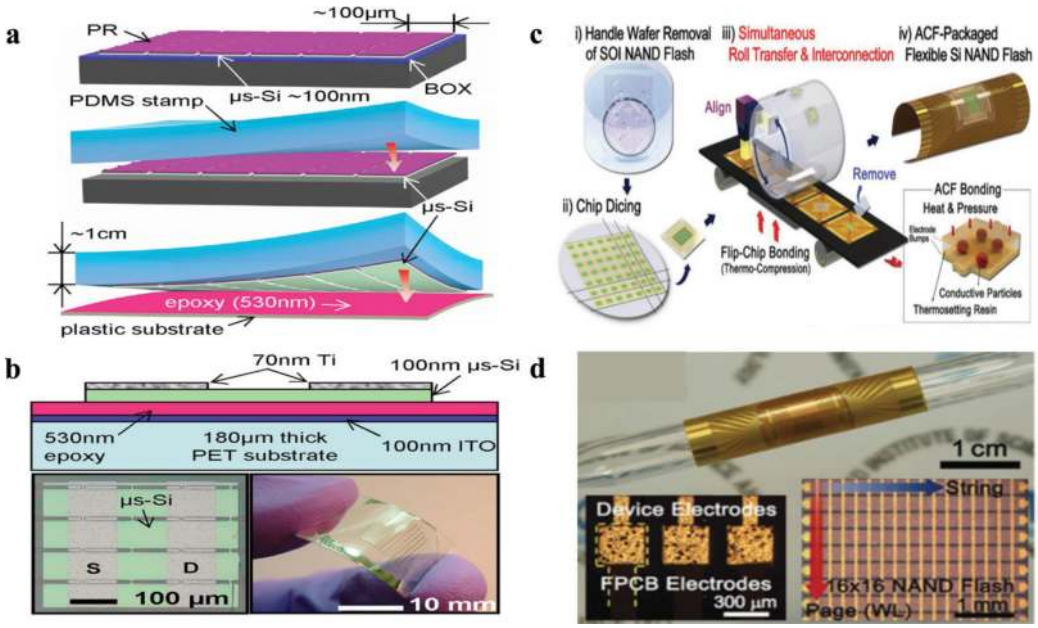

Figure 16.
(a) Process flow for transfer released silicon (μs-Si) ribbons to a plastic flexible substrate. Reproduced with permission [38]. (b) the schematic structure of a flexible thin film transistor with high performance, which was transferred on a PET substrate. The bottom insets show optical images of a device array. In insets, we can see that each device consists of four interconnected microstrips of μs-Si (100 nm thick). Reproduced with permission [38]. Copyright 2005, American Institute of Physics. (c) Process flow for the fabrication of the ACF-packaged flexible Si NAND flash memory using roll-based thermo-compression bonding. (i) Fabricated NAND flash on an SOI wafer was bonded with transfer glass. Release processes are realized by wet etching of the BOX. (ii) NAND chip bonded on transfer glass was separated by dicing. (iii) the released memory was transferred and interconnected on FPCB by using roll-based transfer. (iv) fabricated ACF-packaged Si f-NAND. As shown in inset, the adhesion and interconnection of the electrode bumps of the device and the FPCB are realized by thermosetting resin and conductive particles, respectively. Reproduced with permission [39]. Copyright 2016, John Wiley & Sons, Inc. (d) Photograph of the highly compliant ACF-packaged f-NAND wrapped on a glass rod (diameter of 7 mm). The OM image of the electrode area (left) and the active device area (right) are shown in insets. Reproduced with permission [39]. Copyright 2016, John Wiley & Sons, Inc.

with PR layer on the surface of the wafer and then carefully peeled back to pick up the released wafer with silicon (μs-Si) ribbons [38]. The interaction between the PR and the PDMS must be strong enough to bond them together for removal, with good efficiency [38]. A 180 μm thick polyethylene terephthalate (PET) plastic sheet coated with a 100 nm thick indium tin oxide (ITO) was used as the flexible substrate [38]. A dielectric layer of epoxy was used to enhance the adhesion between released wafer and flexible substrate and was spin coated on flexible substrate [38]. Bringing the PDMS with the μs-Si on its surface into contact with the warm epoxy layer and then peeling back the PDMS led to the transfer of the μs-Si to the epoxy [38].

Kim et al. demonstrate simultaneous roll transfer and interconnection of Si-based flexible NAND flash memory (f-NAND) based on highly productive roll-to-plate ACF packaging [39]. This process is described in **Figure 16b**.

2.4.2 Bonding SOI to flexible substrate

When thinned die or wafer is transferred on the flexible substrate, the bonding between die and flexible substrate must be performed in order to realize the electrical connection between die and other devices.

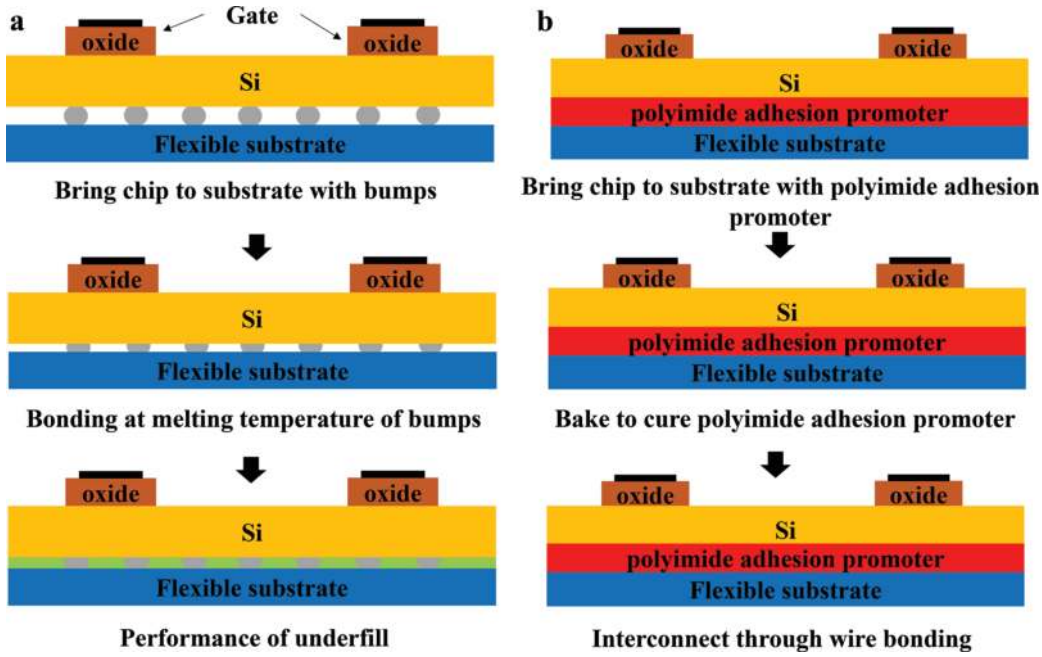

Figure 17.
(a) Process flow for flip-chip bond and (b) process flow for adhesion method.

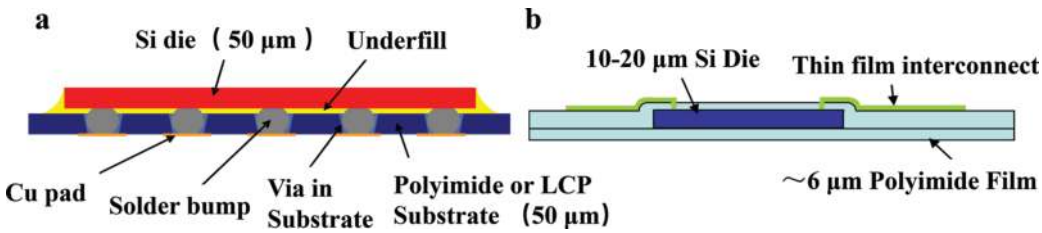

Figure 18.
(a) Illustration of polyimide or LCP substrate and solder assembly approach. Reproduced with permission [40]. Copyright 2008, IEEE. (b) Illustration of thinned Si die embedded in polyimide with thin film interconnect using adhesion method. Reproduced with permission [40]. Copyright 2008, IEEE.

Flip-chip bond and adhesion method can be used to bond released dies to flexible substrate. For the flip-chip bond, polyimide or liquid crystal polymer (LCP) can be used as flexible substrate. For adhesion method, the substrate is made of polyimide, and the interconnection of die is formed through wire bonding.

Flip-chip bond consists of four steps. First, the bumps and pads are fabricated on flexible substrate. Following that, the die is placed on the flexible substrate and aligned. Once the die and bumps are in contact, the bumps are heated at melting temperature, and then die is bonded to substrate. At last an underfill is performed. The materials such as SnPb and SnAg can be used as bumps.

For the adhesion method, a polyimide adhesion promoter such as a dielectric layer of epoxy is applied, so that the die can adhere to polyimide substrate. The polyimide adhesion promoter is spin coated on substrate, and once the wafer is brought to polyimide, the wafer is baked to cure polyimide adhesion promoter. At last the interconnection is formed through wire bonding (**Figure 17**).

Holland et al. [40] used flip-chip bonding to bond die to substrate. Different from our bonding process, they used immersion bump. **Figure 18a** shows thinned die flip-chip bonded on polyimide or LCP substrate. Moreover Holland et al. [40] used also adhesion method to bond die to substrate. Different from our adhesion method, they embed the thinned Si die in Polyimide (**Figure 18b**).

Menard et al. used a dielectric layer of epoxy as polyimide adhesion promoter that was spin coated on substrate to bond the die to polyimide substrate through adhesion method [38].

3. Conclusion

Theoretically, all devices such as transistor circuit, DRAM, NAND flash, and sensors that were fabricated through traditional Si-based CMOS process can also be fabricated in flexible forms by using appropriate release processes and transfer technique. We have mainly described two types of release processes: frontside- and backside-release. The frontside-release is realized by etching the BOX or undercutting silicon under the BOX in SOI wafer. The BOX layer etching is achieved in wet etching with HF-contained etchant, and the bulk silicon undercutting is achieved by XeF_2 isotropic etching. The backside-release process etches the Si substrates through CMP, lapping, or RIE. After releasing, the Si thin membrane with active devices is transferred to a flexible substrate. Polymer stamp transfer, flip-chip bond, or adhesion method can be used to bond released dies to a flexible substrate. By leveraging those silicon-based micromachining processes, flexible electronics can be achieved on top of current standard CMOS process and scale to large volume manufacturing.

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