Chapter 3

Intermetallic Bonding for High-Temperature Microelectronics and Microsystems: Solid-Liquid Interdiffusion Bonding

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Additional information is available at the end of the chapter

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Abstract

Solid-liquid interdiffusion (SLID) bonding for microelectronics and microsystems is a bonding technique relying on intermetallics. The high-melting temperature of intermetallics allows for system operation at far higher temperatures than what solder-bonded systems can do, while still using similar process temperatures as in common solder processes. Additional benefits of SLID bonding are possibilities of fine-pitch bonding, as well as thin-layer metallurgical bonding. Our group has worked on a number of SLID metal systems. We have optimized wafer-level Cu-Sn SLID bonding to become an industrially feasible process, and we have verified the reliability of Au-Sn SLID bonding in a thermally mismatched system, as well as determined the actual phases present in an Au-Sn SLID bond. We have demonstrated SLID bonding for very high temperatures (Ni-Sn, having intermetallics with melting points up to 1280°C), as well as SLID with low process temperatures (Au-In, processed at 180°C, and Au-In-Bi, processed at 90–115°C). We have verified experimentally the high-temperature stability for our systems, with quantified strength at temperatures up to 300°C for three of the systems: Cu-Sn, Au-Sn and Au-In.

Keywords: microelectronics/microsystem assembly, bonding technology, harsh environments, wafer processing, reliability, transient liquid phase

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1. Motivation for SLID

1.1. The challenge of die attach and interconnection

For all electronic systems, the attachment of components to substrates and their electrical connection is a crucial part of the system. Traditionally, the processes for attachment and interconnection have been considered more a craft than a science. The historical focus of electronics and microtechnology has been on the design, manufacturing and testing of components, circuits and devices, rather than on the system integration and the processes needed for actually building the system.

The 'electronic revolution' has given ever-increasing performance of devices at ever-decreasing prices for more than half a century. Initial milestones were the invention of the transistor (1947) and the integrated circuit (IC) (1958). The driving factor has been a continuous decrease in size (of components and on features of components) and cost, made possible through batch processing of silicon wafers. Single-crystal silicon is a very well-defined material with extremely well-characterized properties, allowing process technology that yields extremely small features (10 nm by 2017, with a further decrease expected). Miniaturization of components and the use of large Si wafers give a huge number of components manufactured in every batch, lowering the cost. Furthermore, miniaturization allows an increase in operating frequency (or a decrease in response time), as well as lower losses. The miniaturization and the high-frequency performance of the attachment and electrical interconnect technology has not maintained the same pace as the integrated circuit technology. The need for a more scientific approach for the system-integration technologies has become evident and has gradually evolved over the last decades [1]. The scientific approach is typically termed 'packaging technology', 'system-integration technology' or 'assembly, interconnect and packaging'.

Today, it is generally acknowledged that system-integration technologies often are the limiting factor for the success of an electronic system, in particular, in four different aspects: size, performance, price and reliability.

1. Size: the dimensions needed for electrical interconnections are far larger than the dimensions possible in Si technology. Also, a complex integrated circuit will typically need a high number of interconnects. Hence, the actual size of the component will typically be defined by the space needed to create the interconnects, rather than by the complexity of the IC itself.
2. Performance: a larger feature size implies a larger parasitic inductance and capacitance, as well as a longer signal path. This will limit the high-frequency/high-speed performance of the device. Typically, the packaged device therefore shows a lower operating frequency than what the naked chip would allow.
3. Price: the low price of Si chips is enabled by the parallel processing of a large number of components, in batch processes using large wafers. System-integration technologies such as die attach and electrical interconnection are traditionally processes treating single components, thus being serial processing rather than parallel processing. When the number of devices is high, these serial processes will be more expensive than the parallel Si processing.

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4. Reliability: the most common reason for failure of a system is broken interconnects. There are various reasons for this, some examples are stress caused by different thermal expansions of chip and substrate, uncontrolled growth of intermetallic layers where two metals are joined and galvanic corrosion. Understanding the behaviour of the materials that make up the integrated system is therefore crucial for reducing the failure rate of a device.

In summary, there is a strong need to continue research on interconnect technology, with the aim to construct reliable interconnects in a manufacturing-friendly process. The actual requirements will vary greatly depending on the application, but the possibility to miniaturize the interconnect, as well as to have low electric resistance and high mechanical strength, is an important requirement in many applications.

1.2. Soldering: the standard interconnection technique

The most commonly used interconnection technique is soldering. Any new technology is therefore naturally compared with soldering. Soldering is used in a number of different technologies, with a range of solder materials and on different dimensions of the joints. The common nature for any solder process is the use of a solder material that melts upon heating (wetting the two surfaces that are to be joined), and solidifies upon cooling (forming a solid joint). Typical solder materials are eutectic compounds, chosen because of their low and well-defined melting points. Historically, the standard solder material has been eutectic Sn-Pb, with a melting/solidification temperature of 183°C. Upon the ban of Pb in electronics (RoHS initiative) in 2002, a variety of lead-free solders have emerged, such as Sn-Ag-Cu compounds. The most common is 'SAC305', composed of 3.0% Ag, 0.5% Cu and 96.5% Sn, with a melting point of 220°C (as comparison, pure Sn melts at 232°C).

The advantages of soldering include the following:

1. Short process time: the melting and re-solidification in a eutectic-soldering process are both instantaneous processes. The soldering process does not depend on time-consuming process like chemical reactions, solid-state plastic deformation, stress relaxation or curing.
2. Self-alignment: a certain, initial misalignment of chip and substrate is compensated. While the solder is liquid during the bonding process, the chip can self-align because there is a driving force to minimize the surface tension of a liquid solder. Self-alignment relaxes the requirement to assembly precision, which can lower the cost substantially for fine-pitch systems.
3. Compensation of geometric imperfections: due to the liquid state during bonding, a solder process will create contact also if there is a variation in pad height, surface roughness or non-parallel contact surfaces.
4. Easy reworkability: the solder process is reversible, remelting at the same temperature as the original melting/solidification. Rework may be performed simply by re-heating the solder joint.
5. High conductance of joint: because of the metallic nature of the solder.

1.3. Shortcomings of soldering

Although soldering is a very versatile process, considered to render high reliability, it has certain shortcomings.

Solder joints will not withstand temperatures approaching the melting point of the solder. The joint will fail if the melting point is reached, but will also be susceptible of severe degradation, for example, by creep, at temperatures significantly below the melting temperature. A number of high-temperature applications, such as engine control, oil and gas down-hole instrumentation, geothermal energy and thermoelectric generators, require bonding that can withstand higher temperatures than the solder can. High temperatures may also be an issue during manufacturing: if chips are stacked in three dimensions (3D), more than one bonding process is required. For sequential bonding, soldering with the same solder alloy will jeopardize the earlier made connections. This may to a certain degree be solved by choosing different solder compounds with different melting points. However, there are a limited number of relevant solder alloys, and the corresponding span in melting temperatures is limited, also taking into account that high-temperature solders require high process temperatures and low-temperature solders limit the useful application of temperatures.

If the solder joint is subject to elevated temperature for a prolonged time, the intermetallic layer at the component/pad interface will increase in thickness in an uncontrolled way. Hence, the properties of the joint will change with time. The intermetallic compounds (IMCs) are typically harder and more brittle than the pure metals, particularly compared with Sn-based solder. The interface between the soft solder and the hard intermetallics is a typical fracture site when the joint is subject to mechanical load.

The liquid nature of solder bonding gives rise to a risk of short circuits between neighboring interconnects, if the liquid solder flows between. This dictates a minimum isolation distance between interconnects and is thus a limiting factor for miniaturization, particularly for devices with many interconnects, such as digital circuits.

1.4. The principle of SLID

Solid-liquid interdiffusion (SLID) bonding is a technique based on intermetallics as the bonding medium, receiving increasing attention as an alternative to processes such as solder bonding [2, 3]. While resembling solder bonding in terms of process temperature and materials in use, SLID bonding has an excellent thermal stability: the bond survives temperatures far surpassing the bonding temperature. This makes SLID bonding a promising candidate for high-temperature applications, where solder bonding is not applicable.

The SLID process (also known as transient liquid phase bonding [4–6], isothermal solidification [7] or 'off-eutectic bonding' [8]) uses a system of two metals, where one melts at a high temperature (such as Cu, Au, Ag and Ni) and the other melts at a low temperature (such as Sn and In). The bonding process takes place at a temperature somewhat above the lower melting temperature, assuring interdiffusion of the two metals reacting to intermetallic compounds (IMCs) with high-melting points [9] (see Cu-Sn phase diagram in **Figure 1** as an example). To obtain the high-temperature stability, a complete conversion of the low-temperature melting metal to IMC is needed. Excess of high-temperature metal is normally

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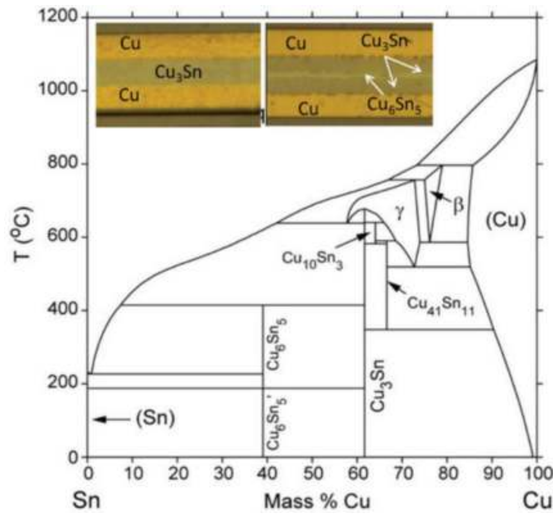

Figure 1. Cu-Sn phase diagram. The insets show a cross section of SLID bonds: complete conversion to Cu_3Sn (left), and incomplete conversion with the remaining Cu_6Sn_5 layer (right).

desired, to allow for process variations such as deviations in the initial layer thickness and any inhomogeneous diffusion during bonding, and to ensure that no reaction takes place between the low-temperature metal and the thin metal layers that serve as adhesion/barrier layers between the two-metal system and the substrate/chip. Such reactions might result in new IMCs with less predictable properties. Importantly, an excess of high-temperature metal also gives ductility to the final bond (the pure metal normally being more ductile than the IMCs).

The Cu-Sn SLID system is the one that has received the most attention. As seen from the phase diagram in **Figure 1**, two IMCs are stable at room temperature: Cu_6Sn_5 and Cu_3Sn. The goal of a Cu-Sn SLID process will be a system in thermal equilibrium with remaining Cu on both sides of the IMC bond-line, implying Cu_3Sn as being the desired phase.

The initial layers of Cu and Sn are typically in the range of micrometres. The bonding process temperature is above the melting point of Sn (232°C), typically in the range of 250–300°C. Cu diffuses into the liquid Sn, and the IMC Cu_6Sn_5 solidifies isothermally. At the Cu/Cu_6Sn_5 boundary, Cu and Sn react to form Cu_3Sn. Cu_3Sn formation is much slower than Cu_6Sn_5 formation, since solid-state diffusion through the Cu_6Sn_5 layer is required. The bonding temperature is kept for sufficiently long time (typically ~30 min) for the reaction to Cu_3Sn to be completed; the final bond consisting of a Cu/Cu_3Sn/Cu layer structure. The bond is then in thermal equilibrium, and no material change is expected upon annealing or aging. The melting temperature of this completed bond-line is ~700°C.

Although the high-temperature stability was the original motivation for developing SLID for interconnections [9, 10], it also has good promise for creating fine-pitch interconnection [3]. Also, the ability to form thin, well-defined bond-lines with metallurgical bond is a specific advantage of SLID [11].

In this book chapter, we detail some of the main results from the SLID research at University of Southeast Norway (USN), which is ongoing during the last decade.

2. SLID bonding

2.1. Test vehicles and substrates

Much of the SLID work done in our group, as well as in other research groups, is carried out by bonding pairs of silicon chips. Si is the standard material for electronics as well as for MEMS (Micro-Electro-Mechanical Systems). Stacking multiple chips on top of each other is increasingly important, to increase integration density by also using the third dimension. By bonding identical materials, the challenge of a thermal mismatch is minimized: during temperature variation, the two bonding partners will experience the same dimensional change, thus minimizing thermomechanical stress.

For the typical bonding process where a chip is bonded to a substrate, the challenge of dissimilar thermal expansion of a chip and a substrate arises. Thermomechanical stress is the result when dissimilar materials are joined together and experience temperature variations. Solder bonding is suitable to handle this, since solder is soft and the solder thickness typically is >100 μm. SLID bonding typically uses thin bond-lines, in the micrometre range. Since the SLID process relies on diffusion, thin layers ensures that the bonds can be manufactured in a reasonable time. Furthermore, the IMC bonding layers are much harder than a solder and will therefore not absorb much of the thermomechanical stress. The remaining layers of a high-melting point metal (such as Cu or Au) may be utilized as the stress-absorbing layer. In our work, we have also bonded SiC chips to ceramic substrates with a significant thermal mismatch using Au-Sn SLID, obtaining excellent reliability in thermal cycling, as will be detailed subsequently.

2.2. Metal layers: design and manufacturing

The layer thicknesses of our initial two-metal system (such as Cu and Sn in the case of Cu-Sn SLID) are typically in the range of micrometres, produced by electroplating. The process is therefore well suited for wafer-level processing with additive patterning, opening for cost-effective solutions and for fine-pitch applications. The layer thicknesses should be designed so that there remains a high-temperature metal after the bond is finalized. Using Cu-Sn SLID as the example, a thickness ratio (Cu to Sn) of 1.3 is needed in order to obtain a final $Cu/Cu_3Sn/Cu$ structure, as seen by

$$\frac{t_{Cu}}{t_{Sn}} > \frac{3\,M_{Cu}\,\rho_{Sn}}{M_{Sn}\,\rho_{Cu}} = 1.3 \tag{1}$$

(where t_{Cu} and t_{Sn} signify the initial total thickness on the two bonding partners, M_x and ρ_x signify the atomic weight and the mass density of element x). Note that this Sn layer may be deposited on one of the bonding partners, or half the thickness on each of the bonding partners. Whereas Eq. (1) dictates the maximum relative Sn thickness, the overall roughness of Cu layers dictates a minimum Sn thickness: since Cu is solid during the entire bonding process, the highest protrusions of the Cu layer will define the standoff height between the two bonding partners. Such

protrusions may be present, for example, at the edges of electroplated layers. As a rule of thumb, the Sn layer should be thicker than the variation in the surface height of the Cu layer, to ensure that liquid Sn fills the volume between the two Cu pads and thus minimizes void formation.

Alternative metal deposition techniques are evaporation, sputtering, printing or the use of preforms. With the exception of preforms, all are compatible with wafer-level processing and patterning. Preforms can be used for die bonding where fine-pitch patterning is not required and for proof-of-concept experiments. Evaporation and sputtering are restricted to thin films (not much more than 1 μm). Printing (of metal pastes) is a low-cost and versatile process, typically giving thicker (tens to hundreds of micrometres) metal layers, with somewhat lower precision in the lateral feature size than the photolithography-defined techniques (evaporation, sputtering, electroplating). Pastes may be formulated with a small particle size to allow fast reactions, but the availability of relevant pastes is presently limited.

2.3. Bonding profiles

The bonding profile (temperature and pressure as a function of time) chosen is crucial in order to obtain optimal results within a reasonable time frame. To obtain a uniform growth of the IMC layers, a short holding time slightly below the melting temperature is typically used [12]. This ensures a thin IMC layer formed at the material interfaces while all materials are solid. This controls diffusion through the solid IMC also when the low-melting point metal is melted. If the temperature is raised to the melting point without this interface IMC formed, the system is prone to scallop growth of IMCs, with voids in the bond-line as a result [13, 14].

2.4. Wafer-level versus chip-level bonding: atmosphere during bonding

We perform bonding at a chip level as well as at a wafer level. Wafer-level processing is the preferred option for high-volume industry, since the parallel processing increases throughput greatly and has the potential for lowering the unit cost. Chip-level processing is the relevant choice for low-volume industry. In a research setting, chip-level bonding also allows for more variation of process parameters to be optimized.

For Sn-based solder on Cu pads, the use of flux is essential for avoiding oxides during soldering. However, remaining flux is a challenge, particularly for vacuum cavities in MEMS devices. Also, the cleaning of flux residues is more difficult for thin SLID bonds than for solder bonds with a higher chip-to-substrate separation. All the SLID bonding in this work (Cu-Sn as well as other systems) is therefore flux-free. For Cu-Sn SLID, this is obtained by using equal Sn thickness on both bonding partners, Sn oxides being thinner and more readily absorbable in the bond-line than Cu oxides [15].

2.5. Characterization

The performance of the bonds is evaluated by shear testing. Usually, shear testing is performed at room temperature. In addition, we performed shear testing while the bonded sample was heated, to verify the applicability of the SLID bonds at elevated temperatures. The fracture surfaces after die shear are inspected in order to identify the fraction sites, showing up at the weaker parts of the SLID bonds.

The bond-line morphology and the phases present are investigated by cross-section microscopy. Cross-sections are made either by mechanical grinding and polishing or by Ar ion milling. Samples are inspected by using optical microscopy and scanning electron microscope (SEM) with EDX (energy-dispersive X-ray spectroscopy). For Au-Sn, we also used X-ray diffraction in order to more clearly identify the phases in the bond-line.

3. Cu-Sn bonding

3.1. Rationale for Cu-Sn

Cu-Sn is by far the most investigated SLID bonding system and also the one used as an example in the previous section. It is the natural choice in applications sensitive to cost, and the material system is quite similar to what is common in soldering, where an Sn-based solder applied to Cu pads is the most common configuration. The fundamental understanding of the process is well established. Our group has experimentally verified the high-temperature stability that has long been predicted from the phase diagram, as detailed in Section 8.1. The main part of our work on Cu-Sn SLID has focused on manufacturing aspects: how to make a flux-free wafer-level process with optimized manufacturing parameters and a predictable result possible. This has led to the industrial implementation of our Cu-Sn SLID process [15–17].

3.2. Fabrication process

Our Cu-Sn SLID work has aimed for wafer-level bonding, with initial experiments carried out at chip level. All our work has been on Si substrates with electroplated layers, typically 5 μm Cu and 1–2 μm Sn. For wafer-level bonding, equal layer thicknesses on both bonding partners have been used, and the bonding profile (temperature and pressure vs. time) has been carefully selected to allow flux-free bonding [2, 18]. For the initial chip-bonding, Sn has been electroplated only on the chip side, in order to allow maintaining the substrate hot (no Cu-Sn interdiffusion prior to bonding) while mounting successive Sn-coated chips.

3.3. Wafer-level process optimization

In order to optimize the bonding profile for a Cu-Sn SLID bond, we developed a model for the kinetics of the reactions from Cu and Sn to IMCs [19]. We annealed Cu-Sn bi-layered test structures, at different times and temperatures. The samples were cross-sectioned and layer thicknesses measured in optical microscopy, the different phases having been verified by SEM and EDX. The layer thickness of pure, unreacted Sn was obtained by etching with 30% HCl (selectively etching Sn and not IMCs), measuring the Cu_3Sn and Cu_6Sn_5 thicknesses and thus calculating the Sn thickness. The evolution of the IMC thickness is then modeled by a quasi-diffusion equation:

$$y_t^2 - y_0^2 = k_0 \, exp\left(\frac{-Q}{RT}\right) t^{2n} \tag{2}$$

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where y_t is the IMC thickness, alternatively Sn thickness reacting to form IMCs; T is the absolute temperature; t is the annealing duration, y_0 is the initial IMC thickness, or Sn thickness already reacted with Cu at $t = 0$; n is an empirical exponent, where $n = 0.5$ signifies diffusion as the mechanism; Q is the activation energy; k_0 is the diffusion coefficient.

Values for Q, k_0 and n (shown in **Table 1**) are extracted through linear fitting using appropriate logarithmic plots, and a Matlab model is constructed, predicting the IMC evolution for any given bonding temperature profile [19]. Note that the change in the empirical exponent n reflects the different physical processes occurring: $n = 0.5$ corresponds to the reaction kinetics being limited by diffusion, implying that the reaction to IMCs is fast. Below the melting point of Sn, the reactions are slower, implying that diffusion does not alone contribute to the kinetics.

Figure 2 shows the experimentally observed thicknesses, together with curves for the model given by Eq. (2) and **Table 1**.

Figure 3 shows two different bonding profiles: one where the simulation predicts that a layer of Cu_6Sn_5 remains after bonding and one where the bond is predicted to be fully converted to a $Cu/Cu_3Sn/Cu$ structure. The lower part of the figures shows cross-section micrographs of samples bonded with the corresponding bonding profile, showing a good correspondence to the predicted values. Important parameters from a manufacturing point of view are as follows:

	Cu_3Sn	Reacted Sn
$k_0\left[\frac{\mu m^2}{min^{2n}}\right]$	7.9×10^6	2.8×10^4
$Q\ \left[\frac{kJ}{mol}K\right]$	78	52
Empirical exponent n	0.5 ($T \geq 232^\circ C$)	0.45 ($T \geq 180^\circ C$)
	0.4 ($180^\circ C \leq T \leq 232^\circ C$)	0.3 ($T < 180^\circ C$)

Table 1. Kinetics coefficients for Cu-Sn SLID. Reprinted with permission from Springer Nature [19].

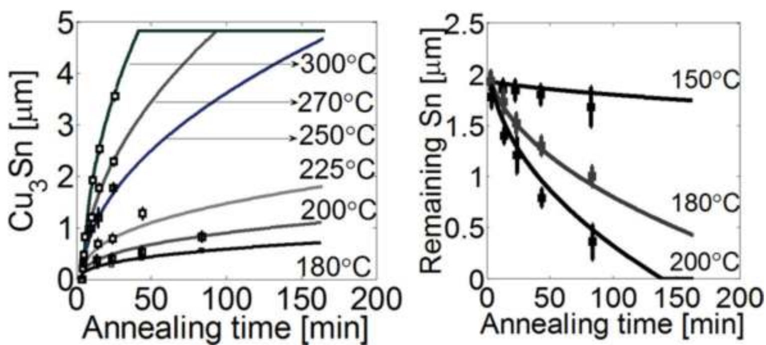

Figure 2. Comparison between simulation results (lines) and measured values (discrete points) for both Cu_3Sn thickness and remaining Sn. Reprinted with permission from Springer Nature [19].

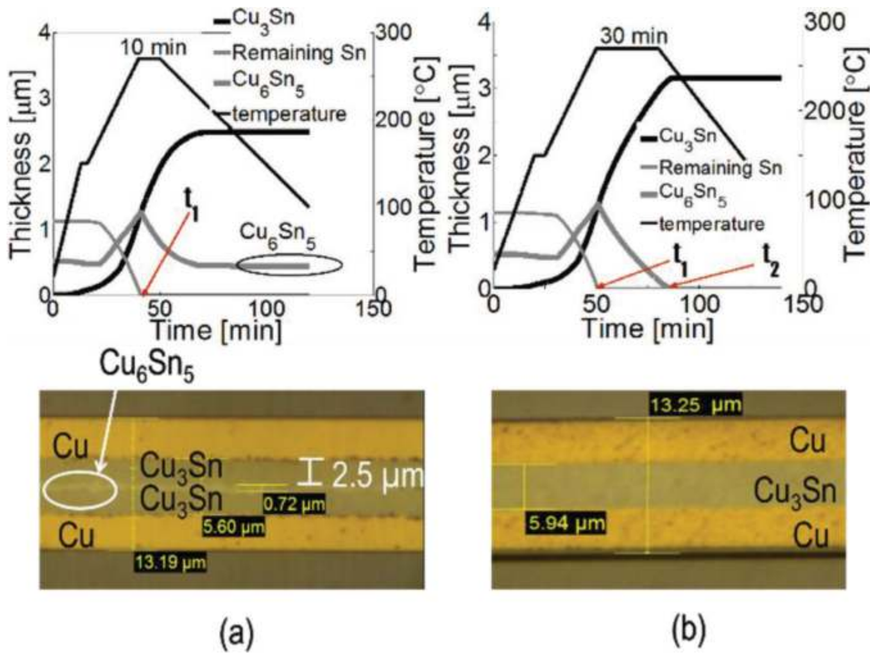

Figure 3. Different bond profiles for Cu-Sn SLID wafer-level bonding and the corresponding cross sections. Reprinted with permission from Springer Nature [19].

1. t_1: the time from the start of the bonding process until all Sn is consumed and the bond has solidified: 41 min for profile (a), 50 min for profile (b).

2. t_2: the time from the start of the bonding process until the final Cu/Cu_3Sn/Cu structure is obtained: 85 min for profile (b), not achieved for profile (a).

t_2 gives the total bonding process time, whereas t_1 gives the minimum time where the wafer bonder should be used (the remaining time to t_2 may be performed as batch annealing).

4. Au-Sn bonding

4.1. Rationale for Au-Sn

Au-Sn is the system of choice for high reliability systems, for example, when chemical inertness and ductility are desired [20]. As a consequence, our work on Au-Sn SLID bonding has included verification of reliability. The Au-Sn phase diagram (see **Figure 4**) is quite more complex than Cu-Sn, and the fundamentals of Au-Sn SLID bonds have previously been less explored than those of Cu-Sn SLID. Hence, our work has included an investigation of the phases present in Au-Sn SLID bonding and the properties of the resulting bond. We have experimentally verified the expected high-temperature stability, as will be detailed in Section 8.1 subsequently.

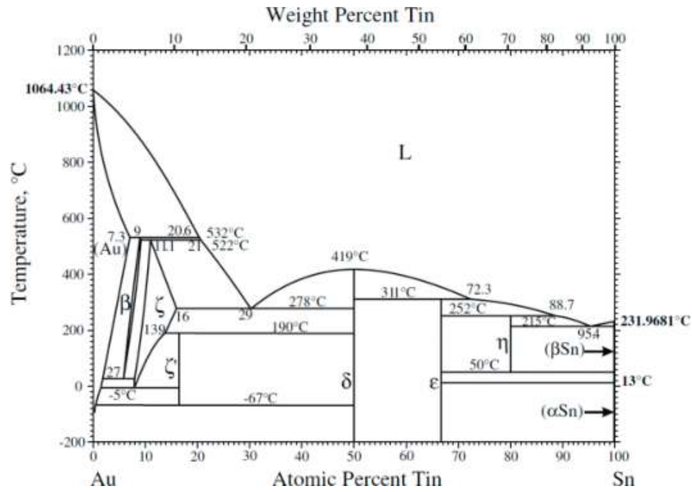

Figure 4. Au-Sn phase diagram, reprinted with permission from Springer Nature [21].

4.2. Fabrication process and testing

For the reliability test and the investigations of the phases present in an Au-Sn SLID bond, a chip/substrate system relevant for use at high temperatures was used: an SiC dummy transistor (BJT) from Fairchild Semiconductor was bonded to an Si_3N_4 substrate with symmetric active metal-bonded (AMB) Cu (150 μm) metallization. This system has a significant mismatch in coefficients of thermal expansion (CTE): SiC and Si_3N_4 having similar CTE of 4.2 ppm/K while the thick Cu layers have a CTE of 17 ppm/K giving a realistic substrate-to-chip thermal mismatch.

The Au-Sn SLID bonding was performed by electroplating 10 μm Au layers on both the chip and the substrate, sandwiching a 7.5 μm thick eutectic $Au_{80}Sn_{20}$ preform between the bonding partners and the bond, varying bonding temperature in the range of 290–350°C and the bonding time in the range of 4–14 min.

The quality of the bonds was probed by die shear testing.

Reliability tests were performed by thermal cycling (1000 cycles, 0–200°C) and high-temperature storage (HTS) at 250°C up to 6 months. Die shear strength was performed after thermal cycling and/or HTS.

Cross-section microscopy was performed on as-bonded and high-temperature-stored samples. The phases were identified by a combination of optical microscopy, SEM/EDX and X-ray diffraction, the latter technique being used both on cross-sectioned samples and on fracture surfaces.

4.3. Main results

The die shear strength of Au-Sn SLID bonds is found to be excellent, in the order of 140 MPa. Such high bonding strengths are obtained for bonding temperatures down to 300°C and bonding times down to 6 min, as shown in **Figures 5** and **6**. A lower bonding time

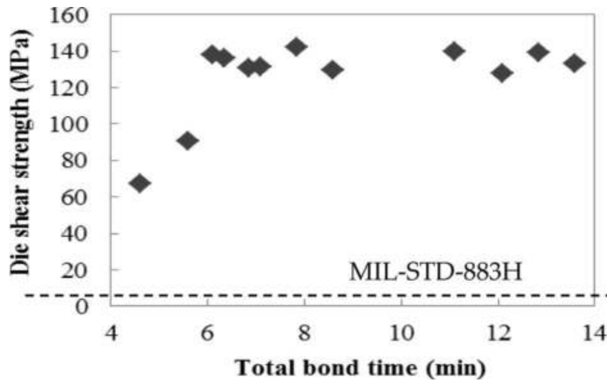

Figure 5. The die shear strength of an Au-Sn SLID bond as a function of the bonding time (time above the melting point of eutectic Au-Sn (278°C)) [22] (© 2012 IEEE).

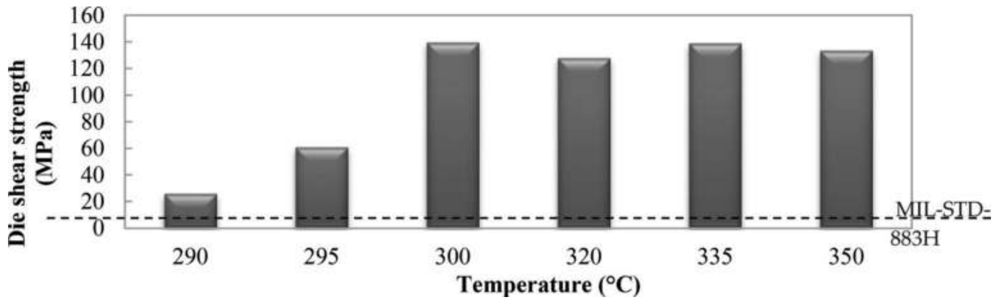

Figure 6. The die shear strength of an Au-Sn SLID bond as a function of the bonding temperature [22] (© 2012 IEEE).

(tested down to 4 min) and temperature (tested down to 290°C) give significantly lower shear strength, but still well above the requirements of MIL-STD-883H [22].

4.3.1. Phases obtained

Figure 7 shows cross-sectional micrographs of a sample bonded at 300°C for 6 min. The IMC layer has been identified by EDX and X-ray diffraction to be the ζ-phase.

Cross-section microscopy (optical and SEM) shows that high-temperature-stored samples have thicker IMC layers compared to the as-bonded. Using X-ray diffraction on cross sections and on fractured bonding surfaces, the IMC layer of these high-temperature-stored samples is identified as the β-phase [23]. This shows that the as-bonded samples with an Au/ζ/Au bond layer structure are not yet in thermal equilibrium. The Au/β/Au structure obtained after our high-temperature storage represents a thermal equilibrium situation, since the Au-Sn phase diagram (**Figure 4**) does not contain phases between Au and β. When designing a layer structure for Au-Sn SLID bonds for high-temperature applications, the overall Au-Sn system should therefore have an Sn content below 8 at%. The evolution of the layer structure upon bonding and aging is sketched in **Figure 8**.

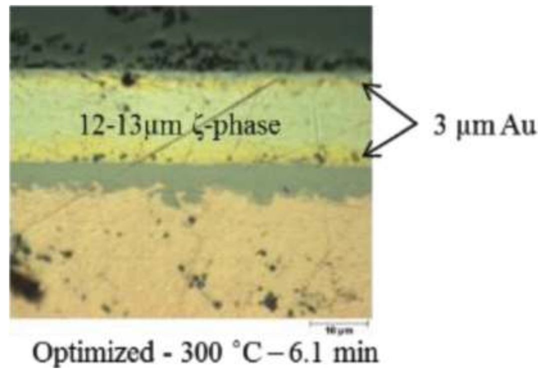

Figure 7. Cross section of an optimized Au-Sn SLID bond [22] (© 2012 IEEE).

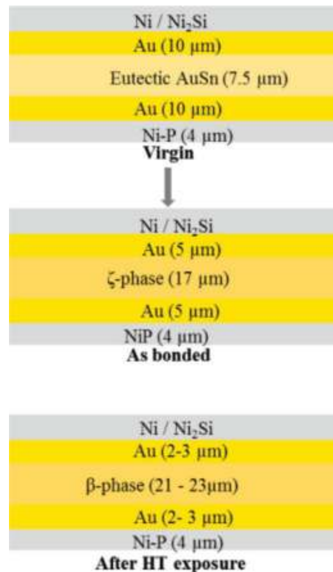

Figure 8. A schematic overview of the layered structure of an optimized Au-Sn SLID bond at different life stages. The different material phases were identified with energy-dispersive X-ray spectroscopy (EDX) and X-ray diffraction. Reprinted with permission from Springer Nature [23].

4.3.2. Thermal cycling survival

Even after combined high-temperature storage and thermal cycling, the shear strength of an Au-Sn SLID-bonded sample is very high, around 70 MPa (see **Figure 9**). This clearly shows that Au-Sn SLID bonding is a suitable choice for high-temperature applications, also with thermally mismatched substrate-chip pairs. The demonstrated reliability is excellent.

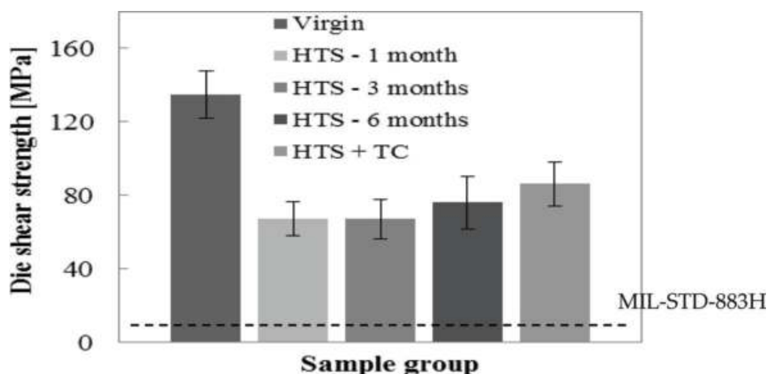

Figure 9. Die shear strength for virgin Au-Sn SLID samples, high-temperature-stored (HTS) samples—at 250°C for 1, 3 and 6 months—and samples exposed for 3 months HTS + 1000 thermal cycles (TC) between 0 and 200°C. Reprinted with permission from Springer Nature [23].

5. Ni-Sn bonding

5.1. Rationale for Ni-Sn

The Ni-Sn material system comprises three IMCs which all have a high-melting point ranging from 798 to 1280°C [24], see **Figure 10**. The high-temperature compatibility is the most frequent reason for investigating the Ni-Sn system [25–27]. In addition, Nickel and tin are relatively low-cost materials which make them attractive for more cost-sensitive applications [26, 28]. The formed IMCs may also have matching thermomechanical material properties which may be critical in applications with very high operation temperatures [29]. Residual Ni can be used as a diffusion barrier for other materials in joint structures, such as Au and Cu, preventing them from contaminating attached devices [30]. The relatively low melting point of Sn, 232°C, also allows similar process temperatures as the Cu-Sn system. In addition, the excellent corrosion resistance of Ni [28] makes the Ni-Sn system attractive for forming SLID joints. Still, information on Ni-Sn SLID joints is sparse.

5.2. Fabrication process

To be able to complete the homogenization process forming Ni-Ni_3Sn joints, the pre-joint structure requires a volumetric ratio, Ni:Sn, of not less than 1.22:1. We have used a symmetric pre-joint structure of 3.0 μm Ni/2.0 μm Sn/2.0 μm Sn/3.0 μm Ni. The layers were built by sputtering a thin Ni layer onto metallized (TiW) Si wafers. The required thickness was achieved by electroplating additional Ni. The top layer of Sn was then electroplated. Samples were pressed together with a contact pressure of about 3 MPa and the temperature was raised above the melting point of Sn and then held there for a period of time until the liquid Sn reacted with the adjoining Ni substrate. The joint was then cooled down. The joint morphology and evolution as a function of process parameters were investigated by changing the

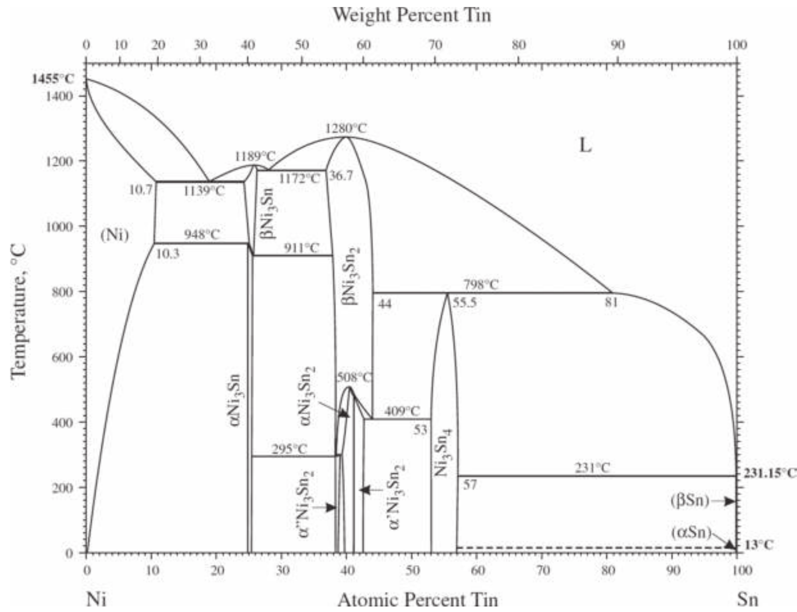

Figure 10. Ni-Sn phase diagram. Reprinted with permission from Springer Nature [24].

process temperature and duration. The maximum temperature was varied between 250 and 360°C, and the hold time was varied between 1 and 20 min. The ramp rate was 120°C/min and the process was carried out in vacuum.

5.3. Main results

Our studies have shown that 5 min at 300°C is insufficient to complete the isothermal solidification process step for our configuration, showing unreacted Sn in the joint centre, see **Figure 11(a)**; 20 min at 300°C or 5 min at 360°C created a developed $Ni_3Sn/Ni_3Sn_2/Ni_3Sn$ joint structure, see **Figure 11(b)** and **(c)**. Bader et al. [25] have reported that 105 h at 400°C was necessary to completely homogenize a 2.6-μm thick Sn layer on Ni into an $Ni/Ni_3Sn/Ni$ structure. The intermetallic formation evolves by forming idiomorphic Ni_3Sn_4 crystals at the Ni/Sn interface. These crystals grow anisotropically into columnar structures extending across the joint. They have a significant impact on the mechanical compliancy of the joint, restricting its ability to conform to volumetric changes as the joint evolves. The phase transformation from liquid to the solid intermetallic phases causes a volumetric shrinkage of about 14–17%. The inability to conform causes a high intrinsic stress state within the joint. This may result in significant voiding as depicted in **Figure 11**. One way to overcome the problem of forming the large idiomorphic crystals restricting the joint compliancy would be to fabricate joints with an Ni-Sn paste. This would also significantly reduce the necessary process time to homogenize the bond [31]. Unfortunately, such pastes are per now not commercially available. The nominal

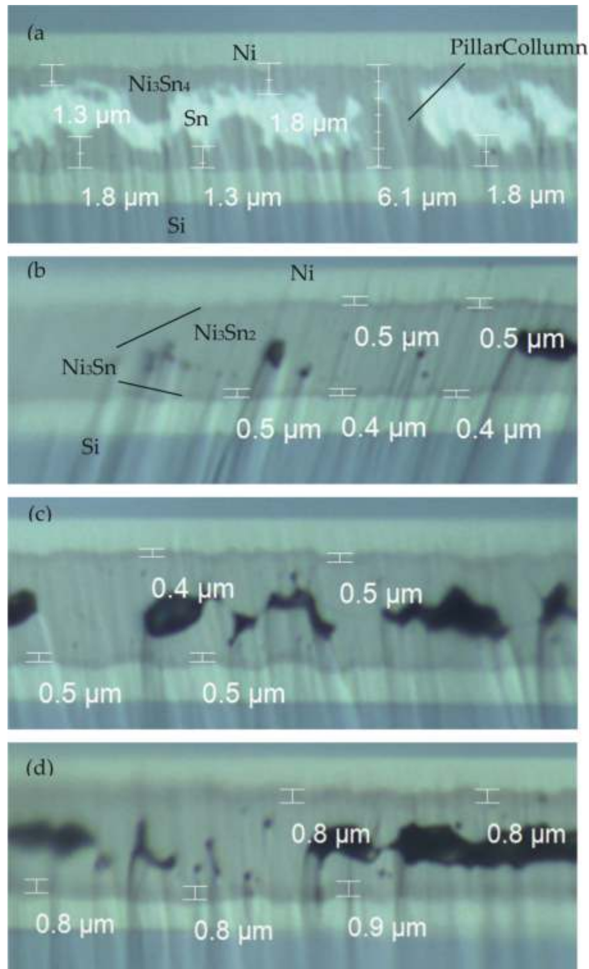

Figure 11. Optical micrographs of cross sections illustrating solidification and homogenization process for four different processes: (a) 1–300°C, 5 min, (b) 2–300°C, 20 min, (c) 3–360°C, 5 min, and (d) 4–360°C, 20 min [27] (© 2016 IEEE).

shear strength was measured to be at least 40 MPa according to the normal shear testing procedure. Greve et al. have demonstrated a shear strength capacity above 10 MPa at 600°C [31]. Fractography revealed that the strength was limited by a poor adhesion layer. Despite severe voiding in the joints themselves, they showed a significant shear strength exceeding 200 MPa when the actual bonded area was considered.

The pertinent literature has studied layered structures, either Ni/Sn/Ni or Ni/Sn. Both Sn preforms [26] and deposited layers have been used. The deposited layers have been electroplated [27, 28, 30], e-beam [32], thermally evaporated, sputtered [25, 32] or a combination of the abovementioned methods.

6. Au-In bonding

6.1. Rationale for Au-In

The Au-In system (**Figure 12**) has a high number of IMCs. Whereas In has a low melting point of 156°C, all IMCs are solid at 450°C and higher. This opens for the possibility of a low-temperature bonding process with the capability of high-temperature stability. A low-temperature bonding is important for temperature-sensitive materials and also to minimize thermomechanical stress generated in the bonding process. Au-In SLID bonding will allow applications in an extended temperature range, defined by the tolerance of the bonded materials, whereas In-based soldering can only be used for applications well below the melting point of In. Our work in Au-In SLID bonding is a feasibility work, demonstrating that wafer-level bonding with good strength is achievable and that the bonds survive temperatures much higher than the melting point of In.

6.2. Fabrication process

Au-In interdiffusion is significant already at room temperature, converting In to $AuIn_2$ [34, 35]. If a system is designed with metal layer thicknesses aiming for an Au/IMC/Au bond-line, similar to Sn-based SLID systems, all In may have been converted to $AuIn_2$ before bonding, leaving no liquid phase available during bonding. Therefore, we have used thin Au layers in our Au-In bonding. In was deposited by evaporation, allowing only thin-layer deposition. We selected Au-In thickness on one bonding partner as 0.16 μm/1.25 μm and the other bonding partner as 0.8 μm Au, as shown in **Figure 13**. Bonding was performed at wafer level.

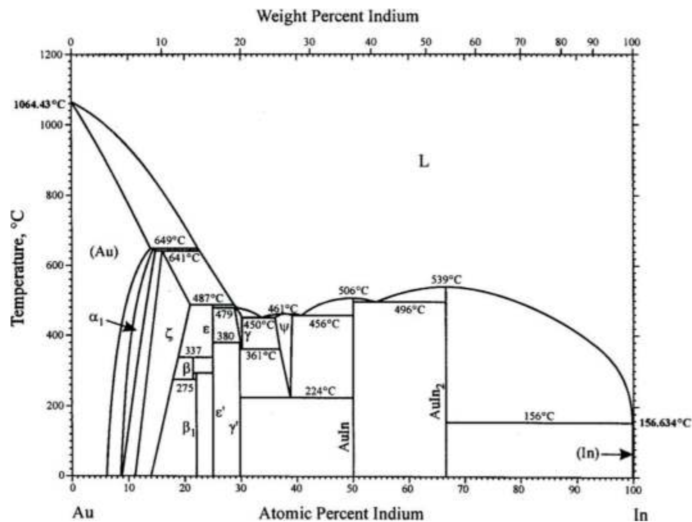

Figure 12. Au-In phase diagram. Reprinted with permission from Springer Nature [33].

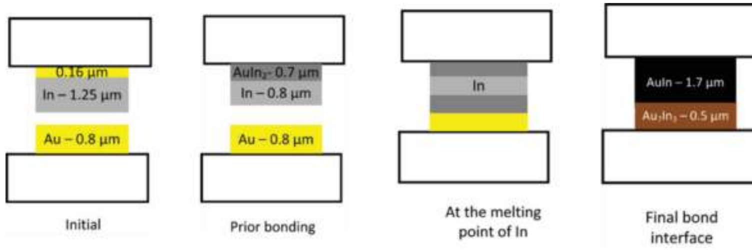

Figure 13. Design principle for Au-In SLID bonding.

6.3. Main results

Wafer bonding of Au-In was successful, with shear strengths in the range of 30 MPa [36]. **Figure 14** shows the microstructure of the final Au-In bond interface, where two IMC phases, AuIn and Au_7In_3, are present.

Shear testing at elevated temperatures, up to 300°C, confirms the high-temperature stability predicted from the phase diagram. **Figure 15** shows that the bond is solid at temperatures much higher than the In melting temperature of 156°C. Actually, the bond-line has a higher shear strength at 300°C than at room temperature. Inspection of the fracture surfaces reveals that die shear at temperatures from room temperature up to 200°C results in brittle fracture, with well-defined fracture surfaces: along the original bond interface, as well as in the adhesion layers. At 300°C, the fracture inside the IMC is very different. It has a ductile nature and no longer follows the original bond interface nor any other well-defined plane. The higher shear strength and change in fracture mode is explained from the phase diagram: a solid-state phase transition to the Ψ phase occurs at temperatures above 224°C. For our layer thicknesses, this phase transition involves interdiffusion of Au and In across the original bond interface, giving an annealing effect at this interface. When the weakest part of the bond-line is strengthened, an overall increase in strength is observed [36].

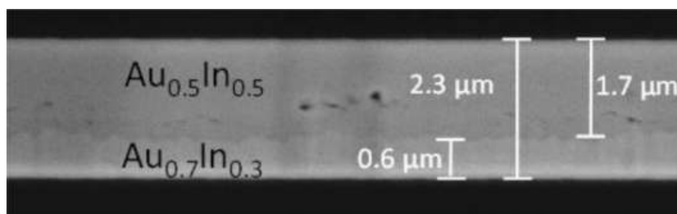

Figure 14. Cross section of the bonded sample. Two Au-In intermetallic compounds (IMCs) are present in the final bond-line. Reprinted with permission from Springer Nature [36].

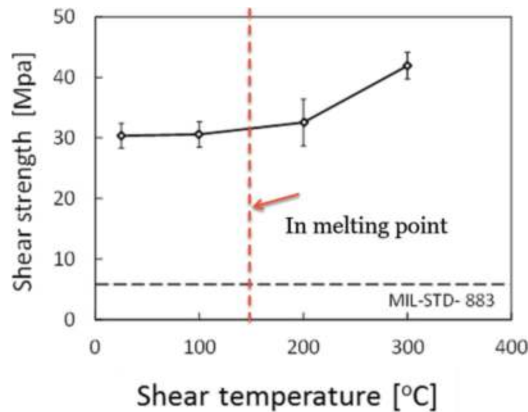

Figure 15. Au-In strength versus temperature.

7. Au-In-Bi bonding

7.1. Rationale for Au-In-Bi

While the use of In as a low-melting point material allows bonding at lower temperatures than ordinary solder temperatures, a number of applications and materials will require even lower bonding temperatures. Examples of temperature-sensitive materials are poled piezoelectric materials (that should not approach or exceed the Curie temperature, which can be ~150°C for a typical piezoelectric material such as PZT, lead zirconate titanate), ferromagnetic materials and polymers.

In-Bi is a metal system with particularly low melting points (see **Figure 16**): 72.7°C for the eutectic composition (78.5 at% In), and with all In-Bi intermetallic compounds having melting points within the range of 89–110°C. Ternary phase diagrams of the Au-In-Bi system are not readily available. However, Au and Bi are not miscible and have no IMCs that are stable at ambient temperatures. The lowest melting point of the Au-Bi system is a Bi-rich eutecticum (241.1°C). A suitable low-temperature bonding process may therefore be expected to result in Au-In IMCs, together with Bi, in the bond-line. The remelting temperature of such a bond will then be that of Bi (271°C). This will allow for a low-temperature bonding process without a severe restriction on the allowed temperature span in application.

7.2. Fabrication process

Most of our Au-In-Bi SLID bonds were carried out by sandwiching a eutectic In-Bi (78.5 at% In to 21.5 at% Bi) preform (thickness about 140 μm) between Au-coated dies and substrates. Bonding was performed with a bonding pressure ranging from 5 to 8 MPa, bonding temperatures ranging from 90 to 130°C and bonding times ranging from minutes up to 15 h [38]. Initial

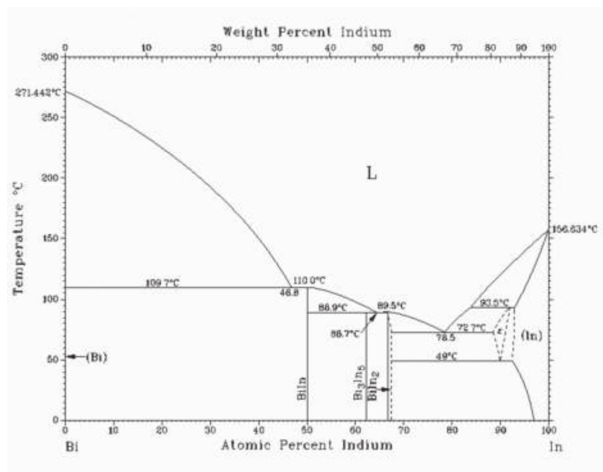

Figure 16. The Bi-In phase diagram. Reprinted with permission from ASM International [37].

experiments using a fast temperature ramp of 20°C/min gave a bond morphology with large scallops. All our main experiments are therefore carried out with a slow temperature ramp of 2°C/min, giving the desired layered SLID bond-line structure where the interdiffusion is controlled by IMC layers formed at the Au-to-preform interface already at temperatures below the melting temperature of the eutectic preform.

Au-In-Bi SLID bonding using thin-film (2.5–3 μm) thermally evaporated eutectic In-Bi on Au surfaces was also demonstrated [39]. This approach opens up for a much shorter process time, as well as being compatible with photolithographic patterning.

7.3. Main results

7.3.1. Phases obtained

7.3.1.1. Bonding at 90°C

Bonding at a low temperature of 90°C is indeed successful, as shown in **Figure 17**. The bond-line is much thinner than the original thickness of the In-Bi foil, showing that the material has been squeezed out while in liquid phase. The bond-line shows a layered structure of various Au-In IMCs, as well as inclusions of the $BiIn_2$ phase. No remaining In phase, no Au-Bi IMCs nor ternary Au-Bi-In phases are observed. $BiIn_2$ has a melting temperature of 89.5°C; hence, a higher process temperature is needed to obtain the desired, higher remelting temperatures.

7.3.1.2. Bonding at 110°C

Figure 18 shows cross-section micrographs of the bonding performed at 110°C.

The cross-sections show a layered morphology similar to **Figure 17** (bonding at 90°C), but with thicker layers of the more Au-rich IMCs AuIn and Au_7In_3. No In-Bi IMCs are observed,

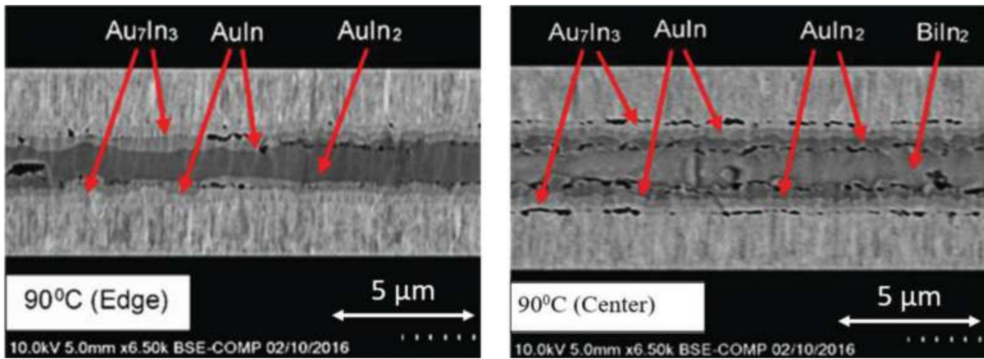

Figure 17. Cross-section micrograph of In-Bi SLID bond on Au pads, bonding temperature of 90°C, temperature ramping rate of 2°C/min and bonding time of 4.5 h. The phases are identified by EDX [38] (© 2016 IEEE).

but inclusions of Bi. This indicates that this bond would have a remelting temperature of 271°C. The existence of Bi as opposed to $BiIn_2$ (which appears in the 90°C-bonded samples) is explained from the Bi-In phase diagram: as the Au-In IMCs grow during the bonding process, the liquid Bi-In is gradually depleted of In and the Bi content rises. If the temperature of the liquid is below 89.5°C, $BiIn_2$ will solidify isothermally as the Bi content in the liquid approaches 33 at%. If the temperature of the liquid is between 89.5 and 110°C, $BiIn_2$ is not stable, and BiIn will solidify isothermally as the Bi content in the liquid approaches 50 at%. For temperatures above 110°C, no Bi-In IMCs are stable, and Bi will solidify isothermally as the In content in the liquid is depleted. The bonding temperature has a finite precision, so a bonding temperature set to 90°C may easily be consistent with a liquid temperature below 89.5°C, and similarly a bonding temperature set to 110°C may easily be consistent with a liquid temperature above the melting point of BiIn.

A bonding temperature of 110°C is marginal if one wishes to avoid the presence of the low-melting Bi-In IMCs. In our later work, we have therefore bonded at 115°C.

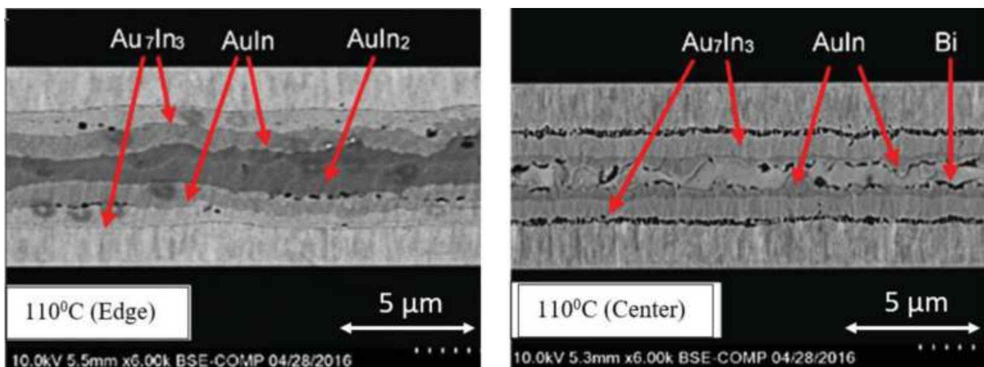

Figure 18. Cross-section micrograph of In-Bi SLID bond on Au pads, bonding temperature of 110°C, temperature ramping rate of 2°C/min and bonding time of 4.5 h. The phases are identified by EDX [38] (© 2016 IEEE).

7.3.1.3. Bonding at higher temperatures and/or longer bonding times

For samples bonded at a higher temperature (120 and 130°C) and/or bonding times longer than 4.5 h, the bond-line morphology is similar to that of the sample bonded at 110°C (**Figure 18**), except that the Au_7In_3 layer is significantly thicker and the $AuIn_2$ layer thickness is much reduced. This is as expected, with increased Au-In interdiffusion.

For extended bonding/annealing times, we expect an entire conversion to Au_7In_3, in an Au/Au_7In_3/Au configuration, when the Au:In ratio allows for that. Further reactions to even more Au-rich IMCs can be expected in order to reach thermal equilibrium, but the kinetics of these reactions is not known.

7.3.1.4. Bonding using thin-film deposited In-Bi

The Au-In-Bi preform SLID bonding discussed earlier requires long bonding times, due to slow diffusion through Au-In IMCs at these low bonding temperatures. Our preliminary experiments with thin-film-deposited In-Bi show that similar bond morphologies can be obtained, with decreased bonding times [39].

7.3.2. Characterization

Solid bond strengths, up to 50 MPa, are recorded. Bonded, acoustically active materials are tested with electrical impedance spectroscopy, confirming a very limited amount of voiding, compatible with ultrasonic applications [39].

8. Conclusion

8.1. Summary of USN results on different SLID systems

Table 2 compares the different SLID systems that our group has worked with and what has been our group's research focus for each system. The obtained bond strength is a good indication of the quality of the bond. For all SLID systems, we obtain shear strength at the level of or higher than when using Sn-based solder (typically around 30–40 MPa [40, 41]). The highest bond strength is obtained by Au-Sn. This system will not show significant oxidation of the metal layers prior to bonding. This assures good wetting of the bonding partners, and a bond with very limited voiding has been the result.

Figure 19 shows the shear strength versus temperature of Au-Sn, Cu-Sn and Au-In bonding systems. All systems show solid bonds at temperatures higher than the melting temperatures of In (156°C) and Sn (232°C), experimentally verifying the predicted high-temperature stability [42]. For Au-Sn, a solid bond at 400°C is also shown [43], without quantification. For Au-In-Bi SLID, a solid bond at 115°C is demonstrated, although a destructive test to quantify the bond strength has not been performed.

All SLID systems survived the highest tested temperature; we have not quantified the actual remelting temperature for any of these.

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	Cu-Sn	Au-Sn	Ni-Sn	Au-In	Au-In-Bi
USN contributions	Flux-free, wafer-level bonding for hermetic sealing Simulation model for IMC kinetics Industrial implementation Strength versus temperature	Composition determined Excellent reliability (HTS and TC, also with CTE mismatch) Strength versus temperature	Bond demonstrated and characterized	Bond demonstrated and characterized Strength versus temperature	Bond demonstrated and characterized (mechanically and acoustically)
Process temperature	>232°C	>278°C	>232°C	>156°C	>73°C
Obtained bond strength	70 MPa	140 MPa	>40 MPa (nominally) > 200 MPa in the actually bonded areas	30 MPa (breaking at bond interface) 40 MPa at 300°C	50 MPa

Table 2. Different SLID material systems.

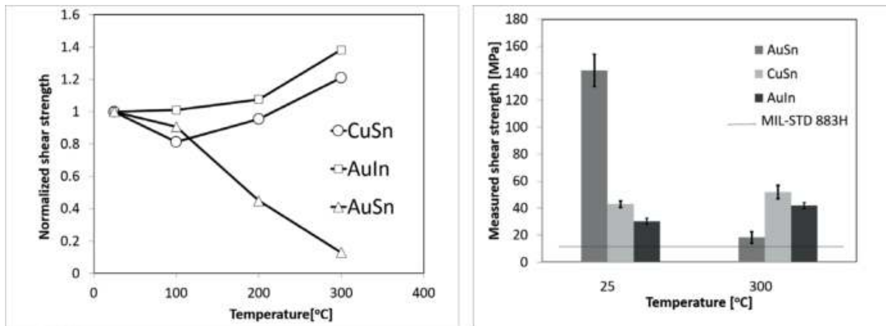

Figure 19. Normalized shear strength versus die shear temperature and actual shear strength at RT and 300°C [42] (© 2014 IEEE).

The temperature behaviour of the three SLID systems shown in **Figure 19** is rather different. For Cu-Sn, the variations in the shear strength with temperature are rather small, as might be expected since the phase diagram shows no phase transitions occurring in the Cu/Cu_3Sn system below 350°C. Au-In shows a remarkable increase in strength at 300°C, explained earlier by a solid-state phase transformation occurring above 224°C. With the layer thicknesses in our design, this gives rise to interdiffusion across the initial bond interface, which was the weakest point in the bond-line at room temperature [36]. Au-Sn shows decreasing strength with temperature, but is solid at temperatures above the eutectic temperature in the Au-Sn system (278°C). The IMC in our Au-Sn SLID bonds is the non-stoichiometric ζ phase, which has a very composition-dependent melting temperature (ranging from 278 to 522°C, see **Figure 4**). We propose that more Au-rich Au-Sn SLID bonds with a longer bonding time, where the β

phase is the resulting IMC, will have the potential of even better high-temperature performance [44]. Note, however, that even though the relative decrease in Au-Sn shear strength is significant, the room temperature strength is extraordinarily high. Even though the strength of this system is reduced at 300°C to a level lower than the two other material systems, it is still at an acceptable level (~3× MIL-STD).

8.2. Related work

Many groups have contributed to research in SLID (**Table 3**). Most work has been on the Cu-Sn system, with Au-Sn as the second-most studied system.

Huebner et al. [3] demonstrated in 2006 that Cu-Sn SLID was capable of producing fine-pitch interconnections, down to 30 μm. This is significantly finer pitch than what can be obtained by a standard solder process. Lannon et al. [45] in 2012 showed the applicability of Cu-Sn SLID for high-density bonding with a very high number of interconnections (>22,000). In recent years, the industry in need of fine-pitch interconnection has implemented 'Cu pillar technology', where the pitch can be less than 10 μm [46], by electroplating fine-pitch Cu pillars (with diameters down to 1 μm [47]) and restricting the solder applied to a small volume

Author(s)	Ref.	Main contribution
Bernstein (and Bartholomew)	[9, 10]	First introduction of SLID, for bonding in microelectronics, in 1966
Huebner et al.	[3]	Cu-Sn SLID for early (2006) fine-pitch (<30 μm) interconnection
Lannon et al.	[45]	Cu-Sn SLID (2012) high-density interconnections (>22,000 interconnects)
Huang et al.	[46]	Solder-capped Cu pillars (fine-pitch technology where the material composition is similar to Cu-Sn SLID)
Liu et al.	[47]	Solder-capped Cu pillars with extreme fine-pitch (down to 1 μm)
Huang et al.	[48]	Metastable SLID: Cu-Sn SLID process not reaching thermal equilibrium, faster process time
Syed-Khaja and Franke	[49]	Solder paste used for Cu-Sn SLID
Vuorinen et al.	[50–52]	Au-Sn and Cu-Sn SLID, dynamics of bonding and of void formation
Ross et al.		
Nga et al.	[53, 54]	Cu-Sn SLID, hermetic sealing of MEMS devices and for through-silicon vias (TSVs)
Yuhan Cao et al.		
Marauska et al.	[55, 56]	Cu-Sn and Au-Sn SLID
Xu et al.		Wafer-level hermetic encapsulation
Chang et al.	[57–60]	Cu-Sn SLID for 3D integration
Civale et al.		
Chang et al.		
Ko et al.		
Cook and Sorensen	[5]	Overview article (2011)

Table 3. SLID and related work, examples from various groups.

on top of the Cu pillars. Although usually referred to as a solder process, the process is very similar to a SLID process because of the small Sn volume applied and a resulting bond-line dominated by intermetallics.

Huang et al. [48] have developed 'Metastable SLID', where an Ni barrier layer restricts the amount of Cu to be used for the reaction with Sn, resulting in a SLID bond with Cu_6Sn_5 as the IMC. This allows for a much faster processing time, while a number of the desired properties of SLID are intact.

Alternative methods for depositing Sn in the Cu-Sn SLID/ TLP system are explored, for example, by using Sn-based solder paste [49].

Vuorinen et al. [50] have investigated Au-Sn and Cu-Sn SLID, with a special focus on the mechanisms of the dynamic evolution during bonding and the corresponding void formation [51, 52].

Although solder bonding is likely to be the most used bonding method also in the future, SLID bonding is likely to be increasingly important for industrial applications where high-temperature performance or fine-pitch metallurgical bonding is important.

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