MIMO System Implementation for WSN Using Xilinx Tools

Wael M El-Medany
University Of Bahrain
Bahrain

1. Introduction

Wireless sensor networks are one of the most rapidly evolving research and development fields for microelectronics. Their applications are countless, and the market potentials are huge. However, many technical hurdles have to be overcome to achieve a widespread diffusion of wireless sensor network technology [1].

This work presents the design and FPGA hardware implementation of a *Multiple-Input/Multiple-Output (MIMO)* system for Wireless Sensors Networks (WSN). This system will offer *more parallel channels between the sensor nodes and the base station at the same frequency band, thereby increasing spectral efficiency.* The hardware design of the MIMO wireless sensor network system has been described using VHDL (VHSIC Hardware Description Language). The design has been simulated and synthesized using Xilinx ISE 10.1i software tools, then tested in hardware level using Xilinx FPGA. The design offers remote monitoring system with MIMO wireless sensor network.

Sensor networks differ from traditional networks in several ways, sensor networks have severe energy constraints, redundant low data rate, and many-to-one flows. The end-to-end routing schemes that have been proposed in the literature for mobile ad-hoc networks are not appropriate under these settings [2]. A wireless sensor network has important applications such as remote environmental monitoring and target tracking. This has been enabled by the availability, particularly in recent years, of sensors that are smaller, cheaper, and intelligent. These sensors are equipped with wireless interfaces with which they can communicate with one another to form a network.

The design of a WSN depends significantly on the application, and it must consider factors such as the environment, the application's design objectives, cost, hardware, and system constraints [3]. WSNs have great potential for many applications in scenarios such as military target tracking and surveillance [4, 5], natural disaster relief [6], biomedical health monitoring [7, 8], and hazardous environment exploration and seismic sensing [9].

Mobile Ad-Hoc and Wireless Networks Evolving Mobile Network concept known as Multiple-Input/Multiple –Output, which has the potential to increase communications data rates by 10-20 times above current systems data rates. Such systems can use reprogrammable logic circuits, specifically Field Programmable Gate Arrays (FPGA), which offers a cost effective and high performance hardware alternative to Application Specific Integrated Circuits (ASIC) in low and mid volume products. Furthermore, FPGAs are becoming important building blocks in embedded systems design [10]. Nowadays many system designs that used to be built in custom silicon VLSI [11] are now implemented in Field Programmable Gate Arrays. This is because of the high cost of building a mask production of a custom VLSI especially for small quantity [12]. In addition to the cost effective, FPGA gives large number of inputs and outputs. The problem with FPGA was that it is volatile; this means that once the power is switched off, the design will be erased, but this problem has been recently solved by the use of the first non-volatile FPGA that has been introduced by Xilinx in 2007, that is Xilinx Spartan 3 AN. The Spartan 3 AN FPGA has a flash memory built on the chip, which keep the design even when the power is off.

With the rapid development of computer technology, the monitored control design of the wireless sensor networks is becoming the core of the design for building automation system [13, 14]. Real-time monitoring provides reliable, timely information of petroleum product's status, important in taking decisions for petroleum production improvement. Evaluation of petroleum production systems is a time consuming and difficult process because it means performing visits to selected petroleum fields to be able to measure and register certain physical, chemical and biological characteristics of the petroleum production areas [15]. For remote monitoring, GSM network has been used for remote communications [16-19].

This research introduces a MIMO wireless sensor networks for a petroleum fields that has a large number of parallel channel offered by Xilinx FPGA for the communications with the wireless sensor nodes, in order to read the data simultaneously from the sensor nodes. The target technology is XC3S1400 AN-5fgg676, which has 676 pines on the package; the design has been synthesized and implemented using Xilinx ISE 10.1i.

2. MIMIO-WSN system architecture

A multiple-input / multiple-output wireless sensor networks system architecture comprising N wireless sensor node and transceiver systems, where N is (I*J) sensor node matrix. There are I-groups of sensor node, each group comprising J-sensor nodes, and each group is communicating with the base station through a communication channel, with a total of I-communication channel. There are I-sensor nodes that can communicate in parallel with the base station through the I-communication channel. At the same time there are I-transceiver antennas at the base station. Figure 1 shows a block diagram for the system architecture of the multiple-input / multiple-output wireless sensor networks. The main controller for the base station has targeted the Xilinx XC3S1400 AN-5fgg676 FPGA, which can be programmed with a design that contains up to 1.4 million of logic gates, with a package of 676 input/output pines.

Around 600 pines from the 676 pines of the FPGA package are available for user applications. Those large numbers of input/output pines are used to increase the number of parallel communication channels. For each channel there are two pines that are required for the communications, one for the data transmit and the other for the data receives. This means that we have up to 300 communications channel, and thereby the number of base station transceiver is also 300, which means that the (I) rows of the sensor node array can be increased up to 300. The VHDL top-level model of the main controller in the base station is shown in figure 2, where Rx1, Rx2,…., and Rx300 are the receiver end of the base station, and Tx1, Tx2,… , and Tx300 are the transmitting end. In accordance there are 300 UART

(Universal Asynchronous Receiver Transmitter) in the main controller of the base station. The UART has been designed using VHDL as a component, and implemented on the FPGA.

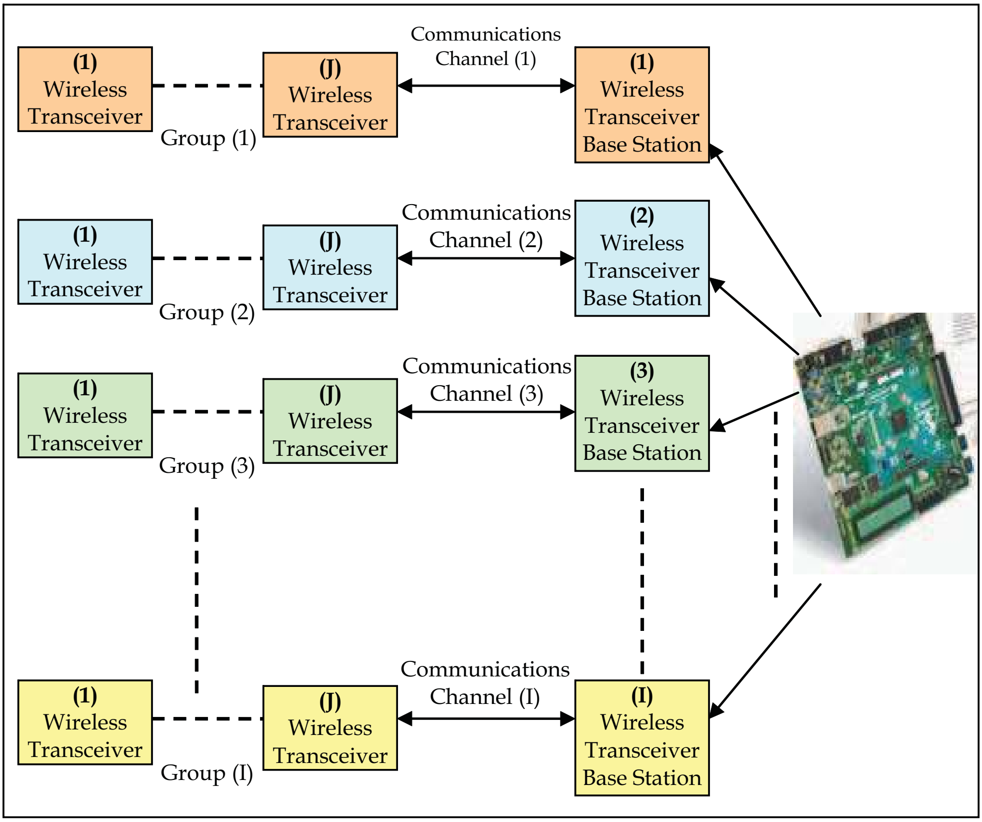

Fig. 1. IMIO-WSN System Architecture

A sensor node is a multi-functional unit performing many different tasks, from managing acquisition to handling communication protocol schedule and preparing data packets for transmission, after filtering, synchronizing and signal processing on data gathered from sensors. Thus, each sensor node requires processing and storage capabilities. Figure 3 shows a block diagram for the main components of the sensor node, there are six units in each of the sensor nodes. The most important unit of the sensor node is the processing unit, which has the main controller of the sensor node. The processing unit handle all the arithmetic and logical operations, receiving data from the ADC, storing data, sending data to the network protocol through the communications unit. The communication unit is a UART, and the sensing unit is changing according to the application, they have a variety of sensing devices, including security and pressure sensing devices and cameras.

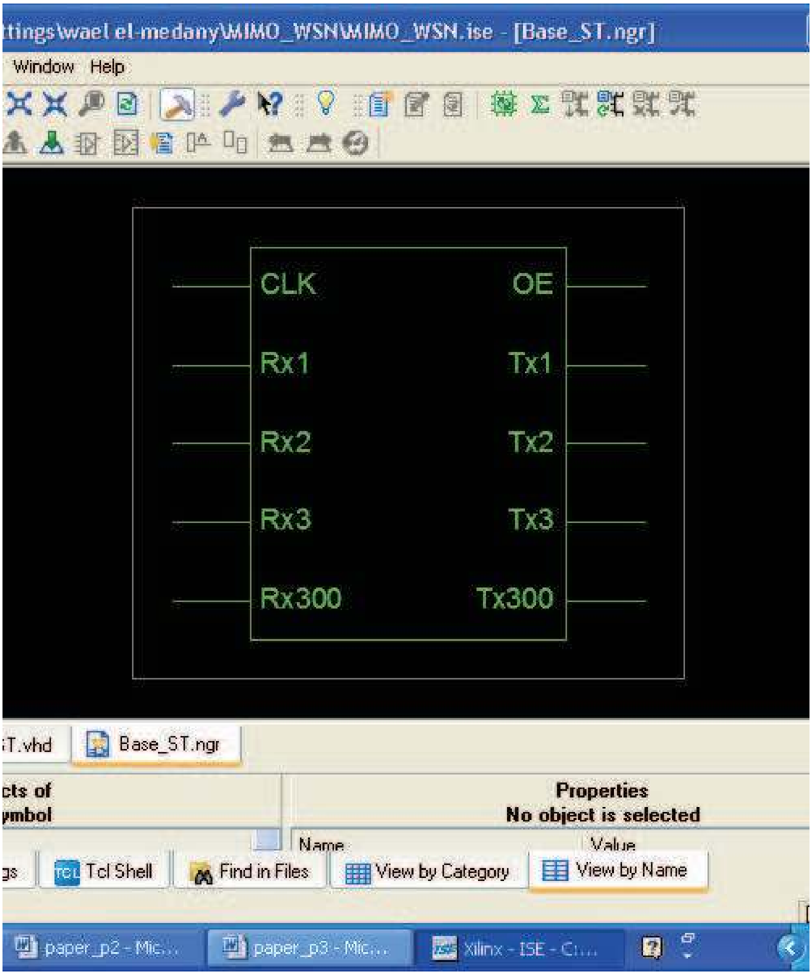

Fig. 2. VHDL Top-Level Design Model

3. Simulations results and efficiency

The VHDL models have been simulated functionally to verify the correctness of the behavioral description for the models. Figure 4 shows the simulation results for the processing unit in the sensor node. Where “clk” is the system clock input, “TS” is an input bit-vector of 8-bit which represents the inputs from the sensing unit. Where the analog value from the sensing unit has to be converted to digital value in binary representation using the ADC; this binary value is represented by “TS” input. This part of the sensor node has been tested using Spartan 3 starter kit from Xilinx, which has four seven segment digits built on the board, the four seven segments are common anodes, and the cathodes for the four seven segments are connected together in parallel. To display an output, you have to do a multiplexing between the four seven segments. The signal "SSCATH" in figure 4 is the

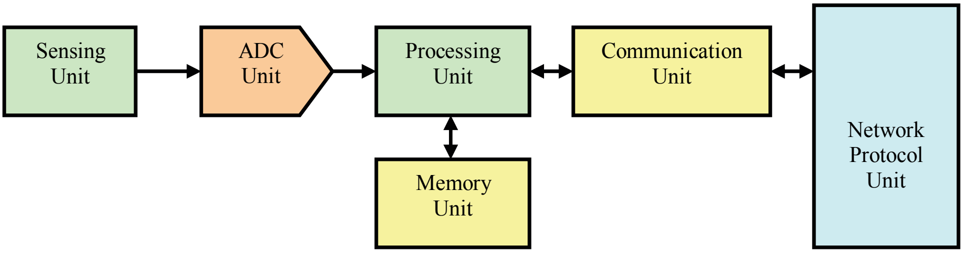

Fig. 3. Block diagram for the main components of the sensor node

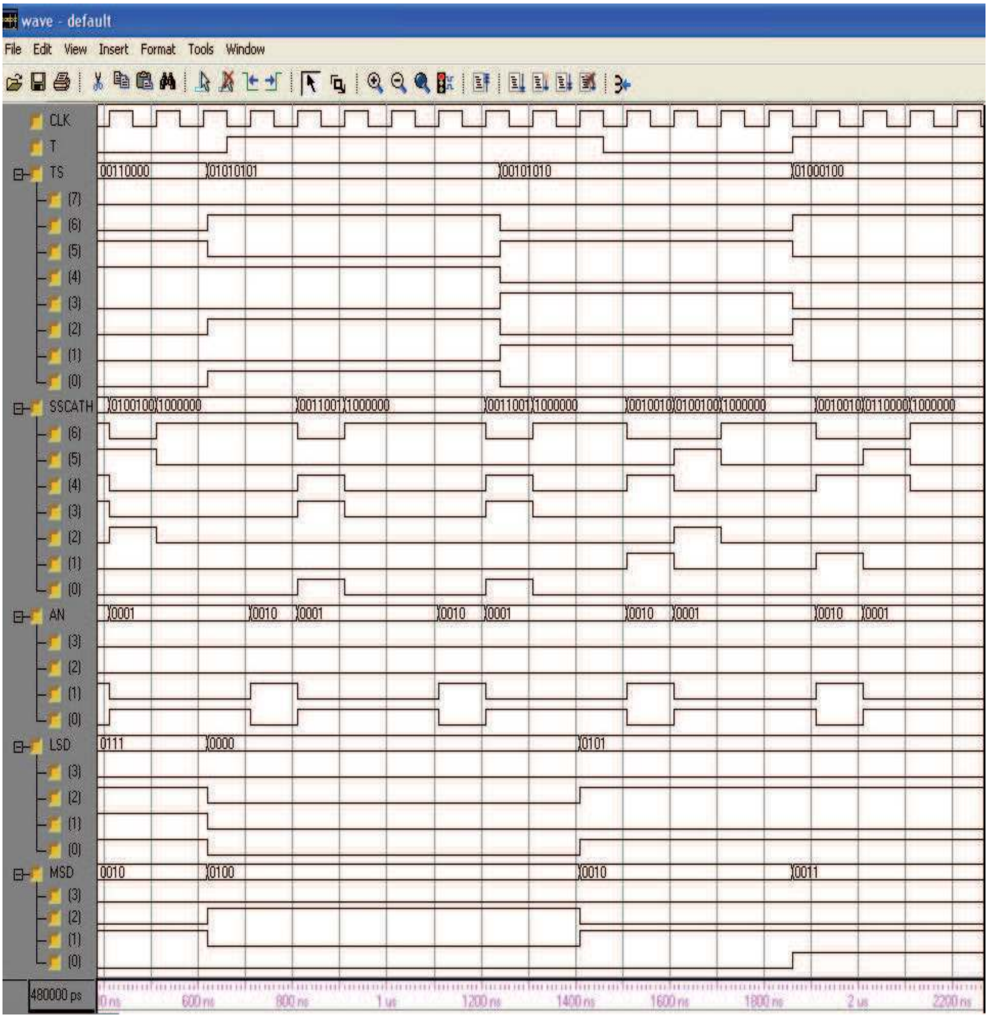

Fig. 4. Simulation results for the Processing Unit in the Sensor Node

cathode output for the seven segment display on the system board, and "AN" is the anode output for the seven segment, it is four bits that representing four digits, but only two of them are used. The values on "AN" represent the multiplexing between the seven segment digits, and the values on "SSCATH" represent the seven segment code for the decimal value. The signal “LSD” and “MSD” are internal signal that representing the two BCD (Binary Coded Decimal) digits of the senor reading. Where "LSD" is least significant digit and "MSD" is most significant digit. Signal "T" is an output signal that indicates the high sensing input and normal input. Figure 5 shows the simulation for the multiplexing between different sensor nodes in the base station. Where “TSC” and “HSC” are two 8-bit inputs from the analog to digital converter of the two Sensing Circuits, “Sel” is the selector input, and “Q” is an 8-bit output of the multiplexer. If (Sel=’0’) then (Q = HSC), and if (Sel=’1’) then (Q = TSC). The selector “Sel” is changing sequentially using binary counter. The MSB of TSC, HSC, and Q are on the left, whether the LSB (Least Significant Bit) are on the right. The increased number of parallel communications channel and multiplexing the inputs of the base station system give high efficiency to our system compared to other system in the literature, as well as reducing cost by using the FPGA devices.

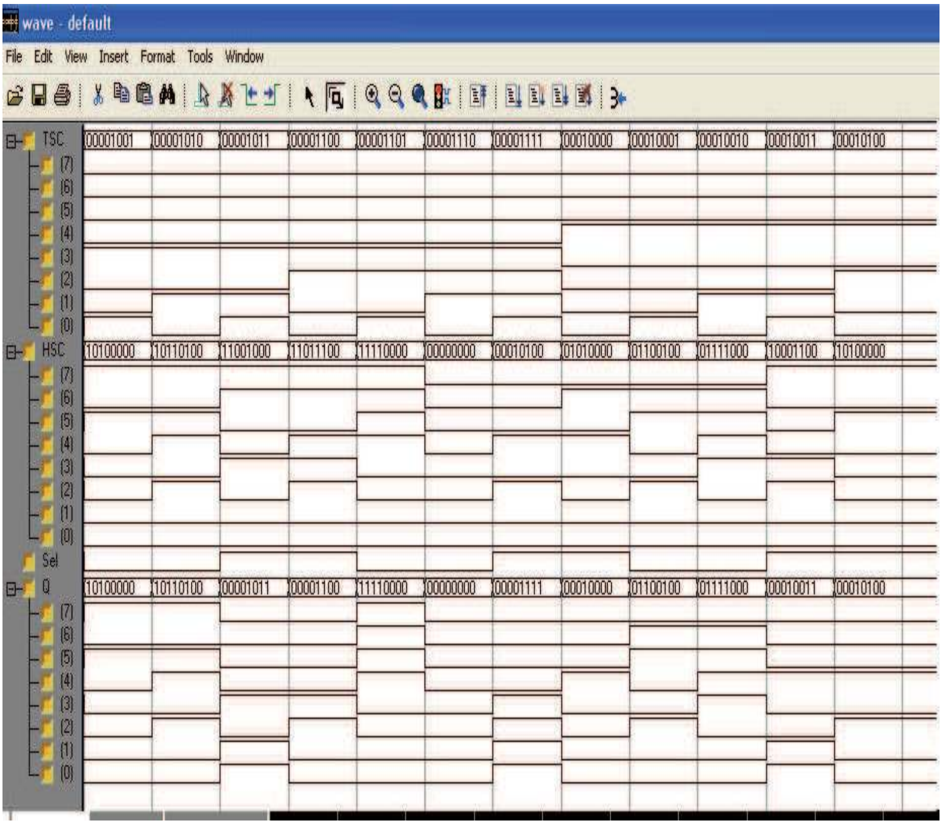

Fig. 5. Simulation results for the multiplexing between different sensor nodes in the Base Station

4. Conclusion

A hardware design and FPGA implementation of a Multiple-Input/Multiple-Output system for Wireless Sensors Networks has been introduced in this paper. The system has increased the number of parallel channels and hence the number of sensor nodes. The system uses the large numbers of Inputs/Outputs pines offered by the FPGA chip to increase the number of parallel channels between the base station and the sensor nodes. The system was designed using VHDL in a high level design method. All parts of the design have been tested in both simulation and hardware level. The implemented design targeted the non-volatile Xilinx XC3S1400 AN-5fgg676 FPGA for final prototype.

5. References

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In recent years, it was realized that the MIMO communication systems seems to be inevitable in accelerated evolution of high data rates applications due to their potential to dramatically increase the spectral efficiency and simultaneously sending individual information to the corresponding users in wireless systems. This book, intends to provide highlights of the current research topics in the field of MIMO system, to offer a snapshot of the recent advances and major issues faced today by the researchers in the MIMO related areas. The book is written by specialists working in universities and research centers all over the world to cover the fundamental principles and main advanced topics on high data rates wireless communications systems over MIMO channels. Moreover, the book has the advantage of providing a collection of applications that are completely independent and self-contained; thus, the interested reader can choose any chapter and skip to another without losing continuity.

InTech Europe
University Campus STeP Ri
Slavka Krautzeka 83/A
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Phone: +385 (51) 770 447
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InTech China
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中国上海市延安西路65号上海国际贵都大饭店办公楼405单元
Phone: +86-21-62489820
Fax: +86-21-62489821