Design Techniques for Microwave and Millimeter Wave CMOS Broadband Amplifiers

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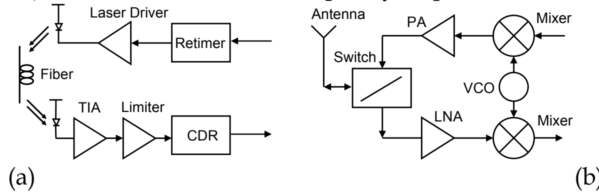
1. Introduction

The microwave and millimeter wave broadband amplifier is one of the key circuit blocks for high-speed optical communication systems. It is also of extreme importance for wideband wireless communications operating within microwave frequency range. Previously reported results were mostly designed using compound semiconductor III–V (Majid-Ahy et al., 1990; Masuda et al., 2003; Shigematsu et al., 2001) or SiGe (Mullrich et al., 1998; Weiner et al., 2003) technologies to take advantage of the superior transistor characteristics. Lately, CMOS technology with continuously scaled feature sizes attracts much attention of circuit designers for wideband amplifier applications owing to the impressive cut-off and maximum oscillation frequencies (Chan et al., 2008). Considering the requirements of modern integrated circuit design such as low cost, low power consumption, and high integration level with other circuit blocks, CMOS technology is of great potential for microwave and millimeter wave broadband amplifier applications.
This chapter provides the fundamental design concepts of broadband amplifier using the modern CMOS technology. Various design techniques are introduced for achieving high performance microwave broadband amplifiers. The main design considerations and current trends are also discussed. We will give a brief overview about the applications of broadband amplifiers and background information in section 1. Section 2 discusses the considerations of transistors and inductive components in standard CMOS process for broadband amplifier design. Section 3 reviews different design techniques for broadband amplifiers with an emphasis on the inductor peaking technique. The bandwidth enhancement ratio (BWER) of each approach is calculated. In section 4, recent advances on CMOS broadband amplifier design for microwave applications are reported. We propose a pi-type inductive peaking (PIP) technique to realize a 40 Gb/s transimpedance amplifier (TIA) in 0.18-μm CMOS technology (Jin & Hsu, 2008). We also propose an asymmetrical transformer peaking (ATP) technique to achieve a miniaturized 70 GHz broadband amplifier in 0.13-μm CMOS technology (Jin & Hsu, 2008). The core area is only ~ 0.05 mm^2 and the Gain-Bandwidth Product (GBP) is up to 231 GHz which is among the highest compared with other reported works with similar or even more advanced technologies. Finally, section 5 provides the closing remarks of this chapter and also some recommendations of further study on CMOS broadband amplifiers for microwave and millimeter wave applications.

1.1 Applications of microwave and millimetre wave broadband amplifiers

The block diagram of a typical fiber-optic communication system is shown in Fig. 1(a). In the transmitter side, the laser driver (LD) amplifies the signal to modulate the laser diodes for converting the electrical signal to optical signal. In the receiving end, a photo detector converts the weak optical signal that transmits through the fiber back to the electrical signal, followed by a transimpedance amplifier (TIA) and limiting amplifier (LA) to amplify the photo current. Among the front-end circuit blocks in a fiber-optic communication system, the LD, TIA, and LA are all broadband amplifiers. Currently, the data rate of the system increases from 10-Gb/s (OC-192) to 40-Gb/s (OC-768) or even up to 80-Gb/s (OC-1536), and the demands increase as well for these amplifiers with a bandwidth up to microwave and millimeter frequency range.

Another main application of broadband amplifiers is for wireless communications. The concept of broadband communication is to transmit the data in a certain bandwidth such that the data rate can increase and the emitted power can reduce. The wider the bandwidth, the greater the information-carrying capacity. There are some specific bands for the broadband communications such as multichannel multipoint distribution service (MMDS, 2-3 GHz), worldwide interoperability for microwave access (WiMax, 2-11 GHz), ultra-wide band (UWB, 3.1-10.6 GHz and 57-64 GHz), and radio astronomy (9 KHz-275 GHz). A typical block diagram of a wireless communication system is shown in Fig. 1(b). For broadband applications, the two front-end amplifiers including the low noise amplifier (LNA) and the power amplifier (PA) both have a wideband frequency response.



(a) (b)

Fig. 1. (a) Block diagram of a typical fiber-optic communication system (b) block diagram of a typical wireless communication system.

2. Design considerations for CMOS broadband amplifiers

2.1 MOS transistors

Transistors play an extremely critical role in microwave circuit design, since the circuit consists of only a few transistors in most cases. Figure 2 shows the small-signal model of a MOSFET, where R_g is the poly gate resistance and R_s is due to the junction resistance. The four terminals are gate (G), drain (D), source (S), and body (B). The gate-source capacitance C_{gs} and gate-drain capacitance C_{gd} are important to the high frequency response of the transistor. The capacitances C_{sb} and C_{db} represent the paracitic capacitances of the body node to the source and drian terminals, respectively.

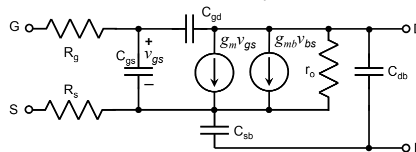


Fig. 2. Equivalent circuit model of a MOS transistor.

By neglecting the source parasitic resistance and the second order effect from the body node, the unity current gain cut-off frequency f_T and maximum oscillation frequency f_{max} of a transistor can be expressed as:

$$f_T = \frac{g_m}{2\pi(C_{gs} + C_{gd})} \tag{1}$$

$$f_{max} = \frac{f_T}{2\sqrt{(R_g)(g_{ds} + 2\pi f_T C_{gd})}} \tag{2}$$

where g_m is the transconductance and g_{ds} is the output conductance ($1/r_0$). According to the equations, the resistive and capacitive parasitics are the main limitation of the transistor f_T and f_{max}, which can be minimized through the transistor layout and selection of transistor geometry. In general, the gate resistance R_g can be reduced by employing the transistors with a multi-finger topology and a short width of each finger. The gate width Wg of each finger typically used is in a range of 1 to 3 μm for RF design if f_{max} is the major design consideration. A large finger number n can increase the transconductance for high-gain amplifier design, while f_{max} reduces with the increased total gate width due to the increase of parasitics. Note that f_T is relatively less sensitive to the increased finger number since the increase of g_m compensates the additional parasitic capacitances. Figure 3 shows the f_T and f_{max} of 0.13-μm NMOS as functions of W_g and n based on the foundry provided transistor model. As shown in the figure, the transistors of a longer W_g (5 μm) have higher f_T compared to that of a shorter W_g (1.2 μm) with the same n, which can be attributed to the increase rate of g_m is higher than that of the parasitic capacitances as W_g increases from 1.2 μm to 5 μm. It can also be observed that f_T does not increase significantly with n. On the other hand, the transistors with a shorter W_g present higher f_{max} resulting from the lower gate resistance R_g, smaller output conductance g_{ds}, and also the lower C_{gd} (under the same n). As the total finger number increases, f_{max} decreases significantly mainly due to the increased parasitic capacitance C_{gd} and output conductance g_{ds}.

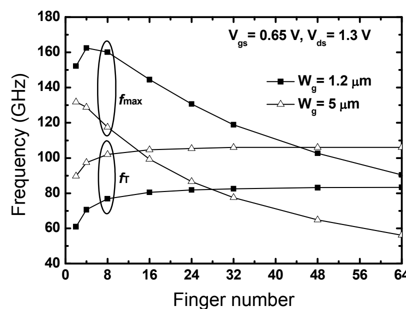
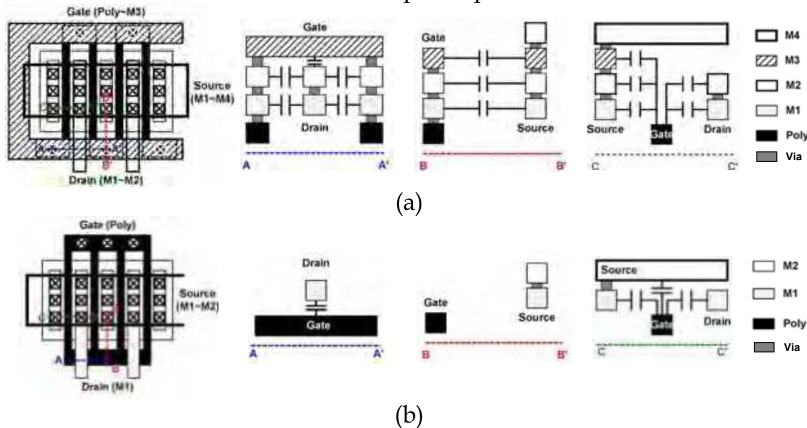


Fig. 3. Transistor (0.13-μm NMOS) f_T and f_{max} as functions of the finger width W_g and finger number n. (W_g= 1.2 μm and 5 μm)

The parasitics can also be reduced by the interconnect layout in the transistors. The wiring effect could be significant on the corresponding parasitic capacitances and resistances

especially for advanced technology with a small feature size (Chan et al., 2008). For transistors with a small gate length such as 65 nm, the parasitics originated from the transistor interconnects are critical to the overall frequency response. By changing the source, drain and gate interconnects in the transistor, the capacitive and resistive parasitics can be reduced effectively leading to improved cut-off frequency f_T and maximum oscillation frequency f_{max}. For example, we propose using the ring-type gate structure and the reduced number of interconnect layers in 65 nm N-MOSFET. The f_T and f_{max} are improved up to 21% and 22% respectively without changing any process steps. Figure 4 shows the comparison of the typical layouts using the meander-type gate with four interconnect metal layers (M_1~ M_4) from the foundry and the proposed transistor layout with the ring-type gate and only two interconnect layers (M_1~ M_2). The corresponding cross sections are also presented as indicated in the figure (*A-A′*, *B-B′*, and *C-C′*). As can be seen, the minimized metal interconnect layer can significantly reduce the sidewall parasitic capacitances and the via induced parasitic resistances leading to improved f_T and f_{max}. The improved transistor characteristics are beneficial to broadband amplifier performance.



(a)

(b)

Fig. 4. Transistor layouts and the corresponding corss sections (a) typical foudry provided layout (b) proposed layout approach. The sidewall parasitic capacitances and the via induced parasitic resistances are both reduced in (b).

2.2 Inductive components

Compared with the low frequency amplifers using analog circuit design approaches, one major difference for microwave amplifiers is the use of inductive passive components. In general, the inductive components are utilized for the matching network in microwave circuits. In addition, with inductive components, the parasitic capacitances which limit the high speed operation of a MOSFET can be resonated out to achieve wideband characteristics. For CMOS IC design, the inductive components such as inductors and transformers are usually designed as a spiral shape to maximize the inductance while minimize the chip area. Design of spiral inductor mainly considers the width w of the line, spacing s between the lines, and the metal thickness t. The foundry often provides a thick top metal layer for high Q inductor design, which has a range around 2 μm to 3 μm. The spacing is limited by the technology, and the minimum value is usually employed for high inductance and small chip area. The minimum width of the metal line is also limited by the technology. The consumed

chip area reduces if using a small *w*, whereas the parasitic resistance could increase and the inductor quality factor (*Q* factor) could drop. For a wider line, a higher *Q* factor may be achieved, but the parasitic capacitance could limit the operation frequency. Figure 5 compares the square and octagonal inductors for the inductance and *Q* based on EM simulations. With the same chip area (100 μm× 100 μm), the octagonal design has a slightly smaller overall length and thus a smaller inductance. The octagonal design also has less resistive parasitics resulting in a higher *Q*. Note that the square type inductor is more suitable for wideband applications owning to its lower *Q* and therefore a wider bandwidth for LC resonance.

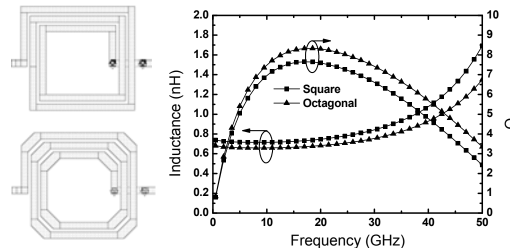


Fig. 5. Comparison of spiral inductors with two diffent shaps. (*w*= 4 μm, *s*= 2 μm, *t*= 2.3 μm, inner diameter= 40 μm)

On-chip transformers are also widely used for microwave and millimeter wave amplifier design. Transformers provides flexible matching and inductive peaking capability with variable coupling ratio and alterable polarity. In some cases, a transformer is essentially equivalent to two inductors with additional mutual inductance but consumes an area similr to one inductor. The transformer layout is also similar to a symmetrical spiral inductor with a turn ratio close to one. Figure 6 shows different layouts of transformers for small turn ratio design. The black line represents the primary coil and grey line represents the secondary coil. The layout of type (a) has a small coupling factor because of less mutual inductance, and is relatively simple to achieve the desired coupling factor. The design of type (b) has a moderate coupling factor. Type (c) has a large coupling factor while the quality factor is smaller due to the capasitive parasitics. Note that the secondary side consists of several coils connected in parallel to obtain a small turn ratio. For these transformers with the winding in the same metal layer, the maximum achieveable couplng factor mainly depends on the minimum metal spacing. Another design shown in Fig. 6(d) use two adjacent metal layers for the winding of the coils. A high coupling factor can be achieved if a thin dielectric layer is between the two metals can be used. Note that the parasitic capacitance is relatively large, which could limit the operation frequency. A general respentation of the equivalent circuit model for an on-chip transformer is shown in Fig. 6(e), where R_1 and R_2 represent the ohmic losses due to the resistivity of the inductor metal lines; C_p is the parasitic capacitance of each coil originated from the spial routing; C_m represents the coupling capacitance between the primary and secondary coils; C_{ox} is the oxide layer parasitic capacitance and C_{si} and R_{si} represent the coupling and ohmic losses due to the silicon substrate. The coefficient *M* describes the inductive coupling between the primary and the secodary coils.

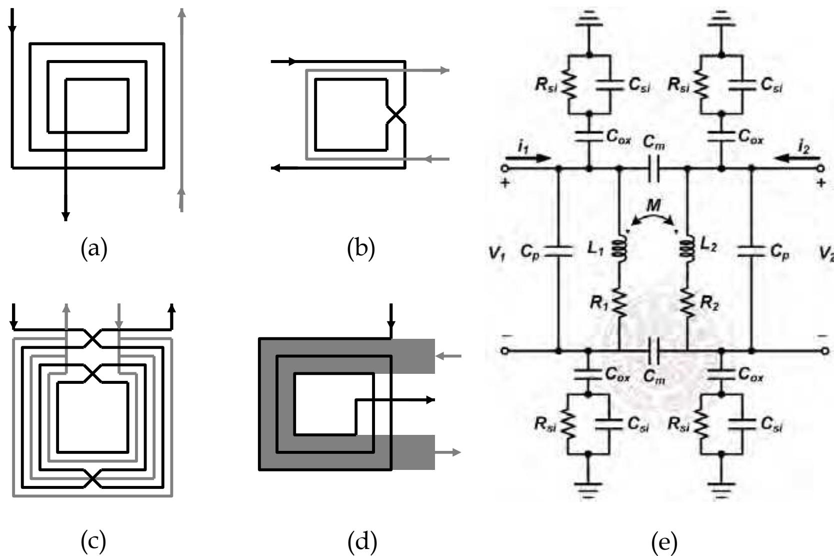


Fig. 6. (a)-(d) different desings of transformers (e) equivalent circuit model of an on-chip transformer.

It is worth mentioning that co-design of active and passive components is a useful approach to optimize the performnce of microwave circuits. For the operation frequencies up to tens of GHz, the undesired resistive and capacitive components can seriously degrade the amplifier performance. As mentioned earlier, interconnect in a transistor is a critical issue for its frequency response and the inductive components are useful for bandwidth enhancement. By co-design of the transistor interconnect and the inductive components, the parasitics can be effectively minimized to enhance circuit performance. More details will be discussed later using the proposed broadband amplifier as an example, in which the transformer design considers with the transistor interconnect layout simultaneously to reduce the parasitics.

3. Design Techniques for Broadband Amplifiers

For the broadband amplifiers designed by MOSFETs, the circuit bandwidth is ultimately limited by the intrinsic capacitances of the transistors. Different approaches were proposed for bandwidth extension such as f_T doubler (Galal & Razavi, 2003), negative impedance converter (Galal & Razavi, 2003), negative Miller capacitance (Galal & Razavi, 2003; Mataya et al., 1968), distributed amplifier (DA) (Arbabian & Niknejad, 2008; Chien & Lu, 2007), and inductive peaking technique (Mohan et al., 2000; Galal & Razavi, 2003; Galal & Razavi, 2004), as shown in Fig. 7. The main design concept in these techniques is all related to how to reduce the impact of the parasitic capacitances on the circuit. Compared with the conventional differential amplifier, the f_T doubler topology reduces the input capacitance roughly to half and thus the f_T extends out to twice of the frequency. The negative impedance converter can generate negative impedance to cancel the undesired parasitics for

bandwidth enhancement. The negative Miller capacitance technique uses the similar concept to cancel the gate-drain capacitance of the transistor to extend the bandwidth. Compared with the bandwidth enhancement using passive components, these techniques utilize active components with a smaller chip area while consume additional power. Note that the effectiveness of the bandwidth extension is sensitive to the bias condition and could induce undesired oscillation problems.

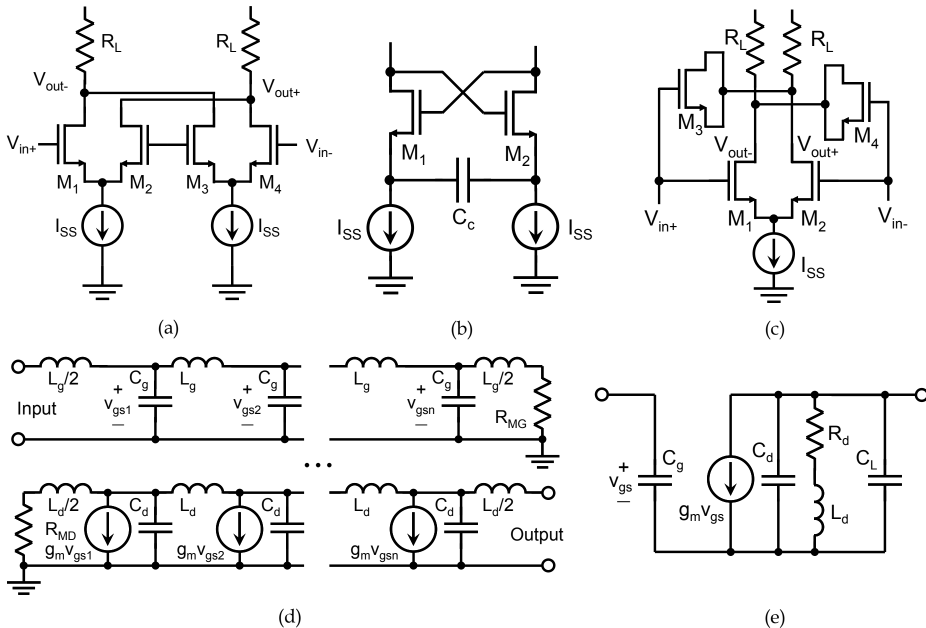


Fig. 7. Bandwidth enhancement techniques: (a) f_T doubler (b) negative impedance converter (c) negative Miller capacitance (d) distributed amplifier (DA), and (e) inductive peaking.

The DA configuration is a popular technique and Fig. 7(d) shows the simplified circuit scheme for a MOS distributed amplifier. The resistors R_{MG} and R_{MD} terminate the gate and drain lines to minimize the destructive reflection for stability and gain flatness. With the inductors L_g and L_d, the input and output artificial transmission lines are constructed by incorporating the equivalent gate and drain capacitances C_g and C_d, respectively. By a proper design of the transmission line delay, the output signal from each stage is added in phase resulting in a gain-bandwidth product much greater than that of an individual amplifier. It should be mention that the DA architecture normally consumes a large DC power and occupies a considerable amount of chip area for obtaining a high gain-bandwidth product.

Another attractive design approach is the inductive peaking technique. The fundamental idea is to introduce a zero by an inductor to cancel the original RC pole and extend the circuit bandwidth. Figure 7(e) shows a simple example of the inductive peaking topology, which is a common-source (CS) amplifier with shunt inductor peaking. With a peaking inductor L_d connected in series with the load resistor R_d, the capacitive parasitics can be

resonated out at the frequency around the original pole to extend the circuit bandwidth. The inductive peaking technique can achieve a large bandwidth while maintain a small power consumption. Various inductor peaking configurations such as shunt peaking, shunt-series peaking (Fig. 8(a)), and T-coil peaking techniques (Fig. 8(b)) will be analyzed together with the discussion of the bandwidth enhancement ratio (BWER) of each technique. Note that the comparison is based on a fundamental cascaded common-source topology, which is widely used for high frequency broadband amplifiers. The proposed wideband design techniques as will be illustrated in Section 4 also employ the cascade configuration. One fundamental difference between the DA and the cascade topology is the overall gain of each stage for the former sums up whereas that for the latter multiplies. As a result, the power consumption and chip area can be effectively reduced using the cascade configuration.

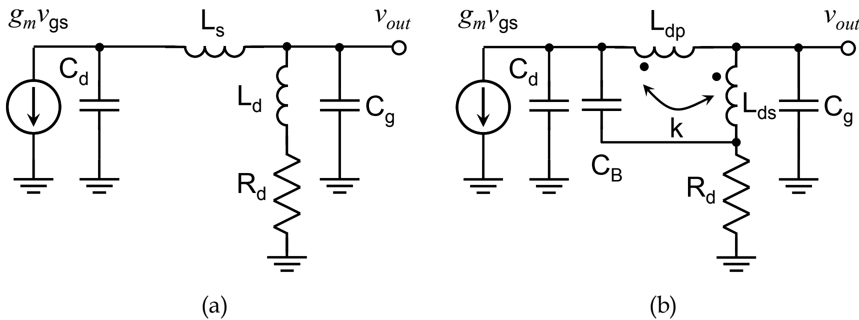


Fig. 8. (a) shunt-series inductive peaking (b) T-coil inductive peaking.

3.1 Shunt Peaking

For the small-signal equivalent circuit model of a cascaded CS amplifier, as shown in Fig. 9, the 3-dB bandwidth of each stage is determined by the drain resistance R_d, equivalent drain capacitance C_d, and equivalent gate capacitance C_g of the next stage. The ratio of C_g to C_d can be determined from the foundry provided model for a more practical estimation, which is between 2.5 and 3.5 (0.5 ~ 60 GHz) in 0.18-μm CMOS technology. Note that the gate-to-drain capacitance C_{gd} is split by the Miller theorem and included in C_g and C_d in this case. To simplify the circuit analysis, C_g/C_d is set to be 3 for the following analysis.

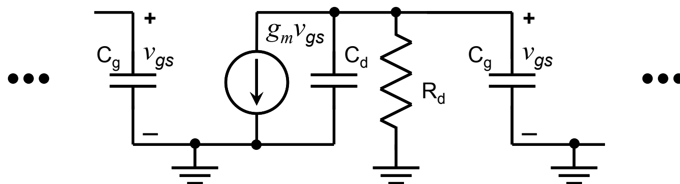


Fig. 9. Small-signal equivalent circuit model of a cascaded common-source amplifier.

The most straightforward bandwidth enhancement technique is probably shunt peaking (Mohan et al., 2000), as shown in Fig. 7(e). By connecting an inductor L_d in series with R_d, the parasitic capacitance of the drain node can be resonated out by a shunt LC resonance. An

alternative explanation is that the peaking inductor introduces a zero to extend the circuit bandwidth. Based on the transimpedance transfer function, the design equation for L_d can be derived and written as:

$$L_d = m_d R_d^2 (C_d + C_g) \tag{3}$$

With an m_d of 0.71, the maximum achievable BWER is 1.85 with a gain peaking of 1.5 dB, as shown in Fig. 10, *curve* (ii). Note that *curve* (i) is the normalized frequency response of this circuit without any bandwidth enhancement method applied.

3.2 Shunt-series Peaking

The second technique is shunt-series peaking (see Fig. 8(a)) which employs two inductors, one inductor L_d is connected in series with R_d and the other inductor L_s is in series with C_g. The design equation for both inductors can be written as:

$$L_d = \frac{L_s}{2} = \frac{R_d^2 (C_d + C_g)}{4} \tag{4}$$

The circuit analysis presented in the original publication (Galal & Razavi, 2004) shows a BWER up to 3.46 with a gain peaking of 1.8 dB based on the assumption that C_g/C_d is one. However, the BWER reduces to 1.83 when C_g/C_d of 3 is used, as shown in Fig. 10, *curve* (iii).

3.3 T-Coil Peaking

A more effective technique is the T-coil peaking (Galal & Razavi, 2003) which utilizes one transformer and one capacitor as shown in Fig. 8(b). The primary coil L_{dp} is connected between the drain node and C_g, and the secondary coil L_{ds} is between R_d and C_g. In addition, the bridge capacitor C_B is connected between the drain node and R_d. By neglecting C_d, the design equations for the transformer and capacitor can be written as:

$$L_{dp} = L_{ds} = \frac{C_g R_d^2}{4}\left(1 + \frac{1}{4\zeta^2}\right) \tag{5}$$

$$k = \frac{4\zeta^2 - 1}{4\zeta^2 + 1} \tag{6}$$

$$C_B = \frac{C_g}{16\zeta^2} \tag{7}$$

For a flat group delay response, a ζ of $\sqrt{3}/2$ results in a BWER of 2.82 if C_d is neglected. Note that the BWER obtained in Fig. 10, *curve* (iv) is reduced to 2.40 since C_d is taken into account for a fair comparison.

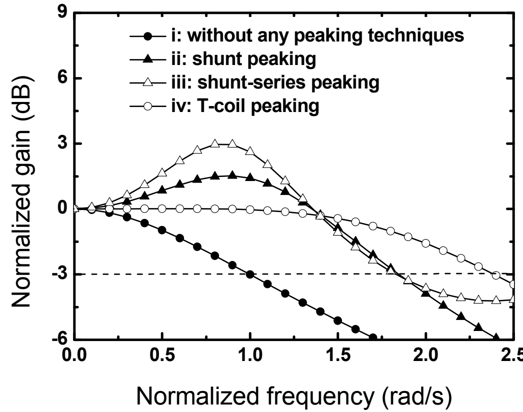


Fig. 10. Frequency response of using different inductive peaking techniques for bandwidth improvement.

4. Proposed Broadband Design Techniques

The above discussed bandwidth enhancement techniques are effective and have been used in many CMOS broadband amplifiers. In this section, we introduce two different inductive peaking techniques for wideband amplifier design.

4.1 π-type Inductor Peaking (PIP)

Figure. 11 shows the small-signal equivalent circuit model of a cascaded CS stage including the proposed PIP inductors (L_{d1}, L_{s1}, and L_{d2}), where R_{d1} and R_{d2} are the drain bias resistors. An improved BWER up to 3.31 can be obtained using the PIP inductor peaking technique by including the drain capacitance C_d, and under an assumption that the ratio of C_g/C_d is 3. The bandwidth improvement by adding each peaking inductor is described as follows.

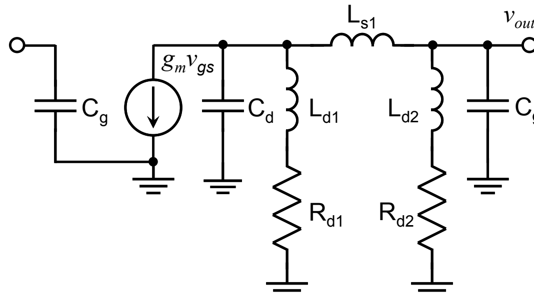


Fig. 11. The equivalent circuit model of one gain stage with the pi–type inductor peaking (PIP) technique.

If not considering the inductors, the drain current $g_m v_{gs}$ flows into C_d, C_g, R_{d1}, and R_{d2}, and generates the output voltage v_{out}. In this case, the 3-dB bandwidth ω_0 is limited by the resistive and capacitive loads. By inserting L_{d2} in series with R_{d2}, the bandwidth is increased by a parallel resonance with C_d and C_g. If L_{s1} is also added, the bandwidth can be further enhanced by a series resonance with C_g at higher frequencies, which forces more drain current to flow through L_{s1} and reach the output terminal. Finally, by introducing one more inductor L_{d1}, C_d and C_g can be resonated in parallel with L_{d1} at even higher frequencies to obtain a further improved bandwidth. According to the circuit shown in Fig. 11, Fig. 12 is the frequency response of the above four conditions, where ω_0 and the DC gain are both normalized. The gradually improved bandwidth can be observed as adding the three peaking inductors step by step. An improved BWER up to 3.31 can be obtained with the three PIP inductors.

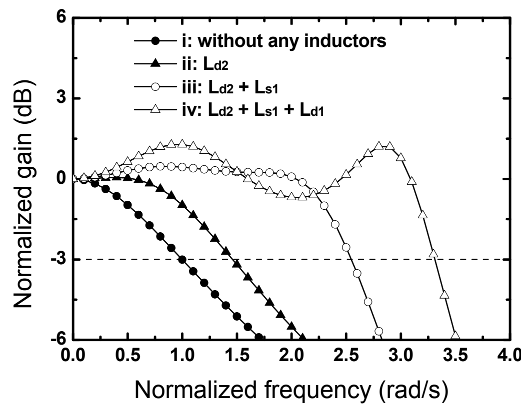


Fig. 12. Comparison of the bandwidth enhancement results using PIP technique under different numbers of peaking inductors, where C_g= 3C_d and R_{d1}= R_{d2}.

Based on the circuit in Fig. 11, the transimpedance transfer function $Z_{PIP}(s)$ can be derived as follows:

$$Z_{PIP}(s) = \frac{v_{out}}{-g_m v_{gs}} = R_{d1}R_{d2}\frac{1+s\left(\frac{L_{d1}}{R_{d1}}+\frac{L_{d2}}{R_{d2}}\right)+s^2\frac{L_{d1}}{R_{d1}}\frac{L_{d2}}{R_{d2}}}{D_0+sD_1+s^2D_2+s^3D_3+s^4D_4+s^5D_5} \quad (8)$$

where

$$\begin{aligned}
D_0 &= R_{d1}+R_{d2} \\
D_1 &= L_{d1}+L_{d2}+L_{s1}+R_{d1}R_{d2}\left(C_d+C_g\right) \\
D_2 &= \left(C_d+C_g\right)\left(R_{d1}L_{d2}+R_{d2}L_{d1}\right)+R_{d1}L_{s1}C_d+R_{d2}L_{s1}C_g \\
D_3 &= L_{d1}C_d\left(L_{d2}+L_{s1}\right)+L_{d2}C_g\left(L_{d1}+L_{s1}\right)+R_{d1}R_{d2}L_{s1}C_dC_g \\
D_4 &= L_{s1}C_dC_g\left(R_{d1}L_{d2}+R_{d2}L_{d1}\right) \\
D_5 &= L_{d1}L_{d2}L_{s1}C_dC_g
\end{aligned} \quad (9)$$

The required inductances for bandwidth improvement can be determined analytically from the transfer function. The numerator includes two zeros (R_{d1}/L_{d1}) and (R_{d2}/L_{d2}) and the denominator contains two pairs of complex conjugate poles. By solving the transfer function with properly designed damping factors (< 0.707), these zeros and poles can enhance the bandwidth effectively. The properties of the poles and zeros as adding the three peaking inductors step by step are summarized in Table 1. Note that these values are obtained by assuming the gain flatness is smaller than 2.0 dB.

	without PIP	L_{d2}	$L_{d2} + L_{s1}$	$L_{d2} + L_{s1} + L_{d1}$
Zero	−	$\omega_{z1} = 1.33$	$\omega_{z1} = 1.33$	$\omega_{z1} = 1.33$ $\omega_{z2} = 2.50$
Pole	$\omega_{p1} = 1.00$	−	−	$\omega_{Ld1,p3} = 1.39$
Complex pole	−	$\omega_{Ld2,p1} = \omega_{Ld2,p2} = 1.15$	$\omega_{Ls1,p1} = \omega_{Ls1,p2} = 1.21$ $\omega_{Ls1,p3} = \omega_{Ls1,p4} = 2.37$	$\omega_{Ld1,p1} = \omega_{Ld1,p2} = 1.28$ $\omega_{Ld1,p4} = \omega_{Ld1,p5} = 3.01$
Damping factor	−	$\xi_{Ld2,p1} = 0.79$	$\xi_{Ls1,p1} = 0.82$ $\xi_{Ls1,p3} = 0.28$	$\xi_{Ld1,p1} = 0.63$ $\xi_{Ld1,p4} = 0.14$

Table 1. Properties of the poles and zeros of one gain stage with PIP under different numbers of peaking inductors, where ξ and ω_n are the damping factor and the corner frequency of the complex poles, respectively.

Based on the proposed PIP technique, a transimpedance amplifier targeting at 40-Gb/s for OC-768 applications is realized in standard 0.18-µm CMOS technology. The 40-Gb/s TIA composes of four cascaded CS stages for high transimpedance gain, as shown in Fig. 13. Identical resistance for the drain bias resistor R_D of each stage is employed, and the input and output impedances are designed as 50 Ω through the resistors R_{M1} ~ R_{M4}. For a high-gain consideration, a large R_D is preferred while the required peaking inductances for PIP topology increases as well. A trade-off exists here since a large inductor not only occupies more chip area but also has lower operation frequency. The resistive parasitics associated with a large inductor also degrade the circuit performance. In practical design, R_D is ~ 200 ohm and the inductors are designed to be smaller than the calculated values to reduce the resistive loss.

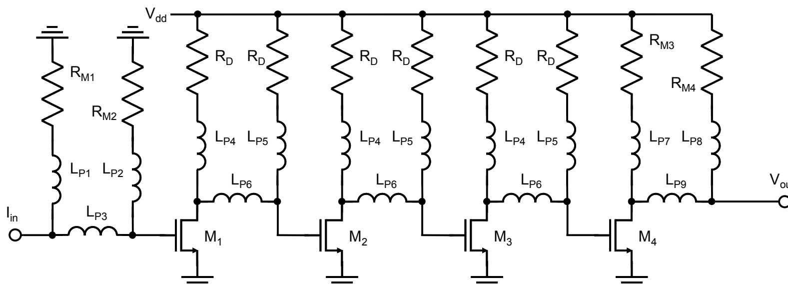


Fig. 13. Circuit topology of the proposed 40-Gb/s CMOS TIA with PIP.

Figure 14 compares the design of a TIA with and without using the proposed PIP technique. With a transimpedance gain Z_T of 51 dBΩ, the simulated bandwidth for the TIA with PIP is improved by a factor up to ~11 (33.8 GHz/3.1 GHz) compared to that without applying the PIP inductors.

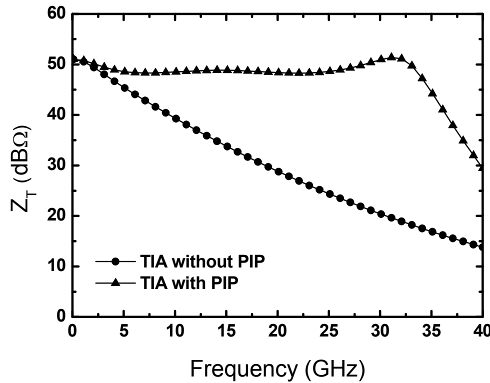
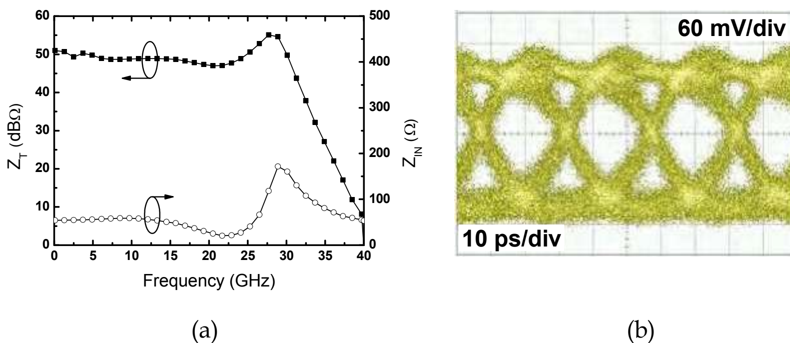


Fig. 14. Simulated frequency response for the TIA with and without PIP.

The TIA was fabricated in 0.18-μm CMOS technology with a chip area of 1.17 × 0.46 mm^2 and measured on-wafer with coplanar ground-signal-ground (GSG) probes. The measured transimpedance gain Z_T is shown in Fig. 15 (a). The gain and the 3-dB bandwidth are 51 dBΩ and 30.5 GHz in the presence of an on-chip C_{pd} of 50 fF at the input, respectively. Note that the C_{pd} placed at the input is to take the photodiode parasitic capacitance into consideration. Under a 1.8 V supply voltage, the amplifier consumes 60.1 mW, and a gain-bandwidth product per DC power figure-of-merit (GBP/P_{dc}) of 180.1 GHzΩ/mW is achieved. To measure the transient response of the 40-Gb/s TIA, a high speed 2^{31}-1 PRBS is applied. With an input current swing of 740 μA$_{pp}$, the output eye diagram at 40-Gb/s is shown in Fig. 15 (b) with an output voltage swing of 263 mV$_{pp}$.



(a) (b)

Fig. 15 Measured (a) transimpedance gain Z_T and (b) eye diagram at 40 Gb/s (2^{31}-1 PRBS) of the amplifier using PIP technique.

4.2 Asymmetrical Transformer Peaking (ATP)

Transformers are very useful for enhancing the microwave circuit performance owing to the mutual inductance. Amplifiers designed with transformers also allow operation under a low supply voltage. Compared to the inductor peaking technique, peaking with transformer can extend the bandwidth whereas with an improved area efficiency. Figure 16 shows the proposed asymmetrical transformer peaking (ATP) technique for broadband amplifier design. The basic design is also the cascaded common-source (CS) configuration to enhance the gain-bandwidth product. Compared with the typically used cascode topology as a unit gain block for microwave amplifier design, the CS design is easier for achieving low power design owning to the low supply voltage. Similar to other inductor peaking techniques, the basic idea of ATP is to resonate out the parasitic capacitance for bandwidth enhancement. Moreover, the transformer has the advantage of additional mutual inductor to reduce the required area of inductors. The asymmetrical primary and secondary coils can also accommodate the unequaled parasitic loading capacitances in a transistor. Based on the foundry provided transistor model and ideal inductive components, Fig. 17 shows the comparison of three designs with the same basic five-stage CS configurations. The results indicate that these designs present a similar low-frequency gain but with an obvious bandwidth difference. Without applying any peaking technique, the bandwidth is only 7.0 GHz (*curve* (i)), while the bandwidth can be significantly enhanced up to 69.7 GHz (*curve* (ii)) if the transformer is symmetrical. With the further improvement with asymmetrical coils in transformer design, the bandwidth increases up to around 80 GHz (*curve* (iii)).

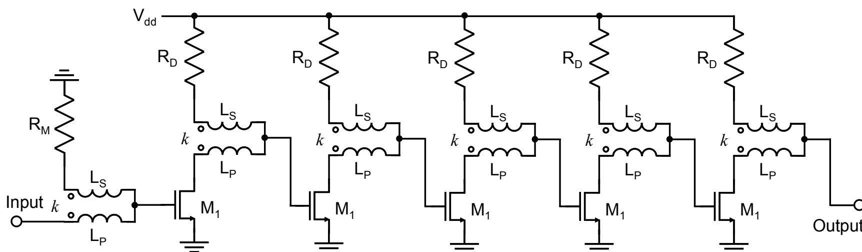


Fig. 16. The proposed broadband amplifier using asymmetrical transformer peaking (ATP) technique.

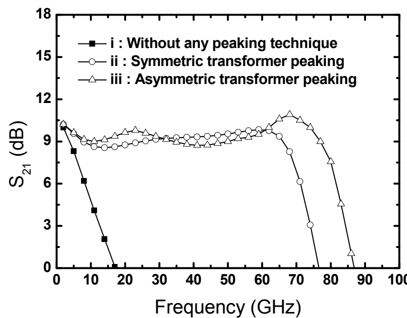


Fig. 17. Simulated frequency response with different inductive peaking techniques.

The small-signal equivalent circuit model for one gain stage in the cascaded CS configuration using transformer peaking technique is shown in Fig. 18, where C_g is the gate capacitance of the next stage and k is the coupling factor. Based on this model, the transimpedance transfer function $Z_T(s)$ from the current source $g_m v_{gs}$ to the output voltage v_{out} can be derived as:

$$Z_T(s) = \frac{v_{out}}{-g_m v_{gs}}$$
$$= R\frac{1+s\left(L_S - k\sqrt{L_P L_S}\right)/R}{1+sR\left(C_d + C_g\right)+s^2\left(L_P C_d + L_S C_d + L_S C_g\right)+s^2\left(-2k\sqrt{L_P L_S}C_d\right)+s^3 R L_P C_d C_g + s^4 L_P L_S C_d C_g (1-k)} \quad (10)$$

As can be observed from (10), one zero (numerator) and two pairs of complex poles (denominator) are introduced, and the damping factors of the poles could be smaller than 0.707 if the circuit is properly designed. For the case of $L_P = L_S$, the design is not optimized due to the inherently unequaled loading capacitances ($C_d \neq C_g$) from each side of the transformer.

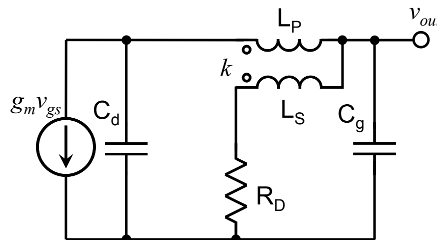


Fig. 18. Small-signal equivalent circuit model for one gain stage using transformer peaking technique.

The polarity of the transformer is also critical in this design. With a similar configuration but opposite transformer polarity, the derived Z_T from (10) can be applied directly except that all the signs need to be inversed for the k-related terms. In other words, the coupling coefficient k becomes negative in the original equation. This difference reduces the frequencies of the zero and the complex poles resulting in a smaller BWER. Based on the above analysis, the unequal inductances and an appropriate transformer polarity are both beneficial for bandwidth extension. By using the asymmetric transformer T_D, the circuit bandwidth can be enhanced up to 80.6 GHz with a gain flatness of ±1.1 dB by L_P= 0.11 nH, L_S= 0.2 nH, and k= 0.3, as shown in Fig. 17, *curve* (iii).

It should be mention that a co-design appraoch is adopted to minimize the undesired parasitics and further enhance the amplifier performance. For millimeter wave design, layout is critical for circuit performance. In this study, the transformer layout is co-designed with the transistors for reducing the loss from interconnect parasitics and minimizing the chip area. In the adopted 0.13-μm CMOS technology, one-poly and eight-metal layers (1P8M) with various metal thicknesses and line spacings are available for transformer design. In typical design, the top layer M8 is employed for inductive components owing to the thicker metal for a lower conductor loss. However, if considering the interconnects and the overall circuit performance, M3 is a better choice for the transformer winding. By using M3 instead of M8, the additional loss introduced by the metal/via connections from M3 to M8 can be

eliminated, which can be significant at the frequency of interest. In addition, the minimum metal spacing of M8 is restricted to 2 μm, whereas the M3 layer provides a spacing of 0.21 μm enabling a transformer with an enhanced coupling coefficient. Although the thickness of M3 is smaller than M8, the skin effect as operating at tens of GHz makes the metal thickness not that critical. For achieving the desired inductance ratio while maintaining design simplicity, two individually wound inductors are closely placed to form a transformer, as shown in Fig. 19 (a). Figure 19 (b) is the chip micrograph of the five-stage CS broadband amplifier with asymmetrical transformer peaking. The circuit area including the DC and RF probing pads is 0.66 × 0.59 mm², and the core area is only 0.48 × 0.11 mm² (~ 0.05 mm²).

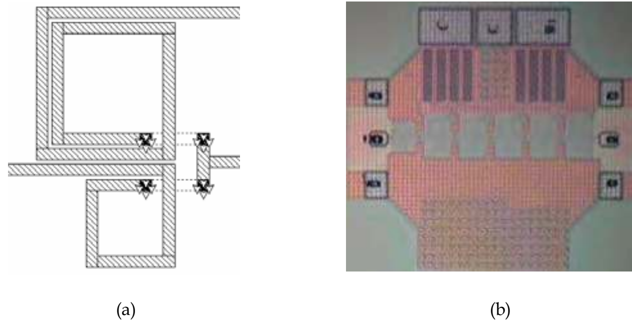
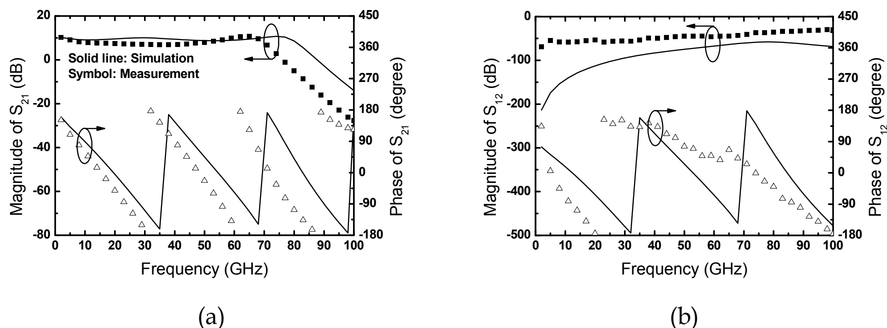
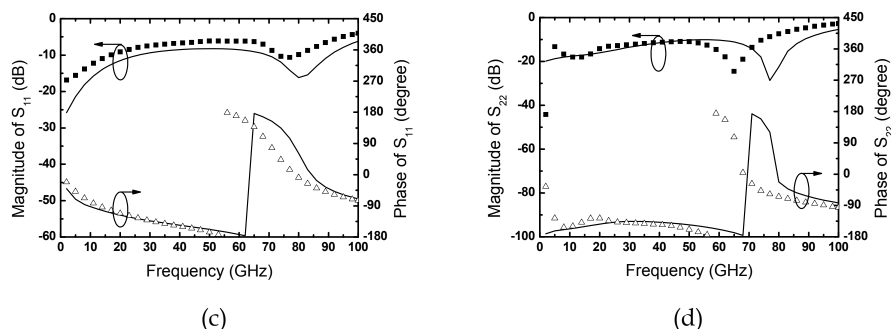


Fig. 19. (a) On-chip asymmetric transformer layout (b) chip micrograph (area: 0.66× 0.59 mm², core area: 0.48× 0.11 mm²)

The broadband amplifier was fabricated in a standard 1P8M 0.13-μm CMOS process. The ground-signal-ground (GSG) RF probes were used for the on-wafer S-parameters measurement from 2 GHz to 100 GHz, as shown in Fig. 20 together with the simulated results. The measured S_{21} at low frequencies is 10.3 dB and the circuit bandwidth is 70.6 GHz under a power consumption P_{DC} of 79.5 mW. A gain-bandwidth product of 231 GHz and a GBP/P_{DC} of 2.9 GHz/mW are achieved. The measured reverse isolation S_{12} is well below -30 dB up to 100 GHz. In addition, the measured S_{11} and S_{22} are below -6.1 dB and -10.8 dB respectively within the circuit bandwidth. The measured output 1-dB compression points $P_{1dB,out}$ are 0.2 dBm, -0.2 dBm, and -1.0 dBm at 5 GHz, 10 GHz, and 20 GHz, respectively.





(c) (d)

Fig. 20. Measured and simulated S-parameters of the proposed broadband amplifier using the proposed asymmetric transformer peaking (ATP).

5. Conclusion

In this chapter, various aspects for the design of microwave and millimeter wave broadband amplifiers using modern CMOS technology were discussed. Section 1 briefly introduced the applications of broadband amplifiers in wireline/wireless communication systems. Section 2 illustrated the design considerations of transistors and inductive components using standard CMOS process. The transistor geometry and interconnect were shown to be critical to its high frequency response. The design tradeoffs were also analyzed for spiral inductors and transformers in CMOS technology. In section 3, different design techniques for broadband amplifiers were reviewed. Three inductor peaking techniques including shunt, shunt-series, and T-coil approaches were compared in details. Section 4 focused on the bandwidth enhancement techniques that we proposed for CMOS broadband amplifier design. With the proposed π-type inductive peaking (PIP) technique, a 40 Gb/s transimpedance amplifier (TIA) was realized in 0.18-μm CMOS technology. We also proposed an asymmetrical transformer peaking (ATP) technique to achieve a miniaturized 70 GHz broadband amplifier in 0.13-μm CMOS technology with a core area of only ~ 0.05 mm^2. The PIP and ATP design techniques can be utilized for many high-speed building blocks in wireline/wireless communications systems, such as laser/modulator driver, multiplexer/de-multiplexer, and low noise amplifier/power amplifier. The successfully demonstrated design techniques for enhancing the performance of CMOS integrated amplifiers at microwave and millimeter wave frequencies enable further studies for various applications.

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