Application of Fourier Series Expansion to Electrical Power Conversion

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Additional information is available at the end of the chapter

Abstract

Many power electronic applications demand generation of voltage of a rather good sinusoidal waveform. In particular, dc-to-ac voltage conversion could be done by multilevel inverters (MLI). A number of various inverter topologies have been suggested so far: diode-clamped (DC) MLI, capacitor-clamped (CC) MLI, cascaded H-bridge (CHB) MLI, and others. Fourier series expansions have been used to investigate and to form a basis of different topologies comparison, to discover their advantages and disadvantages, and to determine their control. In this chapter, we discuss modulation strategies of DCMLI and CHBMLI, solve their harmonics spectra analytically, and compare them using harmonic distortion indices.

Keywords: Fourier series, multilevel inverters, pulse width modulation, harmonics, THD

1. Introduction

The term "power electronics" is used for a family of electrical circuits which convert electrical energy from one level of voltage/current/frequency to other using semiconductor-based switches. The switching process in power electronic converters is called *modulation*, and development of optimum modulation strategies has been the subject of research in power engineering during several past decades. Electrical power conversion has evolved as new topologies, switching devices, control, and modulation strategies have been proposed. Each group of power electronic converters has its own preferable modulation approach optimizing the circuit performance, addressing such issues as switching frequency, distortion, losses, and harmonics generation. Only voltage source inverters modulation will be discussed below.

Before turning to specific issues of modulation, one needs to establish a common basis to compare the modulation schemes. Different merits are used to evaluate a particular pulse

width modulation (PWM) implementation: diminished harmonics [1], filtered distortion performance factors [2], and the root-mean-square (RMS) harmonic ripple current [3]. In this text, analytical solutions to PWM strategies are used to compare magnitude of various harmonic components. This approach has a number of advantages [4].

Firstly, the conventional method of determining harmonic components of a switched waveform using fast Fourier transform (FFT) of the waveform is sensitive to the time resolution of the simulation and periodicity of the overall waveform. Moreover, it ensures that intrinsic harmonic components of PWMs are not affected by such factors as simulation round off errors, dead time, switch ON-state voltages, DC bus ripple voltages, etc.

Secondly, PWM strategies can be compared at exactly the same phase leg switching frequency.

And thirdly, the first-order weighted total harmonic distortion (WTHD) is used for a quick comparison of PWMs since it has a physical meaning (the normalized current ripple expected into an inductive load when fed from the switched waveform) and often used performance indicator.

The rest of the paper is organized as follows. In Section 2, information on the double Fourier series expansions and necessary relations is given. Essentials on PWM are provided in Section 3. Different voltage inverter topologies and their analytical PWM solutions are presented in Section 4. Harmonic distortion factors of the introduced inverter topologies, different modulation schemes are compared in Section 5, and a summary on the chapter is given in Section 6.

2. Double Fourier series expansion

2.1. Double Fourier series decomposition for a double variable function

It is well known that a periodic two variable waveform $f(x, y)$ can be expressed in the form

$$
\begin{aligned}
f(x, y) = \frac{A_{00}}{2} &+ \sum_{n=1}^{\infty} [A_{0n} \cos ny + B_{0n} \sin ny] + \sum_{m=1}^{\infty} [A_{m0} \cos mx + B_{m0} \sin mx] \\
&+ \sum_{m=1}^{\infty} \sum_{\substack{n=-\infty \\ n \neq 0}}^{\infty} [A_{mn} \cos (mx + ny) + B_{mn} \sin (mx + ny)]
\end{aligned}
\tag{1}
$$

where the double Fourier series components can be found in a complex form:

$$
C_{mn} = A_{mn} + jB_{mn} = \frac{1}{2\pi^2} \int_{-\pi}^{\pi} \int_{-\pi}^{\pi} f(x, y) \, e^{j(mx+ny)} \, dx \, dy.
\tag{2}
$$

The first term in Eq. (1) is the *DC offset* that should be zero or negligibly small. The second summation term represents the *baseband harmonics*. The first baseband harmonic, $n = 1$, is the *fundamental harmonic* whose magnitude defines the magnitude of the output waveform. Other baseband harmonics, $n > 1$, represent low-frequency undesired fluctuations about

the fundamental output and should preferably be eliminated with the modulation process. The third summation term in Eq. (1) corresponds to the *carrier harmonics* which are relatively high-frequency components. Finally, the last double summation term in Eq. (1) corresponds to groups of the *sideband harmonics* of order n located around the mth carrier harmonic component.

2.2. Jacobi-Anger expansion and Bessel functions relations

The magnitudes of harmonic components in Eq. (1) are to be determined for each PWM scheme for each particular combination of indexes m and n. The evaluations are based on Jacobi-Anger expansions

$$e^{\pm j\xi \cos \theta} = J_0(\xi) + 2 \sum_{k=1}^{\infty} j^{\pm k} J_k(\xi) \cos k\theta = \sum_{k=-\infty}^{\infty} j^k J_k(\xi) \, e^{jk\theta} \tag{3}$$

and a number of Bessel function properties: $J_{-n}(\xi) = (-1)^n J_n(\xi)$ and $J_n(-\xi) = (-1)^n J_n(\xi)$, that particularly implies $J_0(-\xi) = J_0(\xi)$ [5].

2.3. Parseval's theorem

Given $f(x)$ is a periodic function with the period T, it can be represented by its Fourier series $f(x) = a_0/2 + \sum_{n=1}^{\infty} a_n \cos n\omega t + b_n \sin n\omega t$ where $\omega = 2\pi/T$ is the fundamental angular frequency. Then, on $[-T/2, \ T/2]$, the Parseval's theorem assumes the form

$$\frac{1}{T} \int_{-T/2}^{T/2} f^2(x) \, dx = \frac{a_0^2}{4} + \sum_{n=1}^{\infty} \frac{a_n^2 + b_n^2}{2}. \tag{4}$$

3. Pulse width modulation

To introduce the concept of PWM, let us consider a basic configuration of one-phase two-level inverter leg shown in **Figure 1**. It consists of two switches, S_1 and S_2, and two diodes, D_1 and D_2. Switches S_1 and S_2 are operating alternately at high frequency to generate a quasiperiodic output voltage $v_a(t)$, whose low-frequency components are intended to deliver a prescribed AC supply. When the switch S_1 (S_2) is ON, a positive voltage, $+V_{dc}$, (respectively, negative voltage, $-V_{dc}$) is supplied to a load at the connection point a.

The essential concept of a two-level pulse-width-modulated converter system is that a low-frequency target waveform is compared against a high-frequency carrier waveform, and the comparison result is used to control the state of a switched phase leg. In case of the inverter in **Figure 1**, the phase leg is switched to the upper DC rail when the target waveform is greater than the carrier waveform, otherwise to the lower DC rail. As a result, a sequence of pulses switching between the upper and the lower DC rails is generated, which contains the target waveform as the fundamental component but also a series of unwanted harmonics arising due to the switching process.
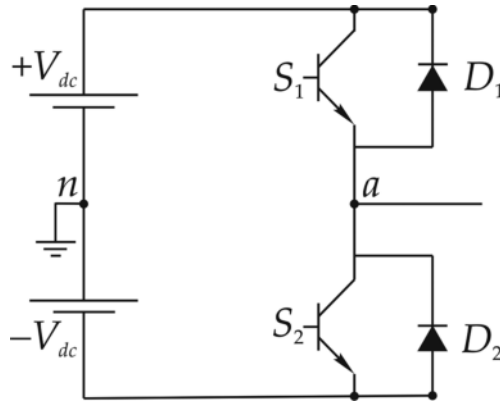
Figure 1. Half-bridge one phase two-level inverter leg.

The most well-known analytical method of determining the harmonic components of a PWM switched phase leg was first developed by Bowes and Bullough [1], who adopted an analysis approach originally developed for communication systems by Bennet [6] and Black [7] to modulated converter systems.

The analysis is based on the existence of two time variables $x(t) = \omega_c t$ and $y(t) = \omega_0 t$, where ω_0 and ω_c are the angular frequencies of the fundamental (target, sinusoid) low-frequency modulated waveform and the carrier high-frequency modulating waveform, $\omega_0 \ll \omega_c$. Variables $x(t)$ and $y(t)$ are considered to be independently periodic. If the ratio ω_c / ω_0 is integer, the generated pulse width trail will be periodic [4].

The problem of finding a PWM for the modulated periodic waveform $f(t)$ can be solved by exploring a unit cell which identifies contours within which $f(t)$ remains constant for cyclic variations of $x(t)$ and $y(t)$ and is equal to the phase leg output voltage. Thus, a three-dimensional (3D) unit cell is a plot of two time variables function with z assuming values of $f(x, y)$ where x and y vary from $-\pi$ to π. Contours of $f(x, y)$ within the unit cell depend on a particular PWM strategy which will be discussed below.

3.1. Carrier-based PWM schemes

3.1.1. Carrier waveforms and unit cells

Since the target waveform is usually a sinusoid, PWM schemes can be categorized based on the carrier waveform: saw-tooth leading edge (**Figure 2a**), saw-tooth trailing edge (**Figure 2b**), and double edge (**Figure 2c**).

Let the modulated waveform of a phase be given $v_a^{\text{id}} = M \cos y$, where M is the modulation index, $0 < M < 1$. For the one-phase two-level inverter leg shown in **Figure 1**, unit cells with contour plots for each carrier waveform modulation are presented in **Figure 3**. The output of the modulated waveform assumes either $+V_{dc}$ or $-V_{dc}$, and the regions of the constant output are bounded by reference waveforms $\Omega(y) = \pm \pi M \cos y$. For saw-tooth modulations, one of
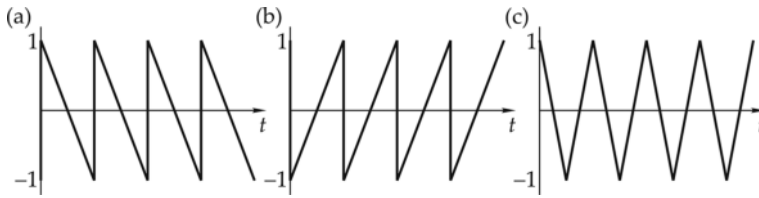
Figure 2. Carrier waveform: (a) saw-tooth leading edge; (b) saw-tooth trailing edge; (c) double edge.
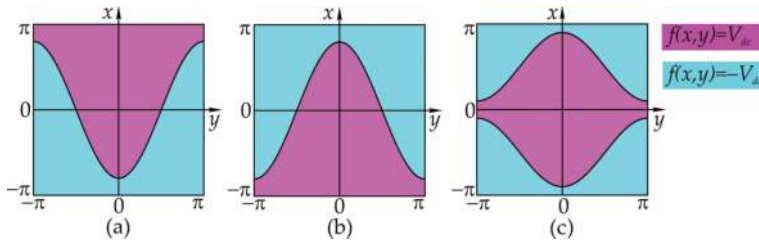

Figure 3. Contour plots for a sine modulated reference waveform and different carrier modulating waveform: (a) saw-tooth leading edge; (b) saw-tooth trailing edge; (c) double edge.

switching time instances (within a period of the carrier waveform) is independent of the reference waveform resulting in only one side of the contour plot to be sinusoid. The double-edge PWM both sides of the switched output are modulated providing better harmonic performance unlike saw-tooth modulations [4]. Hereinafter, only double-edge modulation is considered.

To determine the harmonics content and the output waveform of a particular PWM, the double Fourier series coefficients C_{mn} (or, equivalently, A_{mn} and B_{mn}) are to be found using Eq. (2). To solve the problem, the periodic function $f(x, y)$ is to be integrated over the unit cell of the PWM scheme.

3.1.2. PWM sampling schemes

Based on the choice of switching time instances, PWM schemes can be divided into: naturally sampled (NS), symmetrically regularly sampled (SR), and asymmetrically regularly sampled (AR) PWMs.

3.1.2.1. Naturally sampled PWM

For NS PWM scheme, switching occurs at time instances corresponding to intersection of the carrier and target waveforms. Switching time instances can also be determined as the intersection between the reference waveform and the solution trajectory $y = (\omega_0/\omega_c)x$. For example, switching time instances for the NS double-edge modulation of the one-phase two-level inverter leg in **Figure 1** are defined from its unit cell in **Figure 3c** such that $f(x, y)$ changes

from $-V_{dc}$ to V_{dc} when $x = -\pi M \cos y$,

from V_{dc} to $-V_{dc}$ when $x = \pi M \cos y$.

3.1.2.2. Symmetrically regularly sampled PWM

Switching instances for SR PWM can be determined by the intersection between the sampled sinusoid waveform and the solution trajectory line $y = y' + (\omega_0/\omega_c)x$. The same switching instances can be determined as the intersection between the continuous sinusoid waveform and a staircase variable y' which has a constant value within each carrier interval [4]. In general, the value of y' within each carrier interval can be expressed as

$$y' = \frac{\omega_0}{\omega_c} 2p\pi, \quad p = 0,\ 1,\ 2,\ \ldots \tag{5}$$

where p represents the pth carrier interval within a fundamental cycle. The staircase variable y' in terms of continuous variables x and y is given by

$$y' = y - \frac{\omega_0}{\omega_c}(x - 2p\pi), \quad p = 0,\ 1,\ 2,\ \ldots. \tag{6}$$

The double Fourier series coefficients for the case of SR PWM with a triangle carrier can be found analogously to NS PWM with variable y substituted by variable y' found from Eq. (6).

Considering the previous example with the one-phase two-level inverter leg shown in **Figure 1**, switching time instances for the SR double-edge modulation are defined such that $f(x, y)$ changes

from $-V_{dc}$ to V_{dc} when $x = -\pi M \cos y'$,

from V_{dc} to $-V_{dc}$ when $x = \pi M \cos y'$.

3.1.2.3. Asymmetrically regularly sampled PWM

Switching time instances for AR PWM are determined similarly to SR PWM. Unlike SR PWM, switching occurs twice within each carrier interval for AR PWM. The switching time instances can be determined as the intersection between the continuous sinusoid waveform and two staircase variables

$$y_i' = \frac{\omega_0}{\omega_c}\left(2p\pi + (-1)^i \frac{\pi}{2}\right), \quad i = 1,\ 2, \tag{7}$$

which can be expressed in terms of continuous variables x and y as

$$y_i' = y - \frac{\omega_0}{\omega_c}\left(x - 2p\pi - (-1)^i \frac{\pi}{2}\right), \quad i = 1,\ 2. \tag{8}$$

To write the double Fourier series integral for AR PWM, the switched waveform in each carrier interval must be split into two sections for analysis, and with the results added by

superposition, the first section ($i = 1$) has modulated "rising" edge in the first half carrier interval and a "falling" edge in the center of the carrier interval. The second section ($i = 2$) has a modulated "rising" edge in the center of the carrier interval and "falling" edge in the second half carrier interval. Mathematically, this behavior can be expressed as a sum of two functions, $f_1(x, y)$ and $f_2(x, y)$, representing "rising" and "falling" edges of the double-edge carrier waveform $f(x, y) = f_1(x, y) + f_2(x, y)$.

In the previous example with the one-phase two-level inverter leg (**Figure 1**), functions $f_1(x, y)$ and $f_2(x, y)$ are defined as follows:

$f_1(x, y)$ steps from V_{dc} to $-V_{dc}$ at $x = x(y_1') + 2p\pi$ and from $-V_{dc}$ to V_{dc} at $x = 2p\pi$;

$f_2(x, y)$ steps from V_{dc} to $-V_{dc}$ at $x = 2p\pi$ and from $-V_{dc}$ to V_{dc} at $x = x(y_2') + 2p\pi$.

4. PWM for multilevel inverters

In this section, the following MLI topologies are presented: diode-clamped (DC) MLI, cascade H-bridge (CHB) MLI, and capacitor-clamped (CC) MLI. The three-level diode-clamped inverter, which is also called the neutral-point-clamped inverter, was initially introduced by Nabae et al. [8] in 1981. Thereafter, diode-clamped, cascade H-bridge, and flying capacitor MLIs with higher number of DC voltage levels have been developed [9–11].

4.1. Diode-clamped MLI

4.1.1. DCMLI circuit topology

A three-level diode-clamped inverter is shown in **Figure 4a**. In this circuit, the DC bus voltage is split into three levels by two series-connected bulk capacitors, C_1 and C_2. The middle point of the two capacitors n can be defined as a neutral point. The inverter has two complementary switch pairs: (S_1, S_3) and (S_2, S_4); the complementary switches cannot be turned on simultaneously. The output voltage v_a has three states: $-V_{dc}/2$, 0, and $V_{dc}/2$. For voltage level $V_{dc}/2$, switches S_1 and S_2 should be turned on; for $-V_{dc}/2$, switches S_3 and S_4 should be turned on; and for the 0 level, switches S_2 and S_3 should be turned on.

Figure 4b shows a five-level diode-clamped converter whose DC bus consists of four capacitors: C_1, C_2, C_3, and C_4. Here, the output voltage v_a has five levels: $-V_{dc}/2$, $-V_{dc}/4$, 0, $V_{dc}/4$, and $V_{dc}/2$. In this example, four complementary switches are (S_1, S_5), (S_2, S_6), (S_3, S_7), and (S_4, S_8). For voltage level $V_{dc}/2$, all upper switches S_1 and S_4 should be turned on; for voltage level $V_{dc}/4$, three upper switches S_2 and S_4 and one lower switch should be turned on; for voltage level 0, two upper switches S_3 and S_4 and two lower switches S_5 and S_6 should be turned on; for voltage level $-V_{dc}/4$, one upper switch S_4 and three lower switches S_5 and S_7 should be turned on; and for voltage level $-V_{dc}/2$, all lower switches S_5 and S_8 should be turned on.
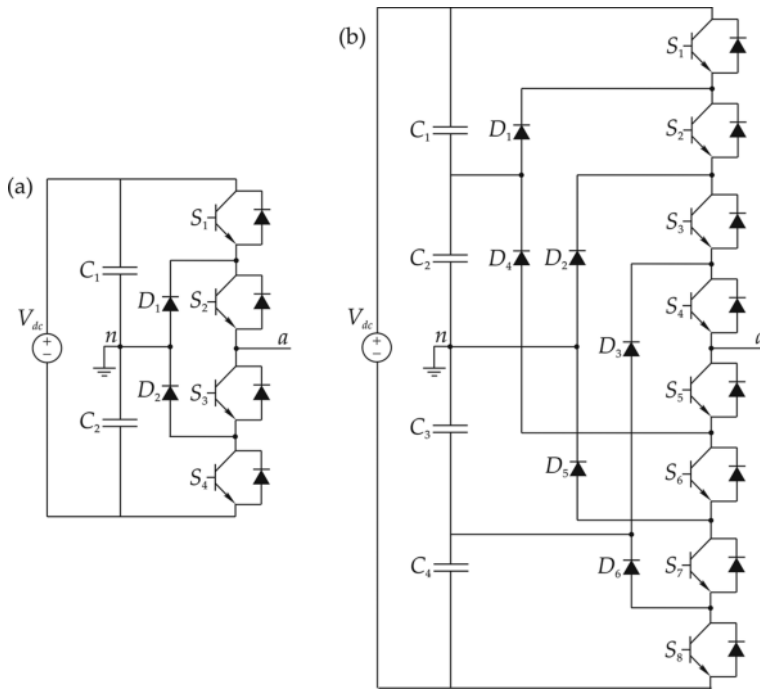
Figure 4. DCMLI circuit topologies: (a) three-level; (b) five-level.

Development of DCMLI of a higher level is constrained by diodes rating for reverse voltage blocking. The number of diodes increases quadratic in the level of inverter; therefore, construction of DCMLI beyond certain level will be impractical. Moreover, the diode recovery time is the major challenge in high-voltage high-power applications [12].

4.1.2. Carrier-based PWM schemes for DCMLIs

For DCMLIs, two or more carrier waveforms are used to modulate the target waveform. The number of waveforms depends on the level of the converter. Usually, the level of an inverter is an odd number, and if L is the level of the converter, then the number of carrier waveforms is $L-1$.

Carrier waveforms can be shifted with respect to each other. Based on the shift between the carrier waveforms, following modulation schemes are identified:

- phase opposition disposition (POD): all carrier waveforms above zero are in phase and 180° out of phase with those below zero;

- alternative phase opposition disposition (APOD): every carrier waveform is 180° out of phase with its neighbors;

- phase disposition (PD): all carrier waveforms are in phase.
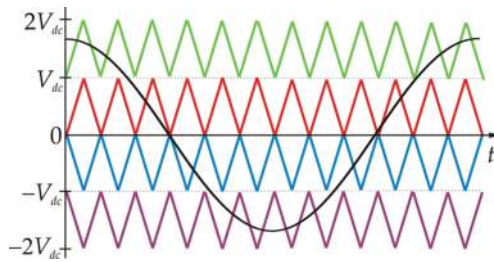
Figure 5. POD PWM scheme for a five-level inverter with the sinusoid reference waveform.
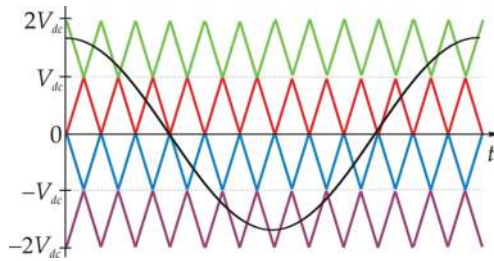
Figure 6. APOD PWM scheme for a five-level inverter with the sinusoid reference waveform.
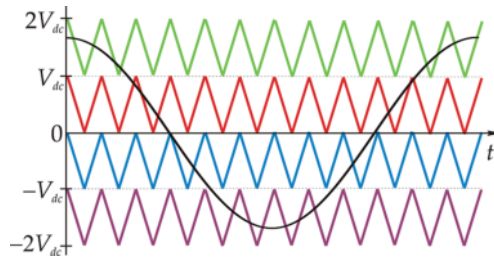

Figure 7. PD PWM scheme for a five-level inverter with the sinusoid reference waveform.

An example of each PWM scheme for a five-level inverter is shown in **Figures 5–7**. Apparently, there is no difference between POD and APOD for three-level inverters.

4.1.3. Contour plots for DCMLIs

If L is the level of the inverter, it denotes $N = (L-1)/2$. Then, function $f(x,y)$ of voltage level assumes one of the values: $-NV_{dc}/(L-1)$, $-(N-1)V_{dc}/(L-1)$, ..., 0, ..., $NV_{dc}/(L-1)$. Let us denote carrier waveforms as $x_1^c(t)$, $x_2^c(t)$, ..., $x_{L-1}^c(t)$ beginning from the lowest one. If the reference waveform is less than $x_1^c(t)$, then $f(x,y) = -NV_{dc}/(L-1)$; if the reference waveform is greater than $x_{i-1}^c(t)$ and less than $x_i^c(t)$, $i = 2$, ..., $L-1$, then $f(x,y) = -(N-i+1)V_{dc}/(L-1)$; and, finally, $f(x,y) = NV_{dc}/(L-1)$ if the reference waveform is greater than $x_{L-1}^c(t)$.

To determine the corresponding contour plot, interval $[-\pi; \pi]$ of the y-axis should be divided in $2N-1$ intervals with limits defined by $M\cos y = m/N$, $m = -N, -(N-1), \ldots, N$. One also needs to consider separately "rising" and "falling" edges of each carrier waveform corresponding to two intervals of variable x: $-\pi \leq x \leq 0$ and $0 \leq x \leq \pi$. Then, the condition that the reference waveform is greater than the carrier waveform $x_i^c(t)$ for "rising" and "falling" edges becomes, respectively:

$$NM\cos y > \frac{x_i^c}{\pi} \text{ if } 0 \leq x \leq \pi, \tag{9}$$

$$NM\cos y > -\frac{x_i^c}{\pi} \text{ if } -\pi \leq x \leq 0. \tag{10}$$

Similarly, the opposite conditions can be defined. Solving in Eqs. (9) and (10) for all values of $f(x,y)$, one can find the contour plot of a particular PWM scheme, accounting for the voltage level in each domain. Examples of different PWM schemes for three- and five-level diode-clamped inverter are given in **Figures 8–12**.
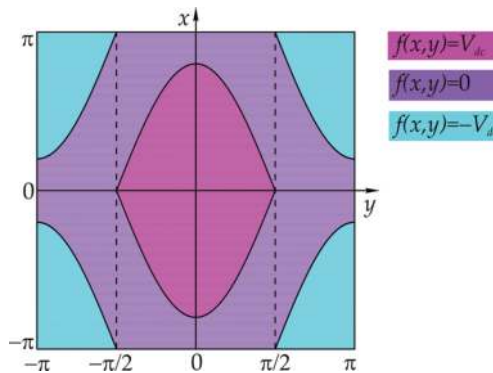
Figure 8. PD PWM scheme for a three-level diode-clamped inverter.
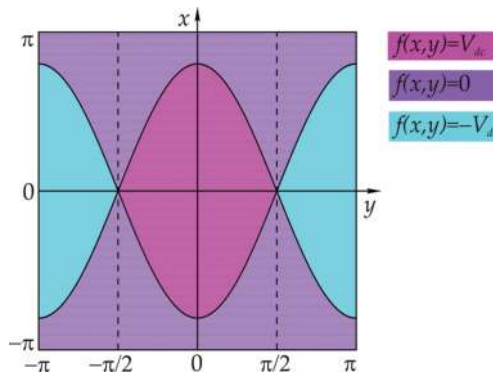
Figure 9. POD PWM scheme for a three-level diode-clamped inverter.
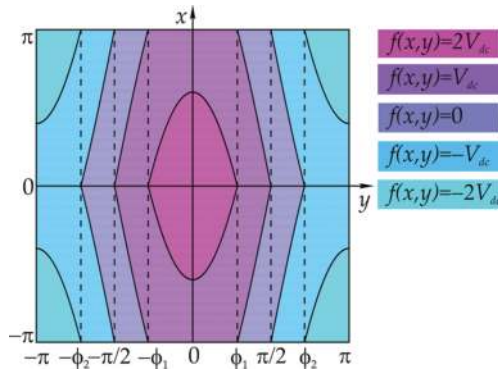
Figure 10. PD PWM scheme for a five-level diode-clamped inverter (here $\phi_2 = \pi-\phi_1$ and $\phi_1 = \cos^{-1}(1/2M)$).
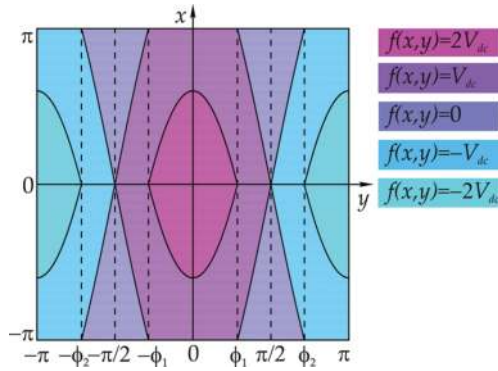

Figure 11. POD PWM scheme for a five-level diode-clamped inverter (here $\phi_2 = \pi-\phi_1$ and $\phi_1 = \cos^{-1}(1/2M)$).
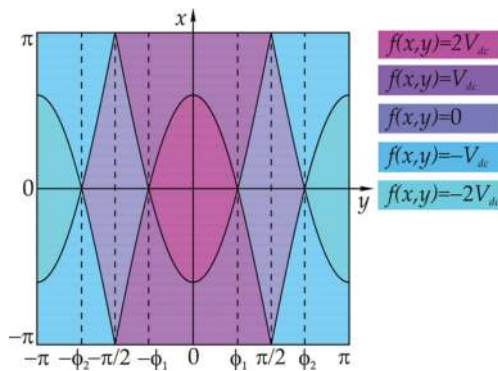

Figure 12. APOD PWM scheme for a five-level diode-clamped inverter (here $\phi_2 = \pi-\phi_1$ and $\phi_1 = \cos^{-1}(1/2M)$).

4.1.4. Harmonic spectra of DCMLIs

Once the unit cell with contour plots of voltage level domains for a particular PWM is obtained, harmonic components of the PWM can be found using Eq. (2) with the help of equations given in Section 2.2. Output voltage waveforms and their Fourier transforms are given below for three- and five-level diode-clamped inverters using different modulation strategies. Harmonic components magnitudes are plotted for first harmonic numbers assuming $M = 0.8$ and $\omega_c/\omega_0 = 40$.

The output voltage of a three-level diode-clamped inverter modulated by NS POD/APOD PWM is given by

$$v_a(t) = V_{dc}M\cos(\omega_0 t) + \frac{2V_{dc}}{\pi}\sum_{m=1}^{\infty}\frac{1}{m}\sum_{p=-\infty}^{\infty}(-1)^p J_{2p+1}(m\pi M)\cos(m\omega_c t + (2p+1)\omega_0 t) \qquad (11)$$

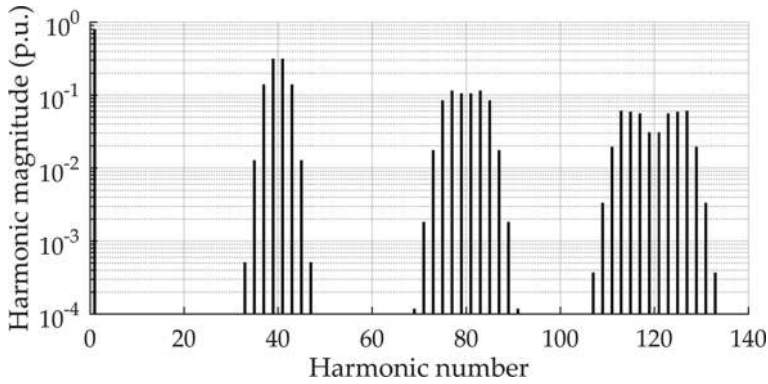and its harmonic components are plotted in **Figure 13**.

Figure 13. Theoretical harmonic spectrum of a three-level diode-clamped inverter modulated using NS POD/APOD PWM.

The output voltage of a three-level diode-clamped inverter modulated using NS PD PWM can be calculated as

$$v(t)a = V_{dc}M\cos(\omega_0 t) + \frac{2V_{dc}}{\pi}\sum_{q=1}^{\infty}\frac{1}{2q}\sum_{p=-\infty}^{\infty}\frac{J_{2p+1}(2q\pi M)(-1)^p}{2s+1}\cos(2q\omega_c t + (2p+1)\omega_0 t) +$$
$$+ \frac{4V_{dc}}{\pi^2}\sum_{q=1}^{\infty}\frac{1}{2q-1}\sum_{p=-\infty}^{\infty}\sum_{s=-\infty}^{\infty}\frac{J_{2s+1}((2q-1)\pi M)(-1)^p}{2p+2s+1}\cos((2q-1)\omega_c t + 2p\omega_0 t) \qquad (12)$$

and its theoretical harmonic spectrum is shown in **Figure 14**.

The output voltage of a five-level diode-clamped inverter obtained by NS POD PWM can be found as follows:
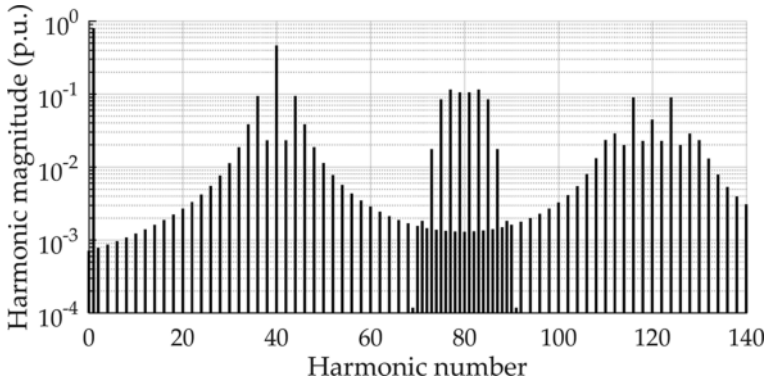
Figure 14. Theoretical harmonic spectrum of a three-level diode-clamped inverter modulated using NS PD PWM.

$$v_a(t) = 2V_{dc}M\cos(\omega_0 t) + \frac{2V_{dc}}{\pi}\sum_{q=1}^{\infty}\frac{1}{2q}\sum_{p=-\infty}^{\infty}(-1)^p J_{2p+1}(4q\pi M)\cos(2q\omega_c t + (2p+1)\omega_0 t) +$$

$$+ \frac{4V_{dc}}{\pi^2}\sum_{q=1}^{\infty}\frac{1}{2q-1}\sum_{p=-\infty}^{\infty}\left[\begin{array}{c}(-1)^p J_{2p+1}(2(2q-1)\pi M)\left(\dfrac{\pi}{2}-2\phi\right)\\ + \displaystyle\sum_{\substack{s=-\infty\\ s+p+1\neq 0}}^{\infty}(-1)^{s+1}J_{2s+1}(2(2q-1)\pi M)\dfrac{\sin(2(p+s+1)\phi)}{p+s+1}\end{array}\right], \quad (13)$$

where $\phi = \cos^{-1}(1/2M)$ and its harmonic spectrum is plotted in **Figure 15**.

The output voltage of a five-level diode-clamped inverter modulated by NS APOD PWM is given by

$$v_a(t) = 2V_{dc}M\cos(\omega_0 t) + \frac{2V_{dc}}{\pi}\sum_{m=1}^{\infty}\frac{1}{m}\sum_{p=-\infty}^{\infty}(-1)^{m+p}J_{2p+1}(2m\pi M)\cos(m\omega_c t + (2p+1)\omega_0 t) \quad (14)$$
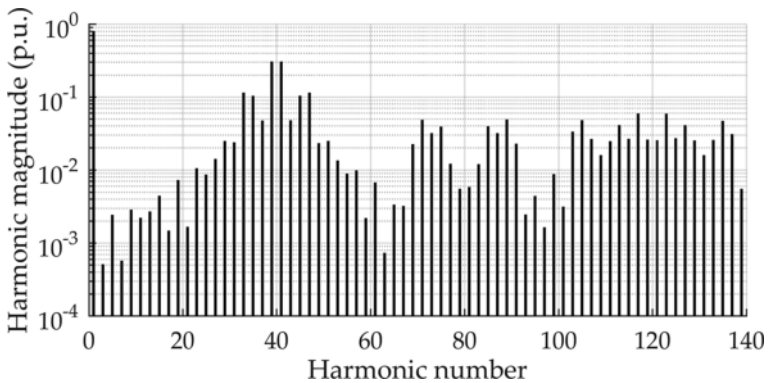
and its harmonics are plotted in **Figure 16**.

Figure 15. Theoretical harmonics spectrum of a five-level diode-clamped inverter modulated using NS POD PWM.
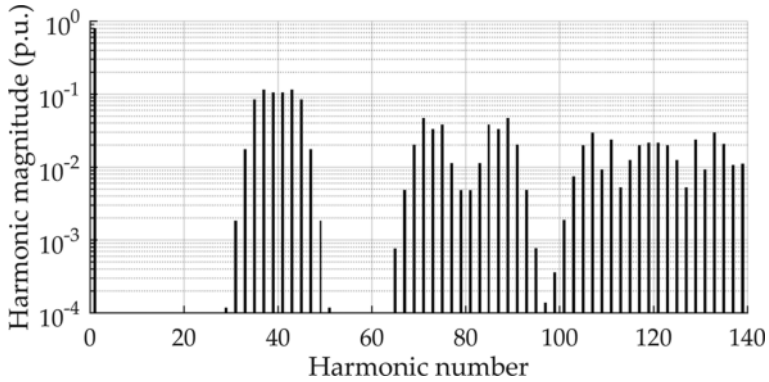
Figure 16. Theoretical harmonic spectrum of a five-level diode-clamped inverter modulated using NS APOD PWM.

The output voltage of a five-level diode-clamped inverter modulated using NS PD PWM is given by

$$v_a(t) = 2V_{dc}M\cos{(\omega_0 t)} + \frac{2V_{dc}}{\pi}\sum_{q=1}^{\infty}\frac{1}{2q}\sum_{p=-\infty}^{\infty}(-1)^p J_{2p+1}(4q\pi M)\cos{(2q\omega_c t + (2p+1)\omega_0 t)} +$$

$$+ \frac{4V_{dc}}{\pi^2}\sum_{q=1}^{\infty}\frac{1}{2q-1}\sum_{p=-\infty}^{\infty}\sum_{\substack{s=-\infty \\ 2p+2s\neq-1}}^{\infty}(-1)^s J_{2s+1}(2(2q-1)\pi M)\frac{\cos\left(\pi(p+s)\right)-2\sin{(\phi(2p+2s+1))}}{2p+2s+1}$$

$$\times \cos{((2q-1)\omega_c t + 2p\omega_0 t)} \tag{15}$$

where $\phi = \cos^{-1}(1/2M)$ and the theoretical harmonics spectrum is shown in **Figure 17**.
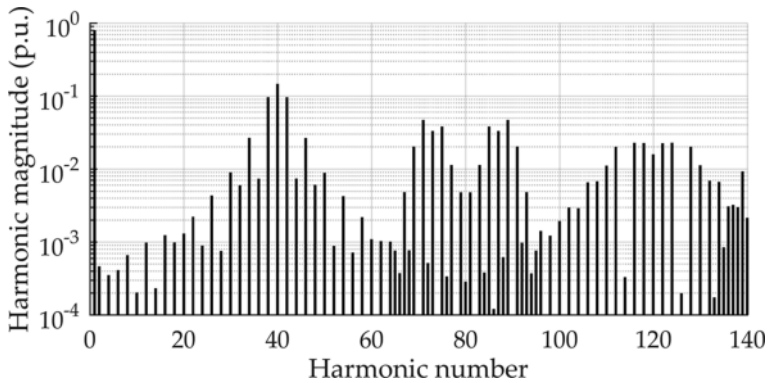

Figure 17. Theoretical harmonic spectrum of a five-level diode-clamped inverter modulated using NS PD PWM.

Below theoretical harmonic contents for SR and AR PWM are presented for a three-level diode-clamped inverter. The output voltage of a three-level diode-clamped inverter modulated with SR POD PWM can be found using

$$C_{m,2n+1} = \frac{2V_{dc}}{q\pi}(-1)^n J_{2n+1}(q\pi M) \tag{16}$$

where $q = m + n\omega_0/\omega_c$. Its harmonics content is shown in **Figure 18**.

The harmonic spectrum of a three-level diode-clamped inverter modulated with SR PD PWM can be determined by equations

$$C_{m,2p} = \frac{2V_{dc}}{\pi^2}\frac{1-e^{jq\pi}}{q}\sum_{k=-\infty}^{\infty}(-1)^p\frac{J_{2k+1}(q\pi M)}{2p+2k+1} \tag{17}$$

$$C_{m,2p+1} = \frac{V_{dc}}{\pi}\frac{1+e^{jq\pi}}{q}(-1)^p J_{2p+1}(q\pi M) \tag{18}$$

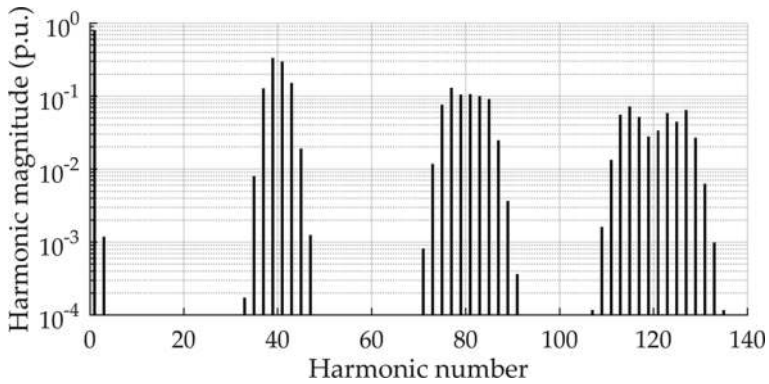where $q = m + n\omega_0/\omega_c$. First harmonics are plotted in **Figure 19**.

Figure 18. Theoretical harmonic spectrum of a three-level diode-clamped inverter modulated using SR POD PWM.
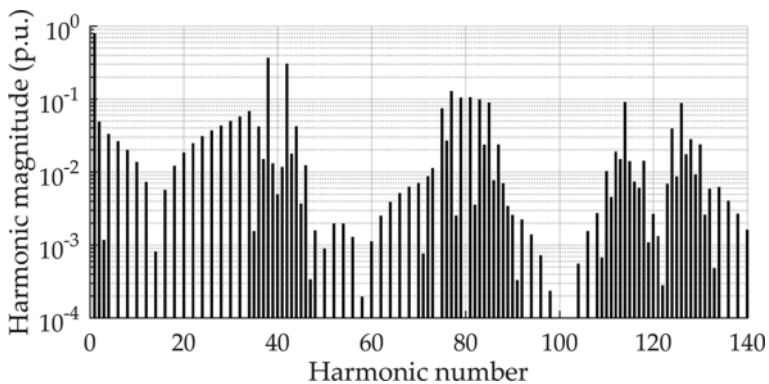

Figure 19. Theoretical harmonic spectrum of a three-level diode-clamped inverter modulated using SR PD PWM.

The harmonic spectrum of a three-level diode-clamped inverter modulated with AR POD PWM can be determined by equations

$$C_{mn} = \frac{2V_{dc}(1-e^{jn\pi})}{\pi^2 q} \left[\begin{array}{l} \frac{1}{n}\sin\left(n\frac{\pi\omega_0}{2\omega_c}\right)\sin\left(n\frac{\pi}{2}\right) + \frac{\pi}{2}J_n(q\pi M)\sin\left(n\frac{\pi}{2}\left[1-\frac{\omega_0}{\omega_c}\right]\right) + \\ + \sum\limits_{\substack{k=-\infty \\ n+k\neq 0}}^{\infty} \frac{1}{n+k}J_k(q\pi M)\sin\left(\frac{\pi}{2}\left[k-n\frac{\omega_0}{\omega_c}\right]\right)\sin\left((n+k)\frac{\pi}{2}\right) \end{array} \right] \tag{19}$$

where $q = m + n\omega_0/\omega_c$ and n is odd. A series of lower order harmonics are shown in **Figure 20**.
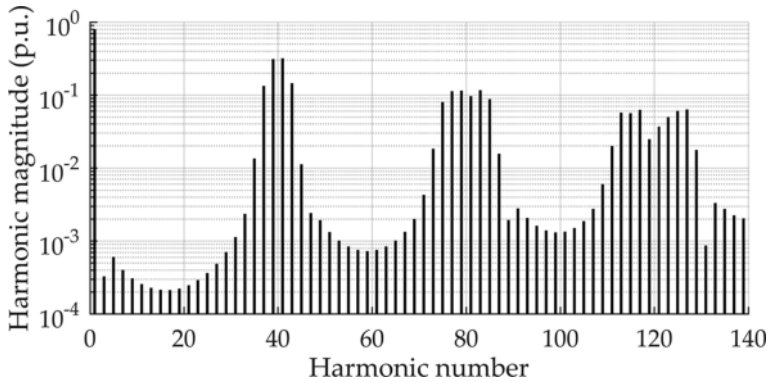

Figure 20. Theoretical harmonic spectrum of a three-level diode-clamped inverter modulated using AR POD PWM.

The harmonic spectrum of a three-level diode-clamped inverter modulated with AR PD PWM can be found using equations

$$C_{m0} = \frac{2V_{dc}}{\pi^2 q} \sum\limits_{s=-\infty}^{\infty} \frac{J_{2s+1}(q\pi M)}{2s+1}\left(1-e^{j(q+2s)\pi}\right) \tag{20}$$

$$C_{mn} = \frac{2V_{dc}(1+e^{jq\pi})}{\pi^2 q} \left[\begin{array}{l} \frac{1}{n}\sin\left(n\frac{\pi}{2}\frac{\omega_0}{\omega_c}\right)\sin\left(n\frac{\pi}{2}\right) + (-1)^{n+1}\frac{\pi}{2}J_n(q\pi M)\sin\left(n\frac{\pi}{2}\left[1+\frac{\omega_0}{\omega_c}\right]\right) \\ + \sum\limits_{k=-\infty, k\neq -n}^{\infty} \frac{(-1)^{k+1}}{n+k}J_k(q\pi M)\sin\left([n+k]\frac{\pi}{2}\right)\sin\left(\frac{\pi}{2}\left[k+n\frac{\omega_0}{\omega_c}\right]\right) \end{array} \right] \tag{21}$$

where $q = m + n\omega_0/\omega_c$ and n is odd in Eq. (21). A series of lower order harmonics are shown in **Figure 21**.

4.2. Cascaded H-Bridge MLI

4.2.1. CHBMLI circuit topology

A single-phase H-bridge inverter is shown in **Figure 22**. It is made up of two single-phase inverter legs (**Figure 1**) connected to a common DC bus. Each phase is modulated in complementary

pattern by a carrier/reference waveform comparison when the switching occurs as it is described above. A single-phase full-bridge inverter generates voltage of three levels: $-V_{dc}$, 0, and V_{dc}.
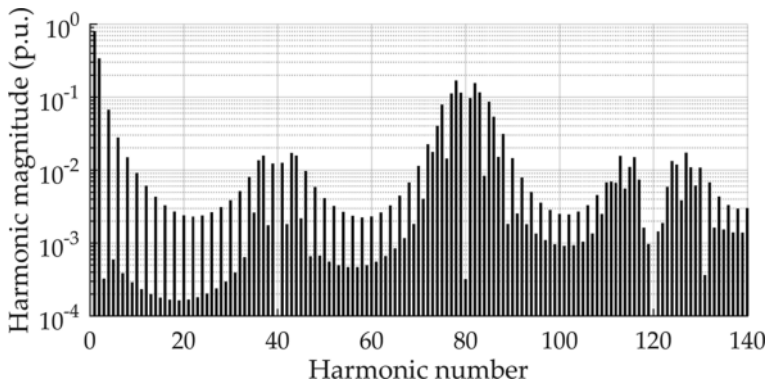

Figure 21. Theoretical harmonic spectrum of a three-level diode-clamped inverter modulated using AR PD PWM.
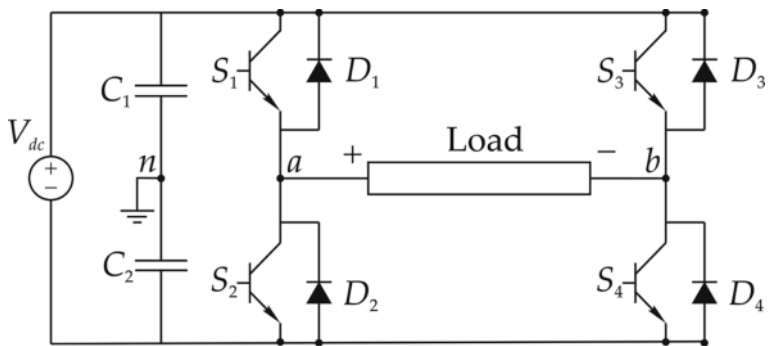

Figure 22. A single-phase H-bridge (full-bridge) inverter.

A cascaded H-bridge multilevel inverter, also called cascaded multicell inverters [12], consists of a number of series-connected single-phase H-bridge inverters connected to separate dc voltage sources. The resulting phase voltage is synthesized by addition of the voltages generated by different cells and is nearly sinusoidal even without filtering. An example of a five-level cascaded H-bridge inverter is shown in **Figure 23**.

Cascaded MLI topology has several advantages: each cell can be controlled independently from the others. Although communication between cells is required to achieve synchronized reference and carrier waveforms, controllers can be distributed. The control scheme is significantly easier than the ones for other topologies. However, it has not been used in practice in low power applications because a separate isolated dc voltage supply is needed for each full H-bridge [4].
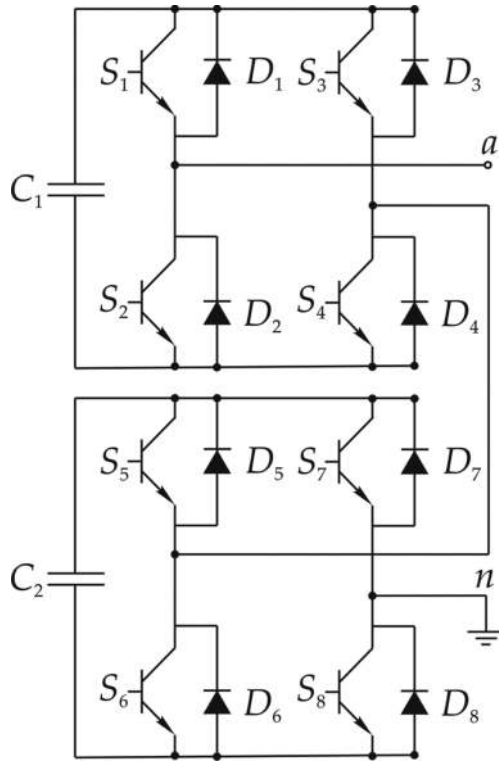
Figure 23. A five-level cascaded H-bridge inverter topology.

4.2.2. Carrier-based PWM schemes for CBHMLIs

Three-level modulation of a single-phase full-bridge inverter can be obtained via combination of voltage modulations of two phase legs a and b. The phase legs are modulated with 180 opposed reference waveforms given by

$$v_a^{id}(t) = \frac{V_{dc}}{2} M \cos y, \tag{22}$$

$$v_b^{id}(t) = \frac{V_{dc}}{2} M \cos (y - \pi). \tag{23}$$

The fundamental line-to-line (l-l) output reference voltage for the inverter is the difference between two phase reference voltages and is equal to

$$v_{ab}^{id}(t) = v_a^{id}(t) - v_b^{id}(t) = V_{dc} M \cos y. \tag{24}$$

Then, the l-l output voltage harmonic components for the inverter are given by

$$v_{ab}(t) = v_a(t) - v_b(t). \tag{25}$$

Applying different PWM schemes to a single-phase half-bridge inverter, one can obtain various modulations for the full-bridge inverter: NS, SR, and AR.

4.2.3. Harmonic spectra of CHBMLIs

The harmonic solution for NS PWM of a phase leg is given by

$$v_a(t) = \frac{V_{dc}}{2} + \frac{V_{dc}}{2} M \cos(\omega_0 t) + \frac{2V_{dc}}{\pi} \sum_{m=1}^{\infty} \frac{1}{m} \sum_{n=-\infty}^{\infty} J_n\left(m\frac{\pi}{2}M\right) \sin\left([m+n]\frac{\pi}{2}\right) \cos(m\omega_c t + n\omega_0 t). \tag{26}$$

Eq. (26) can be applied for each phase leg accounting for 180° phase shift of the reference waveforms resulting in the following harmonic spectrum for NS PWM of a full-bridge inverter:

$$v_{ab}^{NS}(t) = V_{dc}M \cos(\omega_0 t) + \frac{4V_{dc}}{\pi} \sum_{m=1}^{\infty} \frac{1}{2m} \sum_{n=-\infty}^{\infty} J_{2n+1}(2m\pi M) \cos([m+n]\pi) \cos(2m\omega_c t + [2n+1]\omega_0 t). \tag{27}$$

The harmonic spectrum of the output voltage of a full-bridge inverter modulated using SR PWM is equal to

$$v_{ab}^{SR}(t) = \frac{4V_{dc}}{\pi} \left[\sum_{n=1}^{\infty} \frac{J_n\left(n\frac{\omega_0}{\omega_c}\frac{\pi}{2}M\right)}{n\frac{\omega_0}{\omega_c}} \sin\left(n\left[1+\frac{\omega_0}{\omega_c}\right]\frac{\pi}{2}\right) |\sin n\frac{\pi}{2}| \cos(n\omega_0 t) \right.$$
$$\left. + \sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty} \frac{J_n\left(\left[m+n\frac{\omega_0}{\omega_c}\right]\frac{\pi}{2}M\right)}{m+n\frac{\omega_0}{\omega_c}} \sin\left(\left[m+n+n\frac{\omega_0}{\omega_c}\right]\frac{\pi}{2}\right) |\sin n\frac{\pi}{2}| \cos(m\omega_c t + n\omega_0 t) \right] \tag{28}$$

and using AR PWM it is given by

$$v_{ab}^{AR}(t) = \frac{4V_{dc}}{\pi} \left[\sum_{n=1}^{\infty} \frac{J_n\left(n\frac{\omega_0}{\omega_c}\frac{\pi}{2}M\right)}{n\frac{\omega_0}{\omega_c}} \sin\left(n\frac{\pi}{2}\right) \cos(n\omega_0 t) \right.$$
$$\left. + \sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty} \frac{J_{2n-1}\left(\left[m+n\frac{\omega_0}{\omega_c}\right]\frac{\pi}{2}M\right)}{m+n\frac{\omega_0}{\omega_c}} \sin\left([m+n]\frac{\pi}{2}\right) |\sin n\frac{\pi}{2}| \cos(m\omega_c t + n\omega_0 t) \right]. \tag{29}$$

It can be seen that all odd carrier and associated sideband harmonics as well as even sideband harmonics are cancelled out from the *l-l* output voltage. A further cancellation can be obtained by appropriately phase shifting the remaining harmonics of several series-connected single-phase H-bridges. This process is called phase-shifted cascaded (PSC) PWM. The major principle is that the phase shift between two phases of each H-bridge

cell is kept 180°, and then, carriers of each H-bridge are shifted with respect to each other. Optimum harmonic cancellation is achieved via phase shifting each carrier by $(i-1)\pi/N$, where i is the ith converter, N is the number of series-connected single-phase inverter legs, and $N = (L-1)/2$ and L is the number of voltage levels that can be achieved. This modulation is also called phase shift (PS) PWM. The overall cascaded inverter phase leg to dc link midpoint voltage can be obtained by adding up the l-l output reference voltages of each cell:

$$v(t) = \sum_{i=1}^{N} v_{ab}^i(t).$$ (30)

One can see in **Figures 24–32** that carrier harmonics of odd order and even order sideband harmonics are cancelled out in the three-level CHB inverter for all presented topologies, and increasing the level of the inverter is leading to cancelling out other carrier harmonics of order $m \neq kN, k = 1, 2, 3, \ldots$
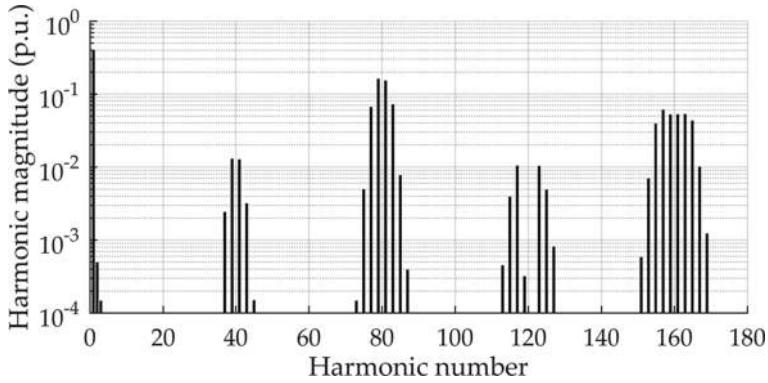

Figure 24. Theoretical harmonic spectrum of a single-phase half-bridge inverter modulated using NS PS PWM.
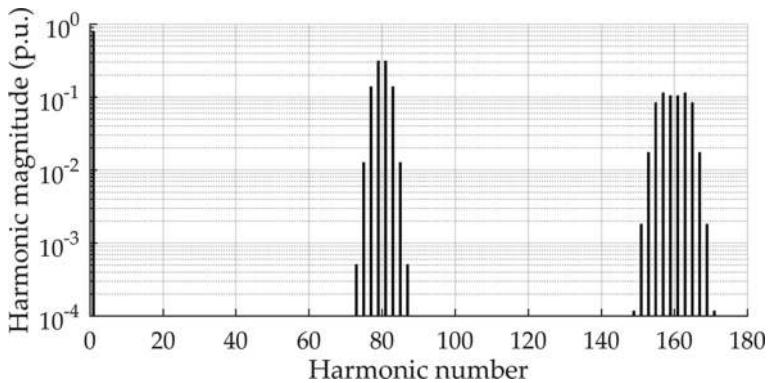

Figure 25. Theoretical harmonic spectrum of a single-phase full-bridge inverter modulated using NS PS PWM.
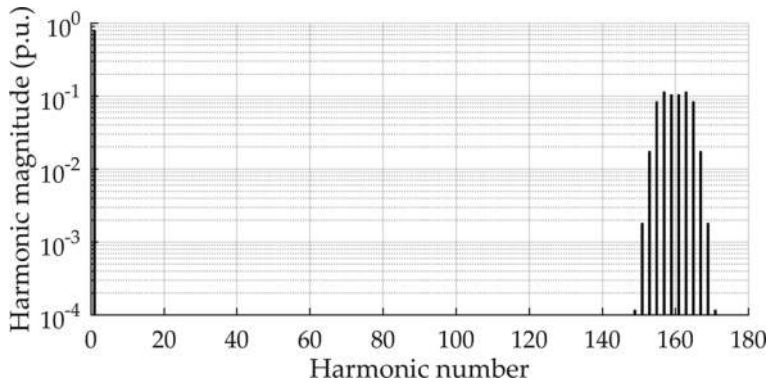
Figure 26. Theoretical harmonic spectrum of a single-phase cascaded H-bridge inverter modulated using NS PS PWM.

Figure 27. Theoretical harmonic spectrum of a single-phase half-bridge inverter modulated using SR PS PWM.

Figure 28. Theoretical harmonic spectrum of a single-phase full-bridge inverter modulated using SR PS PWM.

Figure 29. Theoretical harmonic spectrum of a single-phase cascaded H-bridge inverter modulated using SR PS PWM.
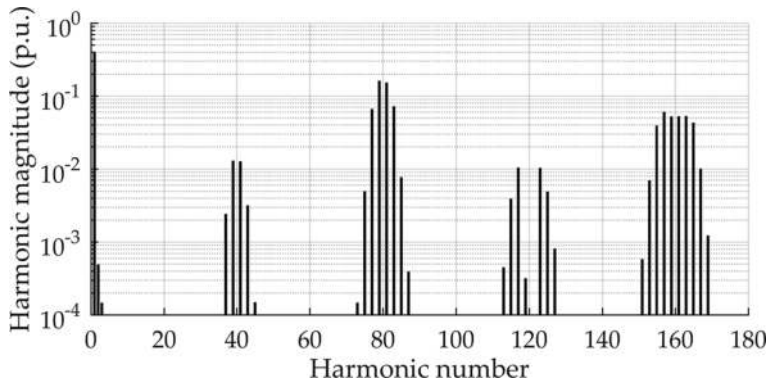

Figure 30. Theoretical harmonic spectrum of a single-phase half-bridge inverter modulated using AR PS PWM.

Figure 31. Theoretical harmonic spectrum of a single-phase full-bridge inverter modulated using AR PS PWM.

Figure 32. Theoretical harmonic spectrum of a single-phase half-bridge inverter modulated using AR PS PWM.
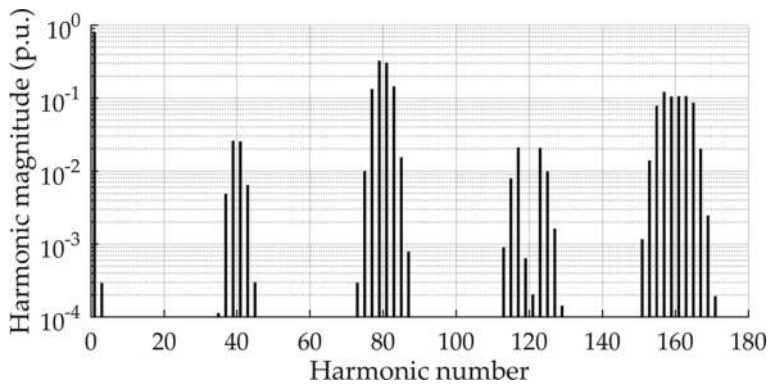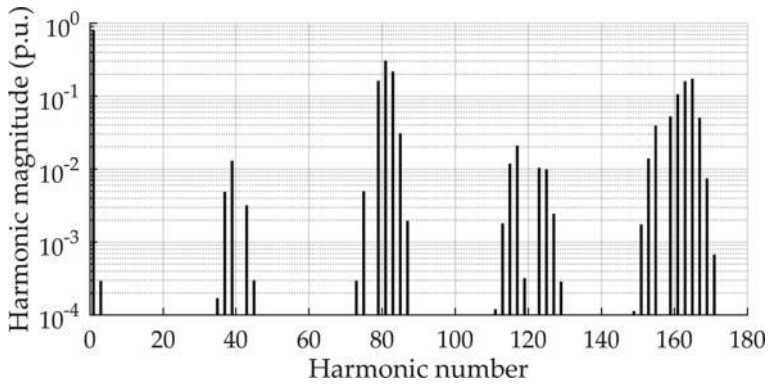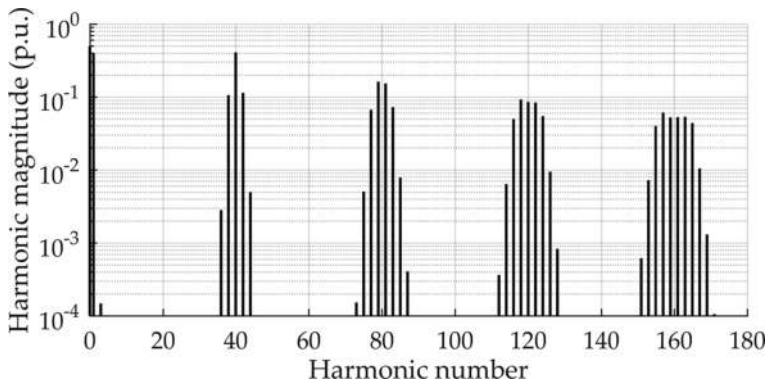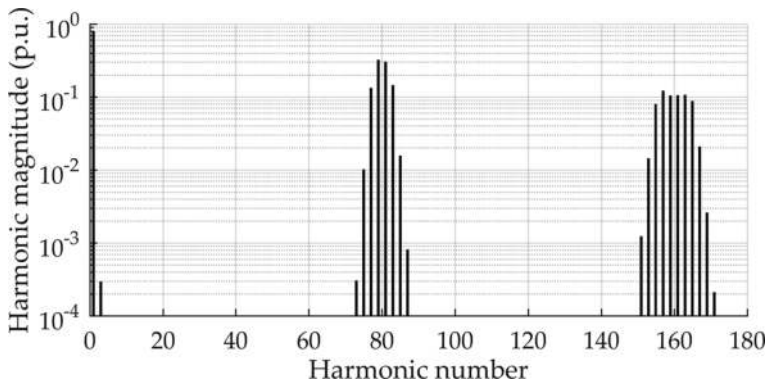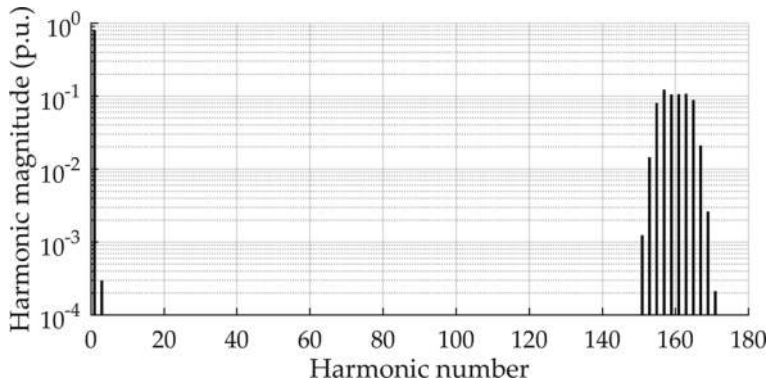
5. Harmonic distortion

Modern power electronic equipment operates in different discrete modes which causes a deviation of the output waveform from the desirable sine waveform due to insertion of undesirable harmonics. The rate of the deviation is presented by a number of basic indices characterizing the harmonic distortion. In particular, these indices enable us to compare the effectiveness of various inverter modulation algorithms. The indices are introduced in this section, and different inverter topologies are compared in their terms.

5.1. Harmonic distortion indices

Given that the output voltage $v(t)$ of a power converter is a periodic function with period T, the *root-mean-square* (RMS) value of the function is defined by

$$V_{rms} = \sqrt{\frac{1}{T}\int_0^T v(t)^2 \, dt}. \tag{31}$$

Since $v(t)$ is periodic with the Fourier series $v(t) = V_0 + \sum_{n=1}^{\infty} V_n \cos{(n\omega t + \varphi_n)}$, the Parseval's theorem can be used to find the RMS voltage of $v(t)$:

$$V_{rms} = \sqrt{V_0^2 + \sum_{n=1}^{\infty} \frac{V_n^2}{2}}. \tag{32}$$

In most of the practical cases, the fundamental harmonic V_1 can be considered as the desired output voltage. The reminder of this expression is then considered as a "distortion" to the output. Factoring out V_1 gives us

$$V_{rms} = V_{1,rms}\sqrt{1 + \frac{2V_0^2}{V_1^2} + \sum_{n=2}^{\infty}\left(\frac{V_n}{V_1}\right)^2}, \tag{33}$$

where $V_{1,rms} = V_1/\sqrt{2}$. The *total harmonic distortion* (THD) of the voltage is defined as

$$THD = \sqrt{\frac{2V_0^2}{V_1^2} + \sum_{n=2}^{\infty}\left(\frac{V_n}{V_1}\right)^2} \tag{34}$$

and the RMS voltage becomes

$$V_{rms} = V_{1,rms}\sqrt{1 + THD^2}. \tag{35}$$

For the purpose of comparing various switching strategies, the *weighted total harmonic distortion* (WTHD) is used:

$$WTHD = \frac{1}{V_1}\sqrt{\sum_{n=2}^{\infty}\left(\frac{V_n}{n}\right)^2} \tag{36}$$

In the case of pulse-width-modulated inverters, the DC voltage remains constant, while the fundamental component varies. On the other hand, for the same ratio of switching to output frequency, the harmonic components vary relatively little, resulting in a large variation of THD and WTHD. Therefore, a normalized WTHD can be used. For the case of half-bridge inverter, the normalization factor is chosen to be the value of the fundamental ac voltage when the modulation index M equals 1, that is, V_{dc}. Thus, the normalized WTHD, WTHD0, becomes

$$WTHD0 = \sqrt{\sum_{n=2}^{\infty}\frac{1}{n^2}\left(\frac{V_n}{V_{dc}}\right)^2} = WTHD\frac{V_1}{V_{dc}} = WTHD \cdot M. \tag{37}$$

5.2. Harmonic distortion indices for a DCMLI

Harmonic distortion indices for all presented inverter topologies and PWMs are provided in **Table 1**. Spectra are evaluated for $M = 0.8$ and $\omega_c/\omega_0 = 40$. It can be noted that a half-bridge inverters and full-bridge inverters demonstrate similar waveform quality regardless the PWM strategy applied. Cascaded H-bridge inverters show improvement in performance with increase in number of levels, which appears due to extensive harmonics cancelations up to harmonics of a high order. Performance of diode-clamped inverters also improves with increasing number of levels; however, the improvement is significantly lower than for the cascaded H-bridge inverters.

There is a substantial difference between different modulations used for the same converter. For example, AR PD is showing the worst performance among all other carrier-based

modulations of a three-level DC inverter which can be explained by the fact that very few harmonics are cancelled unlike the other modulations.

	V_{rms} (p.u.)	THD (%)	WTHD (%)	WTHD0 (%)
Three-level diode-clamped inverter phase leg				
NS POD/APOD PWM	0.6959	71.66	1.58	1.27
NS PD PWM	0.6959	71.65	1.58	1.27
SR POD/APOD PWM	0.6959	71.76	1.59	1.27
SR PD PWM	0.7003	73.23	3.70	2.96
AR POD/APOD PWM	0.6956	71.61	1.58	1.26
AR PD PWM	0.6131	42.37	1.82	1.46
Five-level diode-clamped inverter phase leg				
NS POD PWM	0.6790	65.91	1.57	1.26
NS PD PWM	0.6457	55.02	1.30	1.04
NS APOD PWM	0.6007	35.71	0.81	0.65
Five-level cascaded H-bridge inverter phase leg				
AR PS PWM	0.5929	31.44	0.20	0.16
SR PS PWM	0.6638	61.60	0.67	0.53
NS PS PWM	0.5930	31.43	0.20	0.16
Three-level cascaded H-bridge inverter phase leg				
AR PS PWM	0.6856	68.50	0.79	0.63
SR PS PWM	0.6856	68.67	0.79	0.64
NS PS PWM	0.6856	68.47	0.79	0.63
Single phase half-bridge inverter				
AR PWM	0.4796	136.98	2.87	2.30
SR PWM	0.4797	137.15	2.87	2.30
NS PWM	0.4796	136.93	2.87	2.30

Table 1. Harmonic distortion factors for MLI.

6. Conclusion

In this chapter, an application of double Fourier series to analytical analysis of power width modulation of power electronic converters was presented. The pulse width modulation concept was given, and different pulse width modulation schemes were described. Harmonic spectra and various distortion factors were calculated for various inverter topologies, namely three- and five-level diode-clamped inverters, three- and five-level cascaded H-bridge inverters, and modulated using different PWM schemes. PWM schemes performance varied for different converter topologies; therefore, the preferable PWM strategy is usually determined by a specific converter topology.

Comparing different topologies, the cascaded H-bridge topology contains the least number of sideband harmonics, and they can be further eliminated by increasing the number of levels of the inverter. DCMLIs and CCMLIs are constrained in the number of levels due to diodes physical properties.

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