

Chapter

Ultra-Low-Voltage IC Design Methods

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Abstract

The emerging nanoscale technologies inherently offer transistors working with low voltage levels and are optimized for low-power operation. However, these technologies lack quality electronic components vital for reliable analog and/or mixed-signal design (e.g., resistor, capacitor, etc.) as they are predominantly used in high-performance digital designs. Moreover, the voltage headroom, ESD properties, the maximum current densities, parasitic effects, process fluctuations, aging effects, and many other parameters are superior in verified-by-time CMOS processes using planar transistors. This is the main reason, why low-voltage, low-power high-performance analog and mixed-signal circuits are still being designed in mature process nodes. In the proposed chapter, we bring an overview of main challenges and design techniques effectively applicable for ultra-low-voltage and low-power analog integrated circuits in nanoscale technologies. New design challenges and limitations linked with a low value of the supply voltage, the process fluctuation, device mismatch, and other effects are discussed. In the later part of the chapter, conventional and unconventional design techniques (bulk-driven approach, floating-gate, dynamic threshold, etc.) to design analog integrated circuits towards ultra-low-voltage systems and applications are described. Examples of ultra-low-voltage analog ICs blocks (an operational amplifier, a voltage comparator, a charge pump, etc.) designed in a standard CMOS technology using the unconventional design approach are presented.

Keywords: analog/mixed-signal IC design, unconventional design approach, bulk-driven design, ultra-low-voltage, ultra-low-power, standard nanoscale CMOS technology

1. Introduction

The design of ultra-low-voltage (ULV) and low-power (LP) analog and mixed-signal ICs in modern nanotechnologies represents a real challenge for circuit designers and researches, since it introduces several limitations in numerous aspects. Firstly, since advanced nanoscale technologies offer a possibility to design analog, digital, and radio-frequency (RF) circuits as well as micro-electro-mechanical systems (MEMS) on a single chip, there is usually issue of a common value of the supply voltage. With the technology development, the value of the supply voltage is scaled down significantly. However, the threshold voltage (V_{TH}) of the MOS devices is *not* lowered at the same pace. This fact reduced the voltage headroom for conventional circuit topologies (e.g., cascode structures) to operate

correctly. Low value of the supply voltage may significantly influence the main parameters of analog ICs such as dynamic range (DR), power supply rejection (PSR), noise immunity, etc. The second limiting factor lies in the significant fluctuation of process parameters in nanoscale technologies that brings new requirements to IC design—circuits have to be robust enough against process, temperature, and voltage variations [1].

From the IC design point of view, one of the main problems caused by a lowered V_{DD} value is the reduction of useful voltage range for existing and standard circuit topologies. Analog circuits are suffering mostly from this limiting drawback. Decreasing the threshold voltage, as well as thinner layer of the gate oxide of a MOS (metal oxide semiconductor) transistor cause steep rising of the sub-threshold leakage current that is rather typical for nanotechnologies. These reasons do limit the further decrease of the threshold voltage. **Figure 1** depicts the dependency of the V_{DD} level and the threshold voltage on the technology node that is predicted for years to come by IRDS (International Roadmap for Devices and Systems). One can observe that the threshold voltage cannot follow the trend of the supply voltage level decrease due to substantial leakage currents.

The minimum power supply voltage of CMOS analog ICs designed without dedicated low-voltage (LV) techniques is limited by a value given by the sum of the turn-on voltage V_{GS} of MOS transistor and required voltage swing. For example, the voltage of ≈ 300 mV can be considered an average threshold voltage level in standard deep sub-micron CMOS fabrication process for transistors with reasonable channel length. This amount of external voltage applied between the gate and bulk terminal (or vice versa) is usually sufficient to introduce a strong inversion in the MOS structure and hence, turn-on the transistor. Another problem created by low supply voltages ($V_{DD} \approx 600$ mV and lower) is the limited voltage headroom for cascode circuit structures and stacked transistors [2]. Therefore, new design approaches focused on the low-voltage circuit topologies that can overcome limitations mentioned above are still required.

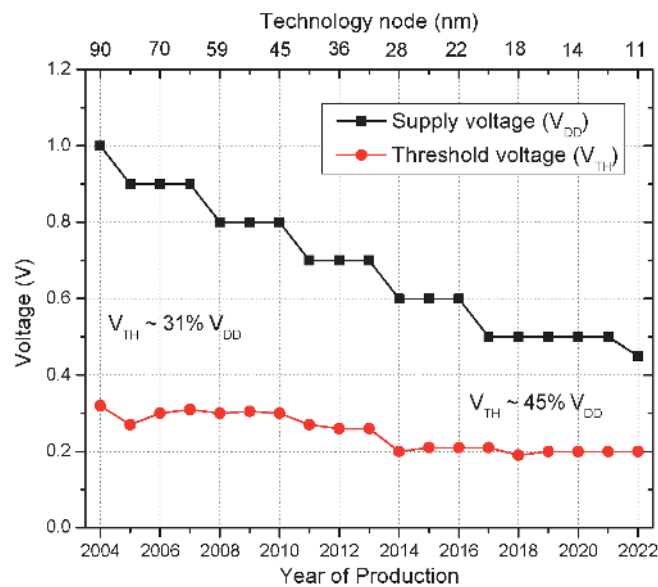


Figure 1. Scaling the supply voltage and threshold voltage in time.

2. Low-voltage design techniques and approaches

In this section, the survey of low-voltage design techniques and approaches that can be used in a standard CMOS technology (no additional process steps) are presented. Generally, low-voltage design techniques can be divided into two groups: conventional methods and unconventional ones. Unconventional methods include bulk-driven (BD) approach, dynamic threshold technique, floating-gate method, quasi-floating gate, and bulk-driven quasi-floating gate approaches. However, only the circuits designed by the bulk-driven and dynamic threshold approaches can be implemented in the standard CMOS technologies without any modification of the fabrication process. On the other hand, the conventional techniques such as circuits with rail-to-rail input/output operating range, MOS transistors working in sub-threshold region, level shifter techniques or MOS transistor in self-cascode structure represent commonly used approaches in the area of low-voltage IC design.

Since only circuits designed by the bulk-driven approach can be implemented in pure CMOS technology, in this chapter, we focus on this LV circuit design technique. At the end of this chapter, some examples of experimental and silicon-proven analog/mixed-signal circuits designed by the BD approach are presented.

2.1 MOS transistor in sub-threshold operation region

Firstly, it is vital to explain the operation regions of the MOS transistor, since this is the most important aspect for analog IC design. The optimum IC design is characterized by the minimum power consumption, minimum silicon area and sufficient frequency response, gain and other circuit specifications. Analog and mixed-signal circuit design procedure of systems using (ultra) low-power supply voltage introduces an extra layer of challenges for even seasoned circuit designers. The problems low supply voltage introduces, negatively influence several design considerations, circuit attributes and possible design options. The first and foremost is the substantially limited inversion level the MOS transistors operate in. This results, among others, in higher mismatch between transistor parameters, exponential temperature sensitivity, and drastically lowered operational frequency. We must not forget the increased silicon area requirements due to large transistors compensating for low transconductance values, increased noise and difficulties with precise secondary effects modeling. All of the above are typical drawbacks of low-voltage/low-power circuit design and their application [3]. The second issue is topological. It lies in constrained possible number of stacked transistors, in order to ensure their operation in saturation region. According to [4], the *theoretical* lower limit for saturation voltage of a MOS transistor in deep the sub-threshold region is defined as $V_{DSsat(min)} \approx 4 \cdot \frac{kT}{q}$, which at room temperature, equals to approximately 105 mV. However, with increasing inversion level, this value grows with square root trend.

The situation has been greatly improved by the development of design-oriented charge-sheet based EKV MOS transistor model (named after its authors—Enz-Krummenacher-Vittoz) [5]. EKV model defines the parameters of MOS device dependent on continuous range of inversion level unlike the industry-standard threshold voltage-based BSIM models. EKV model also introduced the so-called g_m/I_D design approach, which avails simple, yet accurate hand-calculations, straightforward transistor sizing and complete technology independence. In [4], the author defines the level of inversion, also called *inversion coefficient* (IC) of a MOS structure by Eq. (1).

$$IC = \left[\ln \left(1 + e^{\frac{V_{GS} - V_{TH}}{2n \cdot U_T}} \right) \right]^2 = \frac{I_D}{I_{technology} \cdot \frac{W}{L}}, \quad (1)$$

where V_{GS} is voltage between gate and source terminal of the MOS transistor, V_{TH} is a MOS transistor's threshold voltage, n is sub-threshold so-called slope factor, U_T is Boltzmann's thermal voltage (25.86 mV at room temperature), W is MOS transistor channel width, L is MOS transistor channel length, and $I_{specific}$ technology specific, current when a square MOS device ($W = L$) is in the middle of inversion range $IC = 1$.

The point when $IC = 1$ also determines the conditions when the drain diffusion current equals drain drift current. The interpolated dependency of *transconductance efficiency*— g_m/I_D as a function of IC is defined by Eq. (2). It represents very powerful formula since it is completely technology independent [6]. Furthermore, it can be easily implemented into a spreadsheet, introducing automated calculations and transistor sizing.

$$\frac{g_m}{I_D} = \frac{1}{n \cdot U_T \cdot \left(\frac{1}{2} + \sqrt{\frac{1}{4} + IC} \right)} \quad (2)$$

Figure 2 depicts the dependency of g_m/I_D on the inversion coefficient— IC , governed by Eq. (2). The area where $IC \leq 0.1$ represents the sub-threshold operation region that is also called *weak inversion*. The MOS transistor operating under these conditions exhibits high voltage gain, low drain current, low saturation voltage but also large dimensions in order to compensate low transconductance and very low cut-off frequency. When inversion coefficient becomes $IC \geq 10$, the MOS devices is operating in *strong inversion* or above the threshold voltage—the traditional working conditions. MOS transistor can process signals at high frequencies and does not require much of silicon area. However, the gain lowers and the drain current increases. The region in between of the weak and strong inversion ($0.1 \leq IC \leq 10$) describes a smooth transition between these two states. It is often called a *moderate inversion* and it represents a very good trade-off of the transistor and circuit parameters. Furthermore, the modern nanoscale CMOS technologies, working with lowered power supply voltage, are shifting the transistor operation into the

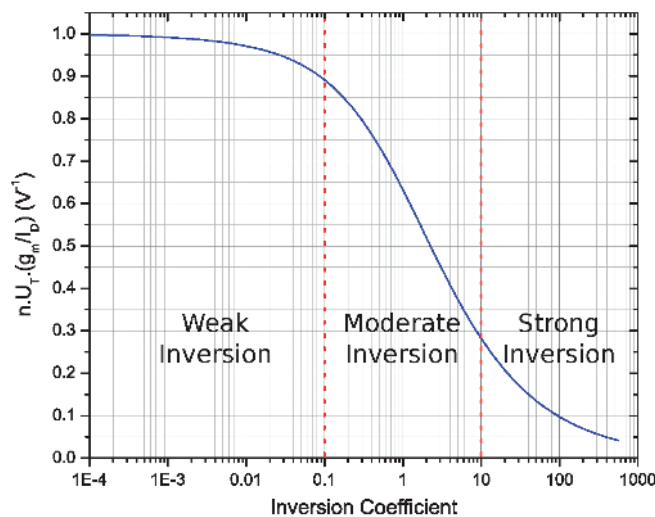


Figure 2.
 g_m/I_D as a function of inversion coefficient— IC .

moderate inversion, as the voltage headroom decreases and the level of the threshold voltage remains fairly constant over time (**Figure 1**).

2.2 Bulk-driven design approach

In the conventional approaches, MOS transistor is usually controlled by its gate potential. However, the current flowing through the device can also be modulated by the bulk-source voltage V_{BS} , which is usually considered a parasitic effect and may introduce undesired body transconductance g_{mb} . In the BD design approach, the input signal is applied to the transistor bulk, while a bias voltage is connected to the gate in order to establish a channel between the source and drain terminals. If a constant V_{GS} is kept as the bias voltage and the input signal is applied to the bulk electrode, then a JFET-like transistor behavior can be obtained. In other words, the inversion channel width is modulated according to the voltage applied to the bulk. Using the bulk as the signal input results in significantly reduced need to overcome the threshold voltage at the MOS transistor.

The effect of the V_{BS} on the drain current is embedded in the threshold voltage V_{TH} . The threshold voltage of MOS transistor can be expressed by Eq. (3). It also serves as *very important* link between g_m/I_D , IC and bulk-driven design approaches.

$$V_{TH} = V_{TH0} \pm \gamma \left(\sqrt{2|\Phi_F| - V_{BS}} - \sqrt{2|\Phi_F|} \right), \quad (3)$$

where V_{TH0} is the threshold voltage with $V_{BS} = 0$ V, γ is technology-specific body factor, and Φ_F is technology-specific Fermi's potential.

Thus, changes in V_{BS} value will result in modification of V_{TH} , which will inevitably modify the inversion coefficient according to Eq. (1) and finally, control the MOS transistor drain current.

In order to analyze the properties of a MOS transistor driven by the bulk terminal, the conventional gate-driven and bulk-driven single stage common-source amplifiers, depicted in **Figures 3** and **4**, have been investigated and compared.

From **Figures 3** and **4**, it can be observed that the input capacitance of the BD single stage amplifier will be higher than in the case of the GD amplifier. It is caused by a parasitic capacitance C_{bsub} between the bulk and substrate terminals. In the case of the GD amplifier, the input capacitance depends on C_{gs} and C_{gd} capacitances, while the BD amplifier has the input capacitance dependent on the bulk-source C_{bs} , bulk-drain C_{bd} and bulk-substrate C_{bsub} capacitances combined together.

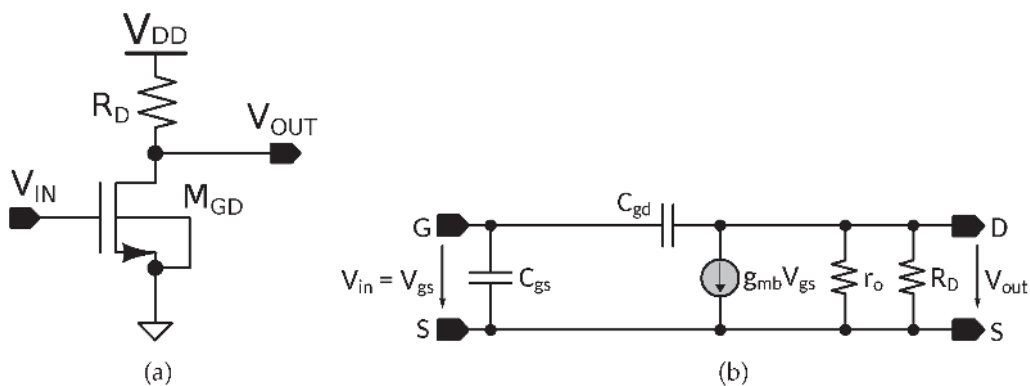


Figure 3. Gate-driven common-source amplifier. (a) Schematic diagram, and (b) Small-signal model.

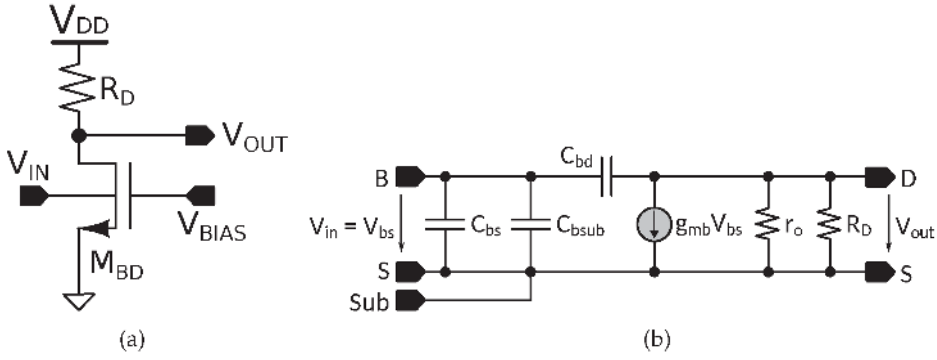


Figure 4. Bulk-driven single stage amplifier. (a) Schematic diagram, and (b) Small-signal model.

The transconductance of the conventional GD transistor can be expressed by the following Eq. (4)

$$g_m = \beta \frac{W}{L} \cdot (V_{GS} - V_{TH}) \quad (4)$$

It is important to point out that Eq. (4) is only valid when the MOS transistor operates in the strong inversion. In the weak inversion, the transconductance is proportionally dependent on the drain current, as given by Eq. (5).

$$g_{m_{wi}} = \frac{I_{DS_{wi}}}{n \cdot U_T} \quad (5)$$

The relationship between the transconductance of a GD transistor g_m and BD transistor g_{mb} is given by Eqs. (4) and (6).

$$g_{mb} = \frac{\gamma}{2\sqrt{|2\phi_F - V_{bs}|}} \cdot g_m$$

$$g_{mb} = \frac{C_{btot}}{C_{gtot}} \cdot g_m \quad (6)$$

$$g_{mb} \approx (0.2 \div 0.3) \cdot g_m$$

where C_{btot} and C_{gtot} are the total parasitic capacitances between bulk and channel and gate and channel, respectively. It can be observed that transconductance of the BD MOS transistor is only 20–30% of transconductance of the GD MOS transistor.

In order to determine the frequency performance of the BD transistor, schematic diagram, and small-signal model (depicted in **Figure 5**) have to be employed. Using small-signal model, the transition frequency $f_{T,BD}$ of the BD MOS transistor can be obtained. Firstly, it is important to define the transition frequency of the GD MOS transistor given by Eq. (7).

$$f_{T,GD} = \frac{g_m}{2\pi C_{gs}} \quad (7)$$

The transfer function and current gain of the BD MOS transistor can be expressed by Eq. (8).

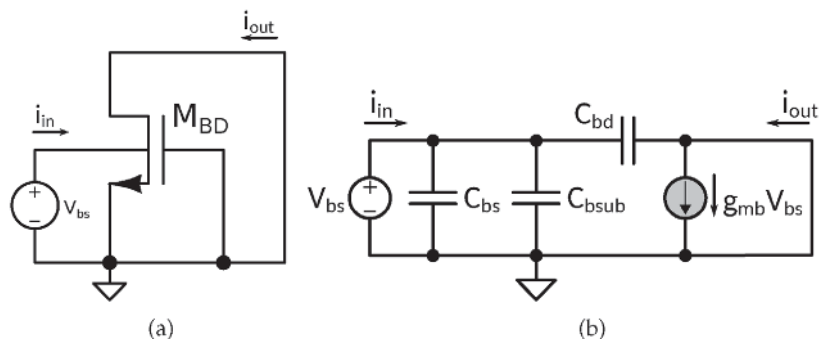


Figure 5. Schematic diagram and small-signal model for $f_{T,BD}$ calculation. (a) Schematic diagram, and (b) Small-signal model.

$$\frac{i_{out}}{i_{in}} \approx \frac{g_{mb} \cdot V_{bs}}{j\omega(C_{bs} + C_{bsub} + C_{bd}) \cdot V_{bs}} \quad (8)$$

$$\frac{i_{out}}{i_{in}} \approx \frac{g_{mb}}{j\omega(C_{bs} + C_{bsub} + C_{bd})}$$

If we consider that unity small-signal gain is obtained at frequency $\omega_{T,BD}$, the transition frequency of the BD MOS transistor can be expressed as follows:

$$f_{T,BD} = \frac{1}{2\pi} \cdot \omega_{T,BD}$$

$$f_{T,BD} = \frac{g_{mb}}{2\pi(C_{bs} + C_{bsub} + C_{bd})} \quad (9)$$

$$f_{T,BD} \approx (0.2 \div 0.3) \cdot f_{T,GD}$$

As can be observed from Eq. (9), the transition frequency of the BD MOS transistor is about five times lower than in the case of a MOS transistor driven by gate terminal. Another important parameter of the amplifier is the noise introduced into the circuit by the active component. The input referred noise of the GD MOS transistor depends on the current i_{ds} and transconductance g_m , and can be expressed as follows:

$$v_{noise}^2 = \frac{i_{ds}^2}{g_m^2} \cdot o \quad (10)$$

Similarly, the input referred noise of the BD MOS transistor is given by Eq. (11), where one can observe that the BD MOS transistor suffers from higher noise due to the lower transconductance g_{mb} .

$$v_{noise,BD}^2 = \left(\frac{g_m}{g_{mb}}\right)^2 \cdot v_{noise}^2 \quad (11)$$

The small-signal output resistance for both GD and BD transistors is identical, and given by Eq. (12).

$$r_o = \frac{1}{\lambda I_{DS}} = \frac{V_A}{I_{DS}}, \quad (12)$$

where V_A represents early voltage and I_{DS} is the current flowing through the MOS transistor. As mentioned above, the BD technique uses bulk terminal for the

signal input, which results in significantly reduced need to overcome the threshold voltage at the MOS transistor input, as a whole. In summary, we can state the important advantages of the BD design technique, which include the following:

- BD MOS transistor depletion characteristics significantly reduce the need to overcome the threshold voltage V_{TH} at the transistor input and increases the voltage headroom for low-voltage applications.
- Suitable for rail-to-rail voltage range.
- Better linearity due to low, transconductance (g_{mb}).
- Possibility to operate with a low value of the power supply.
- Easy to implement in a standard CMOS technology (twin-well process, both MOS devices available).

Unfortunately, if compared to traditional GD design approach, the bulk-driven design method also exhibits the following disadvantages:

- Body transconductance g_{mb} of the BD MOS transistor is 4–5 times lower than the gate transconductance g_m , which leads to inferior frequency response and decreased gain-bandwidth product.
- Input capacitance of the BD MOS transistor is greater, if compared to the traditional GD device.
- Input noise of the BD MOS transistor is increased.
- BD MOS transistors fabricated in a standard CMOS process are prone to the catastrophic latch-up effect.

The last drawback, however, can be effectively mitigated by lowering the power supply voltage below the threshold voltage of a PN junction or by usage of an expensive silicon-on-insulator (SOI) fabrication process. This step would prevent the turn-on of the parasitic bipolar transistor in the substrate.

3. Design examples of low-voltage analog ICs

In this section, several design examples and circuit topologies of basic analog IC building blocks using bulk-driven approach are presented. The described blocks have been silicon-proven through fabrication in a standard CMOS nanotechnology and measurement evaluation of the chip prototypes.

3.1 BD current mirrors

One of the most widely used circuit structures employed in IC design are arguably the current mirrors (CM). It is a two-port circuit, which processes the input current I_{REF} and generates the output current I_{OUT} based on the formula $I_{OUT} = k \cdot I_{REF}$, where k denotes an amplification (or mirroring) coefficient. **Figure 6** depicts the BD configuration of a simple CM. Obviously, more complicated CM structures can be designed using bulk-driven transistors [7].

almost perfectly constant transconductance g_{mb} . The disadvantage of presented topology is linked to the grounded gate terminals of the differential transistor pair. This way, the ground noise will be picked up by the transistors, which degrades the power supply rejection ratio (PSRR) [8]. An example of the BD differential pair use was published in [9], where it was used as the input pair of a variable-gain amplifier (VGA).

3.3 Variable-gain amplifier (VGA)

3.3.1 Description of BD VGA

Figure 8 shows the block diagram of a two-stage VGA. The first stage is formed by a variable-gain differential difference amplifier (DDA) designed using BD approach. The second stage has a fixed gain and is created by a BD common-source amplifier (CSA). For stabilization of the operational point of both stages, two BD common-mode feedback (CMFB) circuits have to be employed. To achieve good stability of the CMFB loop as well as the whole two-stage VGA, frequency compensation circuitry has been applied.

The schematic diagram of the low-voltage VGA circuit is depicted in **Figure 9**. The input stage of the proposed topology is formed by DDA with bulk-driven MOS transistors, in order to obtain rail-to-rail input voltage range. The negative aspect of this solution lies in the reduced voltage gain and the gain-bandwidth product (GBW) [8]. Therefore, it is safe to state, that the proposed approach is suitable for low-voltage and low-frequency applications.

In general, the overall VGA voltage gain can be controlled by adjusting either the total conductance or the total output impedance [8]. Thus, transistors M5 and M6 were employed to control the VGA gain. Modification of control voltage V_{CTRL} modulates the current flow through the input devices M1 and M2, which eventually changes their effective transconductance. This will, in effect, vary the voltage amplification of the first stage, which will result in modification of overall gain of the proposed VGA. The total VGA voltage gain is directly proportional to the transconductance of the gain control devices g_{m5} and g_{m6} . The input transistors along with the gain control devices form a cascode configuration, hence their small-signal parameters affect the overall output resistance of the first stage. Detailed small-signal analysis of the complete VGA is conducted in the following subsection. The second stage represents a BD common-source stage with the fixed gain that offers rail-to-rail input voltage range and a wide swing (nearly rail-to-rail) at the VGA output. Two CMFB circuits were used to achieve the stable operational point of both VGA stages.

Figure 9 depicts the implemented frequency compensation circuit. The second amplification stage of the proposed VGA consists of devices M9–M12 and transistors M13–M16 along with capacitors C_c are responsible for the stability of the whole

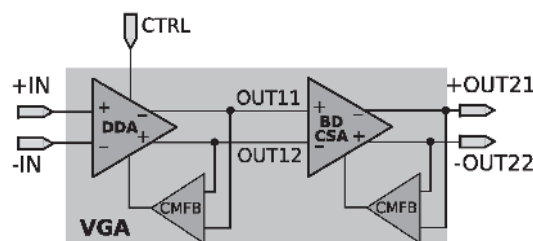


Figure 8.
Block diagram of VGA.

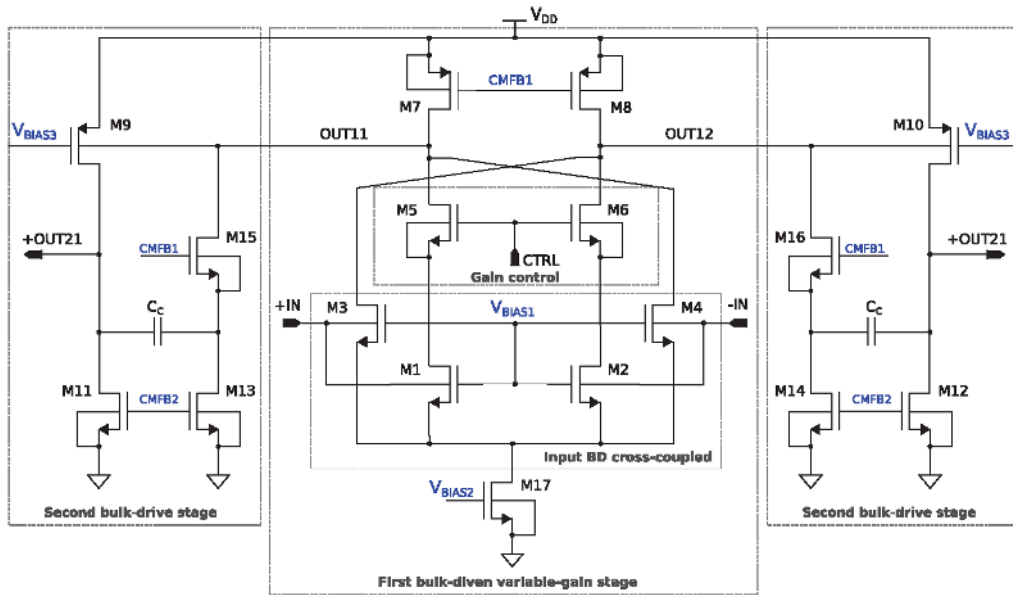


Figure 9.
 Schematic diagram of VGA.

circuitry. The proposed compensation approach removes the feed-forward path between the outputs of both amplifying stages by introducing a sufficient voltage gain the feedback path (transistor M15 and M16). The position of the dominant pole is, therefore, maintained, but the position of the output pole gets shifted by the factor of introduced gain. The compensation capacitor C_c is employed between the virtual ground handled by the devices M13 and M14, and the output node of the VGA.

3.3.2 Design principle of VGA based on small-signal analysis

From the design point of view, it is important to ensure good stability and investigate the parameters that influence the gain of the proposed two-stage VGA. For this purpose, the small-signal model of VGA shown in **Figure 10** was used. We have to note that the output capacitance of the first stage was neglected. Thanks to the overall symmetry of the topology, we can perform the small-signal analysis just for one half-circuit and investigate the influence of $+V_{in}$ and $-V_{in}$ separately. The total voltage gain will be, therefore, equal to the sum of the partial contributions of the respective gain stages.

The resulting formula defining the total DC gain of the discussed VGA is follows:

$$A_v = G_{m1}R_{out1} \cdot G_{m2}R_{out2} = A_1 \cdot A_2 \quad (14)$$

where A_1 and A_2 is gain of the first stage and the second stage, respectively. The total transconductance and the total output resistance of the first VGA stage are denoted as G_{m1} and R_{out1} , respectively. The same parameters associated with the second stage are named G_{m2} and R_{out2} . The impact of frequency compensation block has been neglected for additional simplification of the small-signal analysis Eq. (14).

G_{m1} and G_{m2} depicted in **Figure 10** are defined follows:

$$G_{m1} = g_{mb1} \cdot \frac{g_{m5}}{g_{ds1} + g_{m5}} - g_{mb4} = g_{mb1} \cdot C - g_{mb4} \quad (15)$$

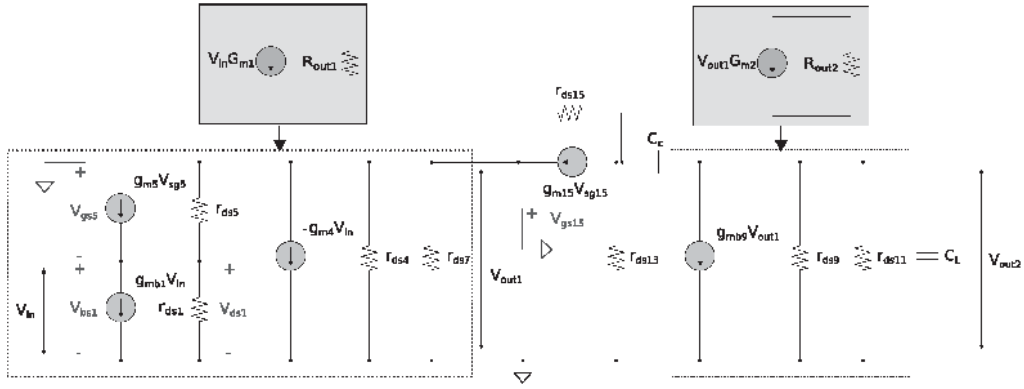


Figure 10.
Small-signal model of the VGA.

$$G_{m2} = g_{mb9} \quad (16)$$

where g_{mb1} , g_{mb4} , and g_{mb9} are bulk transconductance of transistors M1, M4, and M9, g_{m5} is a transconductance of transistor M5, while g_{ds1} and g_{ds5} are output transconductance of transistors M1 and M5, respectively. In Eq. (15), we consider that $g_{m5} \gg g_{ds5}$. The total transconductance of the first stage can be varied by the transconductance of transistor M5, while the second stage has a fixed value of transconductance.

$$C = \frac{g_{m5}}{g_{ds1} + g_{m5}} = \frac{1}{1 + \frac{g_{ds1}}{g_{m5}}} \quad (17)$$

One can observe that the total transconductance of VGA (G_{m1}) can be controlled by transconductance g_{m5} , which depends on the control voltage (CTRL). **Figure 11** shows the dependence of the total transconductance G_{m1} on the coefficient C that can vary in the range from 0 to 1. If $g_{m5} \ll g_{ds1}$, the coefficient C from Eq. (17) becomes zero and the total transconductance of VGA will be equal to $-g_{mb3}$. In the opposite case (when $g_{m5} \gg g_{ds1}$), coefficient C is equal to 1 and G_{m1} will be equal to $g_{mb1} - g_{mb3}$. This means that by increasing the transconductance g_{m5} , the total transconductance G_{m1} is decreased.

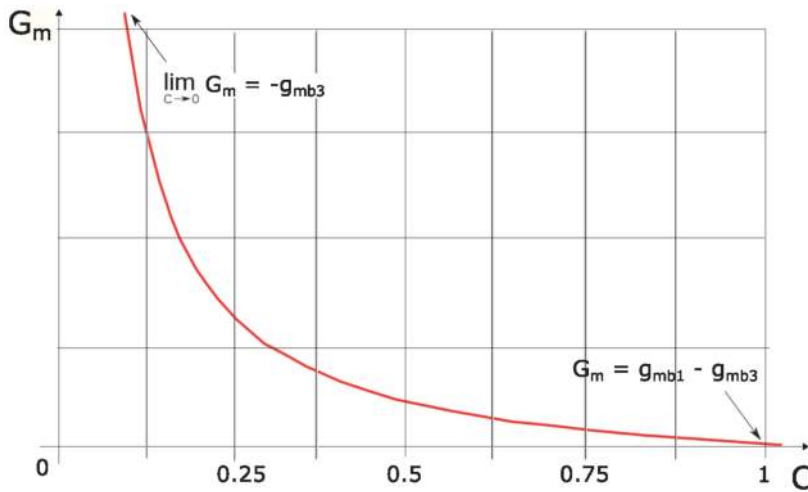


Figure 11.
Transconductance G_{m1} versus the coefficient C .

Besides, the total transconductance G_{m1} also depends on g_{ds1}/g_{m5} ratio. If numerator and denominator of the ratio are divided by I_{ds1} , the following expression can be written:

$$\frac{g_{ds1}}{g_{m5}} = \frac{\frac{g_{ds1}}{I_{ds1}}}{\frac{g_{m5}}{I_{ds1}}} = \frac{V_{CTRL} - V_{TH1}}{2 \cdot (V_{A1} + V_{ds1})}, \quad (18)$$

where V_{CTRL} is the control voltage of VGA, and V_{TH1} , V_{A1} , and V_{ds1} is the threshold voltage, Early voltage and voltage between source and drain of transistor M1, respectively. From Eq. (18), it can be observed that g_{ds1}/g_{m5} ratio, which controls the total transconductance G_m , depends on the control voltage of the proposed VGA. Using the small-signal model depicted in **Figure 10**, the output resistances R_{out1} and R_{out2} of the proposed VGA are expressed as

$$R_{out1} = \underbrace{\left[(1 + g_{m5}r_{ds1})r_{ds5} + r_{ds1} \right]}_A \parallel \underbrace{r_{ds4} \parallel r_{ds7}}_B, \quad (19)$$

$$R_{out2} = r_{ds9} \parallel r_{ds11}, \quad (20)$$

where r_{ds1} , r_{ds4} , r_{ds5} , r_{ds7} , r_{ds9} , and r_{ds11} are the output resistances of respective devices. The results of the presented small-signal analysis indicate that the first stage gain can be controlled by varying the transconductance of device M5, which is linearly dependent on the VGA control voltage (CTRL). However, the gain of the second stage defined by g_{mb9} , r_{ds9} , and r_{ds11} , is completely independent of CTRL.

The known location of the poles and zeros present in the proposed topology and their analytical definition is crucial for stability evaluation. The small-signal model of the circuit (**Figure 10**) has been used again for the pole-zero analysis. The overall small-signal model for both stages of the discussed VGA can be simplified to a single voltage-controlled current source (VCCS) with their associated output resistances R_{out1} and R_{out2} , respectively (dotted line and gray boxes). The respective small-signal current generation can be expressed $V_{in}G_{m1}$ and $V_{out1}G_{m2}$. Moreover, adopting the simplified model, the low-frequency gain can be re-written in more detail as follows:

$$A_v = \frac{A_1 A_2 \cdot [A_{M15}r_{ds13} + r_{ds13} + r_{ds15}]}{A_{M15}r_{ds13} + R_{out1} + r_{ds13} + r_{ds15}} \approx A_1 A_2, \quad (21)$$

where A_{M15} is a small-signal gain of transistor M15 while r_{ds13} and r_{ds15} are the output resistances of transistors M13 and M15, respectively. If we consider that $R_{out1} \ll A_{M15}r_{ds13} + r_{ds13} + r_{ds15}$, the low-frequency gain of the designed amplifier can be approximately expressed as $A_1 A_2$. Using this approximation, the error between simulated and calculated low-frequency gain will be about 3%.

The first pole defines the amplifier bandwidth (BW), and it is approximately given by Eq. (22).

$$p_1 \approx \frac{-1}{(C_L + C_c)R_{out2} + \frac{A_{M15}A_2 R_{out1} r_{ds13} C_c}{A_{M15}r_{ds13} + r_{ds15}}} \quad (22)$$

It was considered in the approximation that R_{out1} and r_{ds13} are much lower than $A_{M15}r_{ds13} + r_{ds15}$. Since, the VGA has the second stage with a fixed gain, by observation of Eq. (22), it can be concluded that BW might be influenced by resistance R_{out1} . Therefore, the design of the discussed VGA can be conducted in two different ways.

The resistance R_{out1} is dependent on coefficients A and B (Eq. (19)), thus the bandwidth of the VGA can be either influenced by the controlling voltage or not. The resulting R_{out1} is defined by parallel combination of both coefficients, therefore their values determine the frequency properties of R_{out1} . When the portion of A dominates ($A \ll B$), the control voltage will adjust G_{m1} and R_{out1} , which eventually allows for greater range of gain control. On the other hand, the bandwidth will be also influenced. The other option is when R_{out1} is determined by B ($A \gg B$). In this case, the gain can be controlled in narrower range, but the bandwidth will be independent of CTRL. Based on the presented design considerations, we have chosen to employ the second option, in order to obtain constant bandwidth across the control voltage range.

To achieve a stable operation of the proposed VGA topology, the so-called *pole splitting* compensation technique has been implemented. The second pole p_2 needs to be positioned at much higher frequency than the GBW. The analytical definition of p_2 to GBW ratio is expressed as follows:

$$\frac{p_2}{GBW} = \frac{1/p_1^2 \cdot [A_{M15}r_{ds13} + r_{ds15} + R_{out1}]}{A_1A_2R_{out2}r_{ds13}r_{ds15}C_LC_c \cdot [r_{ds15} + R_{out1}]} \quad (23)$$

It is obvious, that for satisfactory amount of phase margin (PM), the numerator of Eq. (23) has to be greater than the denominator. It is widely accepted that $PM = 60^\circ$ is sufficient for maintaining a stable operation of amplifier circuits, which will be met when the ratio $p_2/GBW \approx 2$. An important remark regarding PM is that it is negatively affected by gain A_1 , hence very high value of A_1 will result in lowered PM. On the other hand, if the VGA is stable even with high gain level A_1 , it will maintain stability for low A_1 , too [8].

3.4 Low-voltage BD comparator

In this section, we would like to describe the proposed topology of a voltage comparator operating with the power supply voltage (V_{DD}) of 0.4 V. Due to very limited voltage span, the comparator has to be able to process the input signals in rail-to-rail range. Another important feature regarding voltage comparators is the hysteresis. The proposed comparator topology contains four levels of hysteresis programmable by input digital code. Additional but very welcome feature especially in low-power circuits is enable function. Its whole purpose is to inhibit the circuit function and lower the internal current consumption into the leakage range. One can easily observe the main advantages of the discussed comparator topology. Unlike the traditional comparator circuit with three stacked MOS transistors, the proposed one, employing just two stacked devices, can obviously function with lower supply voltage levels. The second benefit lies in the rail-to-rail input voltage range achieved by only one differential structure, rather than parallel combination of two separate PMOS and NMOS amplifiers. Another important contribution, if compared to the traditional comparator, is based on the lack of the internal bias reference block. This feature simplifies and speeds up the design procedure, lowers the overall quiescent current consumption and enables setting the current flow through the circuit branches just by respective transistor sizing.

3.4.1 Description of low-voltage comparator

The analog core of the proposed circuit is depicted in **Figure 12** along with the devices' dimensions. Let us discuss the topology of the ultra-low-voltage rail-to-rail

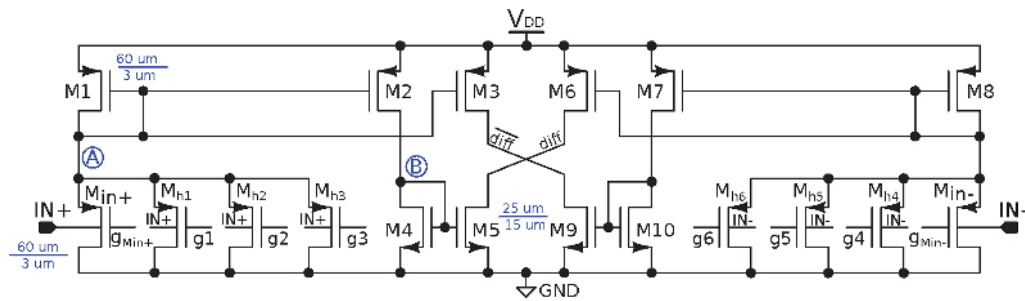


Figure 12.
 Analog core of ultra-low-voltage comparator.

voltage comparator. As one can observe, the input signal is processed by bulk-driven MOS transistors. This is an elegant way to solve the issues with the threshold voltage of respective devices. The most dreaded problem associated with rather exotic bulk-driven circuits is so-called *latch-up effect*, which causes catastrophic short between the power supply rails. However, with power supply voltage set to $V_{DD} = 0.4 \text{ V}$, such an event cannot occur, because the threshold voltage of PN junction even at $T = 150^\circ\text{C}$ does not decrease below the specified value.

The input PMOS devices M_{in+} and M_{in-} act as a current sources. The static current flowing through the input branches is being modulated by the input voltage according to Eq. (3). This voltage-to-current conversion occurs in highly linear manner thanks to almost ideally constant transconductance $g_{mb} = \frac{dI_D}{dV_{BS}}$ across whole input voltage range. The current from the input branches is afterward copied by means of unity current mirror system comprised by devices M1–M10. The differential voltage is created in nodes called *diff* and $\overline{\text{diff}}$ by current-to-voltage conversion. The differential signal is further processed by digital block, which is depicted in **Figure 13**.

The gate terminals of low-side devices employed in analog core are controlled by the digital part. The input devices can be cut-off when their gate terminals are pulled up—digital block issues logic one, when the circuit function is being inhibited. Otherwise, the gates are pulled down by logic zero, which sets their operation in to active, saturation, and region. The schematic diagram omits four

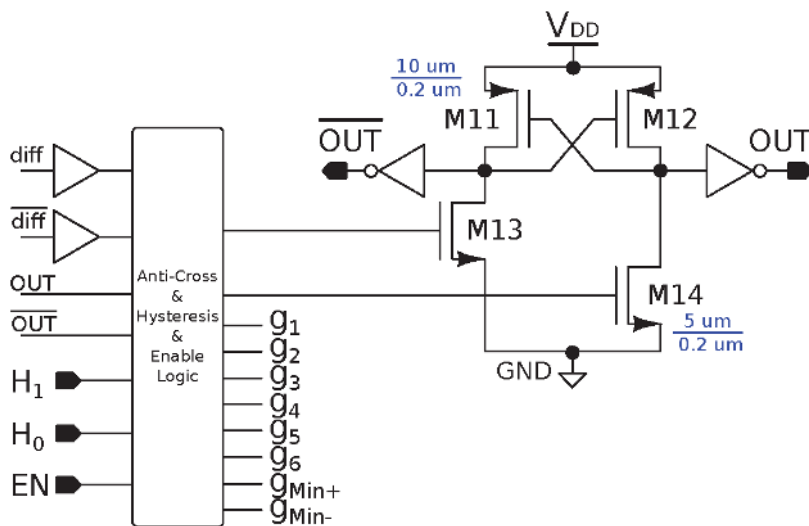


Figure 13.
 Digital control and output block of the ultra-low-voltage comparator.

pull-up and pull-down devices, which are responsible for ensuring a definite and known potential in the analog core nodes, when the circuit function is being disabled.

Transistors M_{h1} – M_{h6} are used to introduce hysteresis into the transfer characteristics without any external component required. The principle of operation is rather simple, yet very effective. In our case, we created four different levels of symmetrical hysteresis. The amount of hysteresis is programmable by 2-bit input code processed by the controlling digital block. Based on this information, the gate terminals of respective devices are pulled up or down and creates hysteresis of ± 0 , 10, 20, and 50 mV. Therefore, the static current flow in the input branches is disbalanced, which in effect, shifts the trip point of the comparator. The beauty of this method is in minimal area and current consumption overhead, since the amount of the hysteresis is determined by transistor size. Another important feature is the possibility of creating customized shape (e.g., non-symmetrical) and level of hysteresis.

The controlling block and output latch are depicted in **Figure 13**. The controlling block processes the input signals of enable and hysteresis functions and the feedback signal from the output latch and the differential voltage from the analog core. The combinatorial logic issues logic states for the gate terminals of transistors in the analog core accordingly. It is also responsible for protecting the output latch from simultaneous switching based on the feedback information. Such an event has been observed with highly rippled power supply voltage. The output signal from the latch is afterwards “buffered” by digital inverter(s) sized accordingly to the capacitance load and speed/slew-rate requirements.

3.4.2 Design considerations and analysis

Let us discuss the design considerations of the proposed comparator topology. Since the power supply voltage has already been set to $V_{DD} = 0.4$ V due to bulk-driven input stage, we need to determine the operational temperature, or in other words the temperature corners. The usual choice is set within the industrial standard -20°C and 85°C , which was also our case. Another important aspect is a selection of CMOS fabrication process node. Current standard (as of 2020) for analog/mixed-signal designs presets the choice into planar deep sub-micron technologies (e.g., 500, 350, 130, or 90 nm) thanks to their fair trade-off between the cost and the general properties of the process and available electronic components. Analog/mixed-signal designs in finer technology nodes usually face complications requiring advanced solutions and workarounds, which outweighs the advantages linked to smaller silicon circuit area or higher operational speed.

The final transistor sizes can be seen in **Figures 12** and **13**. From the designer’s point of view, the analog part has to be symmetrical, which decreases the overall effort required during the design period. One can observe, rather large MOS transistor dimensions. This choice has been done, in order to mitigate the process fluctuations associated with nanoscale CMOS processes. Furthermore, it also increases the level of inversion within the respective devices since higher the inversion coefficient, the lower current mismatch and process sensitivity.

The small-signal model of the proposed topology is shown in **Figure 14**. Thanks to the overall symmetry of the analog core, we will greatly benefit from analyzing only one half of the circuit. We have chosen the left-hand side, for our analysis. Furthermore, the devices from both topology sides are mutually interchangeable for the sake of small-signal analysis, if needed. The nodes marked “A” and “B” in the transistor-level schematic (**Figure 12**) are also depicted in the small-signal model. Another analysis simplification is, that the overall voltage amplification can be

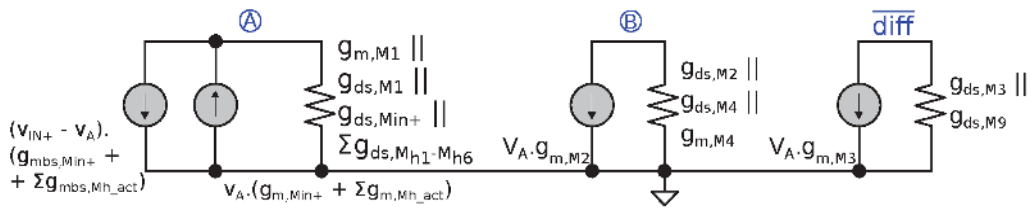


Figure 14.
 Small-signal model of the proposed ultra-low-voltage comparator.

expressed as a product of partial voltage amplifications (or as a sum of partial voltage gains) of respective stages. For even further simplification, we have also omitted the enable pull-up and pull-down devices, which do not affect the overall accuracy that much and can be therefore neglected.

The first stage is comprised of devices M_{in+} , M_{h1--6} and diode-connected MOS transistor M1. The input node is the actual comparator input terminal. The output node, in this case, is the node named “A”. As one can observe, the bulk-driven M_{in+} inherently contains a negative voltage feedback, which unfortunately decreases the voltage amplification below unity. This is depicted as two current sources working against each other in the small-signal model. The precise analytical expression of the first stage voltage amplification is defined by Eq. (24). It is apparent, that the overall amplification is dependent on the activated hysteresis devices.

$$A_{V_A} = \frac{g_{mbs_{Min+}} + \sum g_{mbs_{Mh_act}}}{g_{ds_{Min+}} + g_{m_{Min+}} + g_{mbs_{Min+}} + g_{ds_{M1}} + g_{m_{M1}} + \sum g_{ds_{Mh1-h6}} + \sum g_{m_{Mh_act}}} \quad (24)$$

The second amplification stage is consist of devices M2 and M4. The input port is the “A” node and the output port would be the node named “B.” The devices form a classic configuration of PMOS common-source amplifier with diode-connected transistor acting as a load. The small-signal model yields an Eq. (25), which defines the voltage amplification of the second stage.

$$A_{V_B} = \frac{g_{m_{M2}}}{g_{ds_{M2}} + g_{ds_{M4}} + g_{m_{M4}}} \quad (25)$$

The third and final stage of the model is comprised of devices M3 and M9. However, due to already explained reasons, we can swap the MOS transistor M9 with device M5, if desired. The topology of this stage can be described as a common-source amplifier with MOS transistor acting as load with fixed-bias. The small-signal model also reveals the fact, that the final stage is driven by the first stage only. Hence, the second stage does not contribute to the overall amplification, at all. The analytical voltage amplification provided by the final stage is defined by Eq. (26).

$$A_{V_{diff}} = \frac{g_{m_{M3}}}{g_{ds_{M3}} + g_{ds_{M9}}} \quad (26)$$

As we discussed earlier, the final voltage amplification is a product of partial amplification contributions of the respective stages. However, the final analytical formula is unnecessarily complex and can be significantly simplified, if the circuit designer follows some of the common sense rules. The most basic one is associated with the “reasonable” channel length and/or minimized channel length modulation along with saturation operation mode of the transistors employed in the analog

core. If this requirement is met, the sum of output conductance g_{ds} of respective devices in the denominator of Eq. (24) can be neglected, since it is several orders of magnitude lower than the sum of their transconductances g_m . Keeping in mind that the second stage does not contribute to the overall gain, we can re-write the resulting formula as follows:

$$A_V \approx \left(\frac{g_{mbs_{Min+}} + \sum g_{mbs_{Mh_{act}}}}{g_{m_{Min+}} + g_{mbs_{Min+}} + g_{m_{M1}} + \sum g_{m_{Mh_{act}}}} \right) \cdot \left(\frac{g_{m_{M3}}}{g_{ds_{M3}} + g_{ds_{M9}}} \right) \quad (27)$$

It is apparent that for the maximized voltage gain, one should increase the transconductance of M3 and minimize the output conductance of devices M3 and M9. Since the topology is symmetrical, the same applies for the counterparts of discussed transistors.

Another important design consideration is the minimum power supply voltage the circuit can reliably operate with. The presented topology contains only two stacked transistors that need to be saturated for correct functioning. Therefore, we can express the *theoretical* minimum power supply voltage at room temperature in as follows:

$$V_{DD_{min}} = 2 \cdot V_{DS_{sat}} \approx 2 \cdot \left(4 \cdot \frac{k \cdot T}{q} \right)_{T=300K} \approx 206.88 \text{ mV} \quad (28)$$

The expression is taken from the EKV MOS transistor model theory for deep weak inversion [4]. In real scenario, the saturation voltage dependence on the level of inversion is of square root trend. Furthermore, considering a non-ideal conditions, the more realistic expectation is about $V_{DD_{min}} = 230 \text{ mV}$ at room temperature.

3.5 Ultra-low-voltage BD charge pump

3.5.1 Description of the BD charge pump

CMOS realization of the conventional charge pump based on the cross-coupled voltage doubler is shown in **Figure 15**. This charge pump represents one of the highly efficient topologies suitable for on-chip implementation. Both types of MOS devices are employed in the cross-coupled charge pump. The proposed control approach mitigates the excessive voltage stress, which the thin gate oxide of the MOS transistor is exposed to. The voltage drop is comprised of the equivalent resistance of the switched capacitors and the voltage drop across the turned-on transistor [10].

The cross-coupled charge pump (**Figure 15**) is based on two inverters connected in cross-couple fashion. The discussed topology, exhibits the same level of minimal input switching voltage $V_{\phi_{min}}$ as the traditional CMOS inverter the sum of threshold voltages of the respective MOS transistors employed. Hence, a specific modifications to the circuit topology are required, in order to enable the implementation in ultra-low-voltage applications.

One of the possible alternatives is to employ an inverter with resistor acting as a load, which would create the so-called pseudo-inverter. However, the solution is unacceptable in low-power systems, since it notably increases the internal current consumption of the charge pump. Another possibility is to tie the bulk terminal of the MOS transistors to a fixed potential and lower their threshold voltage (**Figure 16(b)**). Unfortunately, this approach substantially increases the sub-threshold leakage of the MOS transistors and their bulk current, as well. Hence, it

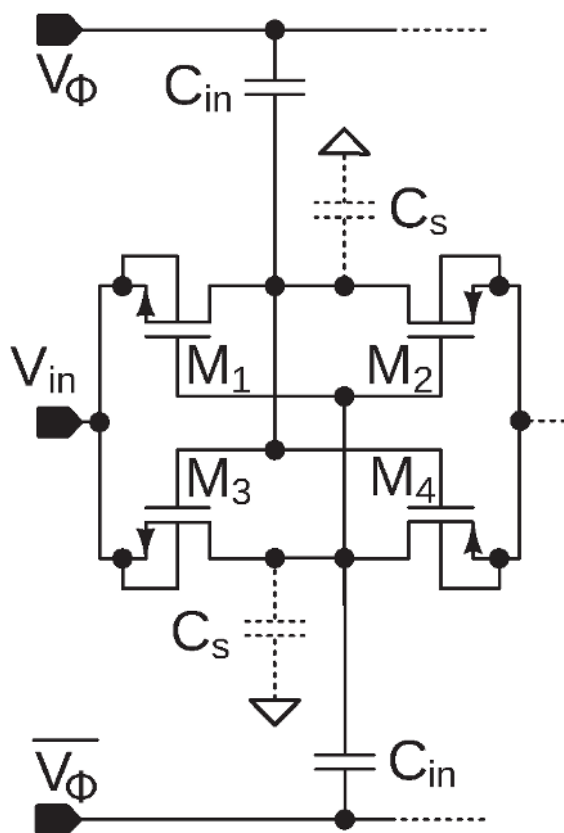


Figure 15.
 Conventional cross-coupled CP (one stage).

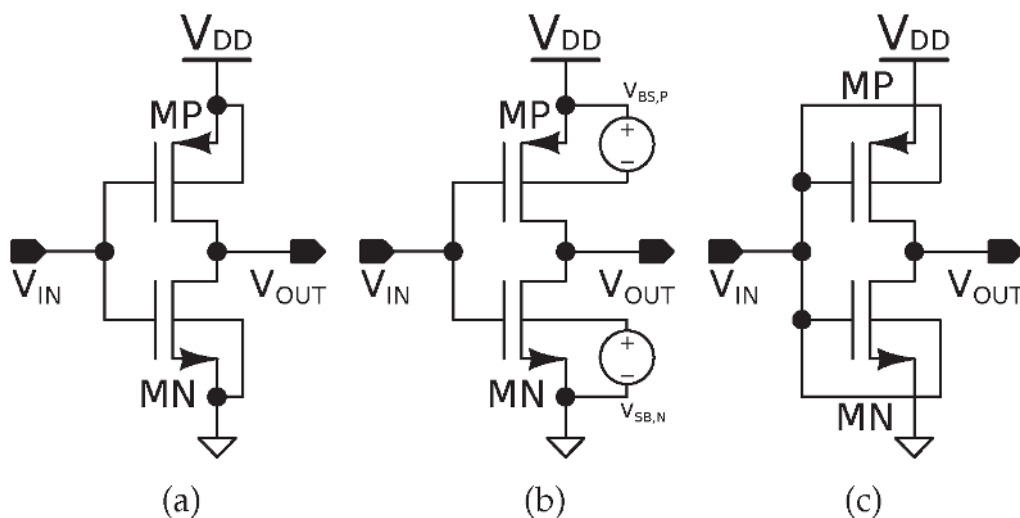


Figure 16.
 Different topology inverters in CMOS technology. (a) CMOS inverter, (b) CMOS inverter: reduced VTH (c) CMOS inverter: dynamic VTH.

suffers from the same drawback as the solution mentioned previously. The most effective approach, as it seems, is the so-called dynamic threshold voltage control. The basic idea is depicted in **Figure 16(c)**. As one can observe, the bulk terminals are connected to the input signal. This way, the cut-off transistor exhibits nominal threshold voltage and the turned-on transistor exhibits lowered threshold voltage

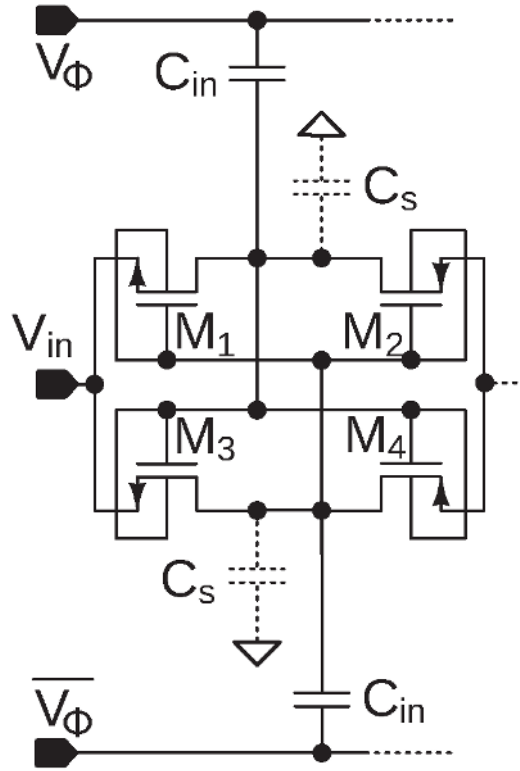


Figure 17.
Bulk-driven cross-coupled CP (one stage).

level, which improves its drain current and switching speed. The trade-off of this method is increased leakage current of one transistor only.

Dynamic threshold inverter topology (**Figure 16(c)**) can be considered as an appropriate building cell for ultra-low-power and low-voltage charge pump designs. A very important design consideration for such a system is inevitability of twin-well CMOS fabrication process, since both PMOS and NMOS devices have to be isolated from the common substrate by their own wells. Another consideration is restricted power supply voltage. Its level must not exceed 0.6 V (at room temperature). Otherwise, parasitic NPN and PNP bipolar transistors will turn on, which with the high probability may cause triggering of latch-up effect. These limitations have to be taken into account, if designing the charge pump with dynamic V_{TH} MOS inverters.

The BD charge pump based on the cross-coupled topology is shown in **Figure 17**. The charge pump employing dynamic threshold CMOS inverter is able to process very low levels of input voltages. This also represents the main advantage of the proposed topology [10]. However, the drawback lies in the limited voltage range the charge pump can work with, because of the increased risk of latch-up triggering. Hence, the main application area of such charge pump topology is constrained to low-voltage and low-power systems.

3.5.2 Design procedure of BD charge pump

Theoretical value of the output voltage can be expressed as follows:

$$V_{out} = V_{in} + N \left(V_{\phi} \cdot \frac{C_{in}}{C_{tot}} - I_L \left(R_{on} + \frac{R_{eq}}{2} \right) \right), \quad (29)$$

where N is a number of stages used, V_{in} is the input voltage, V_{out} is the output voltage, V_{ϕ} is the switching voltage, C_{in} is the switching capacitance, C_{tot} is sum of switching capacitance and parasitic capacitance $C_{tot} = C_{in} + C_s$, I_L is sum of output and leakage currents $I_L = I_{out} + I_{leakage}$, R_{on} is switch-on resistance of NMOS and PMOS transistor, and R_{eq} is equivalent resistance of switching capacitor.

Due to limited voltage headroom, the sub-threshold operation is usually chosen for low-voltage/low-power charge pump designs. Although, when the input voltage is lesser than threshold voltage of MOS transistors, the overall efficiency will be degraded, since the switching properties of the devices are drastically reduced. The dependence of MOS transistor turn-on resistance R_{ON} on the overdrive voltage (V_{EFF} or $V_{GS} - V_{TH}$) is defined in Eq. (30).

$$R_{ON} \sim \frac{1}{e^{V_{GS}-V_{TH}}} \quad (30)$$

It can be observed that effective voltage V_{EFF} in relation to R_{ON} acts as argument of exponential function located in denominator, which implicates the substantial sensitivity to change of this quantity. In order to overcome this issue, many techniques such as dynamic control, feed-forward biasing of the bulk electrode, multi-stage topology, implementation of charge transfer switches (CTS) parallel with pass gate switches (PGS) or backward control of the previous stage by body electrode voltage can be included in the low-voltage CPs design [11–14].

3.6 Evaluation of the proposed LV circuits

In order to fully verify the design concepts discussed in this chapter, the proposed circuit topologies have been designed in general purpose twin-well 130 nm CMOS technology. Both types of fabricated long-channel devices exhibit the standard threshold voltage around $V_{TH} = 260$ mV at room temperature. **Figure 18** depicts the micrograph of the fabricated prototype chip along with the physical layout design. For better clarity, we omitted some of the top metal layers. The blue rectangles pin-point the location of the proposed circuits on chip. The chip also contains a stand-alone test transistor in order to verify the devices' compact simulation model accuracy and fabrication process fluctuations as well.

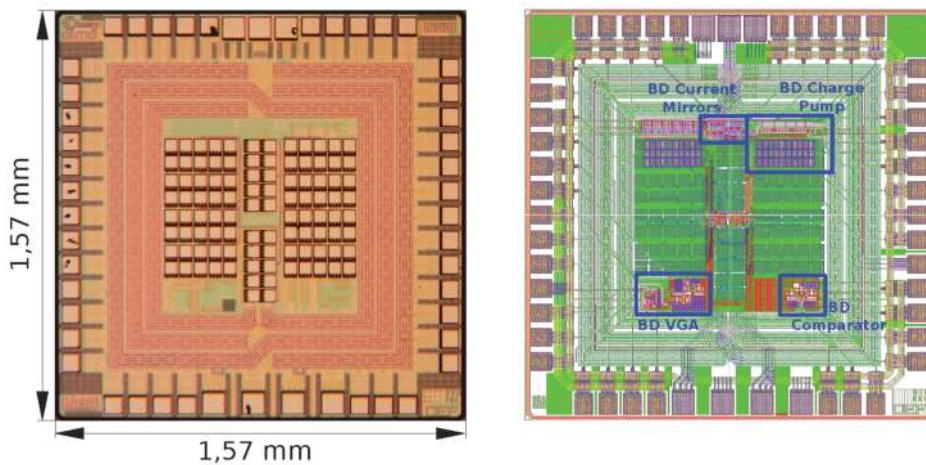


Figure 18.
 Micrograph and physical design of the prototype chip.

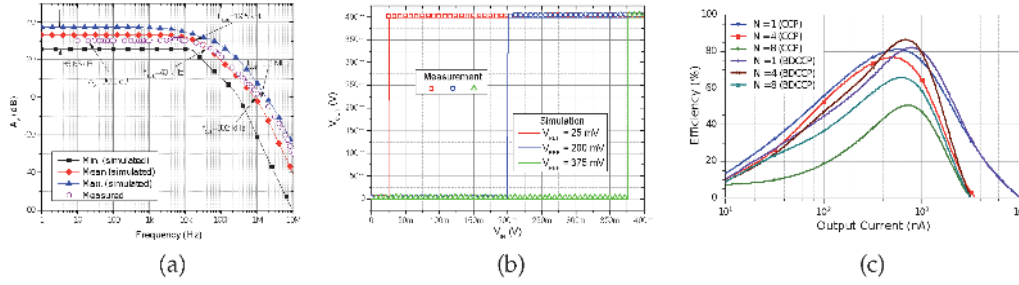


Figure 19. Measured and simulated parameters of the proposed circuit topologies on the prototype chip. (a) VGA frequency response, (b) Comparator transfer characteristics, (c) Charge-Pump efficiency.

The selected parameters of the proposed VGA, voltage comparator, and charge pump are depicted in **Figure 19**. The graphs contain the measured and simulated results for direct comparison and evaluation.

The comparison of simulated and measured data of frequency response of the proposed VGA is depicted in **Figure 19(a)**. We used the Monte-Carlo analysis results to obtain the borders of the expected gain range. As one can observe, the measured frequency response remains between the borders specified by the simulation and deviates only slightly from the Monte-Carlo mean curve. The measurement and simulation conditions were identical, the load capacitance of 10 pF, the control voltage $V_{CTRL} = 0.1$ V, ambient room temperature, and power supply voltage of $V_{DD} = 0.6$ V were used. The obtained measured results at these operating conditions were the following. The voltage gain of $a_V = 30$ dB, gain-bandwidth of $GBW = 1.2$ MHz and bandwidth of $f_{-3dB} = 40$ kHz were observed. The worst-case discrepancy of the measured low-frequency gain compared to the mean Monte-Carlo curve is approximately ± 5.85 dB.

The transfer characteristics of the proposed rail-to-rail comparator are depicted in **Figure 19(b)**. The simulated results correlate very well with measured curves for all input voltage conditions. In our experiments, the comparator exhibited correct function for all four levels of hysteresis and the rail-to-rail operation has been confirmed by setting the reference voltage only 3 mV from the power supply range. This test can be considered quite strict, since it would also reveal issues with the input offset voltage. Monte-Carlo simulations performed on 3000 samples in corner and ambient temperatures resulted in the mean value of input offset $V_{offset} = 592$ μ V with standard deviation of $\sigma = 1.91$ mV [15]. Furthermore, the power consumption at $V_{DD} = 0.4$ V has been measured in the upper half of nW range including the ESD structures leakage, PCB, and oscilloscope probe parasitics. However, we have also observed correct operation with $V_{DD} = 0.25$ V, which indeed astonishing result.

Figure 19(c) shows dependence of the efficiency on the output current. This is the example where the comparison of different charge pumps based on GD and BD cross-coupled inverter were compared. The best efficiency for the given parameters can be observed for the output current of 1μ A, where the BD cross-coupled charge pump achieves the efficiency of 80% in four-stage architecture ($N = 4$) in given CMOS technology.

4. Conclusions

Considering the current onset of ultra-low-voltage and ultra-low-power operation requirements for today's CMOS analog/mixed-signal ICs and their fabrication,

a promising alternative to standard design approach and circuit topologies are discussed in this chapter. We presented low-voltage and low-power design techniques, which are focused on driving the MOS transistor through its bulk terminal, as well as setting the operating point of employed MOS transistors within the sub-threshold (weak inversion) or moderate inversion region. The combination of described design techniques provides the significant power consumption minimization (nW feasible), while maintaining acceptable circuit performance and parameters. The motivation for research and development in given scientific field is enormous and new published results are expected to grow in upcoming years.

The proposed circuit topologies of basic analog IC building blocks have been designed and fabricated in 130 nm twin-well general purpose CMOS technology with industrial operating temperature range taken into account. The experimental measurements performed on the prototype chip samples confirm a successful implementation and correct circuit operation with ultra-low-power supply voltage. Hence, we can state that the feasibility of presented IC design approach has been successfully demonstrated and the circuit topologies have been silicon-proven, which opens the door for even deeper gradual investigation and understanding of given scientific topic with promising future impact on the IC industry as well.

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