

# The Progress and Challenges of Applying High-k/Metal-Gated Devices to Advanced CMOS Technologies

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## 1. Introduction

### 1.1 Motivation for implementing high dielectric constant gate dielectric for advanced CMOS scaling

Semiconductor devices need to have good performance, with a low cost and low power dissipation. For decades, research and development of semiconductor processing technology and device integration have focused on enhancing performance and reducing costs using SiO<sub>2</sub> as the gate dielectric and doped polysilicon as the gate electrode. The most effective way to enhance performance and reduce costs is to scale the device gate length and gate oxide. Scaling the gate length results in fabricating more devices per wafer (i.e., increase the device density) and thus reduce the cost per chip, while scaling the gate oxide enhances the drive current and reduces the short channel effects due to gate length scaling. However, as the gate oxide becomes thinner, the power to operate transistors increases because of greater gate oxide leakage current. To resolve this high gate oxide leakage problem, the mechanism of the carriers tunneling through the gate dielectric must be better understood. In an ideal metal-insulator-semiconductor (MIS) device, the current conduction in the insulator should be zero. In a real MIS device, however, current can flow through the insulating film by various conduction mechanisms. The two primary conduction mechanisms for electron tunneling through high quality gate dielectric are discussed below.

#### 1.1.1 Direct tunneling

In a metal-insulator-semiconductor (MIS) stack, when the oxide voltage ( $V_{ox}$ ) is smaller than the metal-insulator barrier height, the electron tunnels directly from the metal electrode into other semiconductor electrode through the insulator. This is known as the direct tunneling process. The equation for direct tunneling current density (current normalized by device area) is proportional to

$$J_{DT} = A \exp(-m^{1/2} V_b^{1/2} T_{ox}) = B \exp(-m^{1/2} V_b^{1/2} K) \quad (1)$$

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where  $m$  is the effective mass of the electron,  $V_b$  is the barrier height,  $T_{ox}$  is the physical thickness of the gate oxide  $\text{SiO}_2$ ,  $K$  is the dielectric constant of the insulator, and  $A$  and  $B$  are pre-exponential factors. From this equation, one can observe that the  $T_{ox}$  or  $K$  is the dominating factor in controlling the direct tunnel current density. The tunneling current density increases dramatically as the  $\text{SiO}_2$  becomes thinner. In general, the gate leakage increases 100 times for every 0.5 nm that the  $\text{SiO}_2$  is thinned. The gate leakage density is as high as the  $10 \text{ E}^4 \text{ Amp/cm}^2$  range for  $\text{SiO}_2$  as thin as 1.1 nm. The high gate leakage increases standby power consumption according to the following equation:

$$P_{\text{STANDBY}} = (I_{\text{subth}} + I_{\text{GIDL}} + I_g) \cdot V_{\text{dd}} \quad (2)$$

Where:  $I_{\text{subth}}$ : subthreshold leakage current  
 $I_{\text{GIDL}}$ : gate-induced drain leakage current  
 $I_g$ : gate leakage  
 $V_{\text{dd}}$ : supply voltage

On the other hand, Eq. [1] shows that increasing the dielectric constant of an insulator dramatically reduces the direct tunneling current. This is because the gate oxide physical thickness ( $T_{ox}$ ) and the dielectric constant  $K$  of an insulator are correlated by the equivalent oxide thickness (EOT) defined as

$$\text{EOT} = (K_{\text{SiO}_2}/K_{\text{insulator}})T_{\text{insulator}} \quad (3)$$

where  $K_{\text{SiO}_2}$  and  $K_{\text{insulator}}$  are the dielectric constant of  $\text{SiO}_2$  and the insulator, respectively, and  $T_{\text{insulator}}$  is the physical thickness of the insulator. Based on this definition, an insulator material with a five times greater dielectric constant than  $\text{SiO}_2$  would require a five times greater physical thickness than  $\text{SiO}_2$  to keep the same EOT as  $\text{SiO}_2$ . Therefore the tunneling current for a device using this insulator would be orders of magnitude lower than that using  $\text{SiO}_2$  because the tunneling leakage current decays exponentially as the insulator becomes thicker.

### 1.1.2 Fowler nordheim tunneling

When the oxide voltage ( $V_{ox}$ ) is greater than the metal/insulator barrier height, the electron tunnels from the metal electrode into the insulator conduction band first and then travels toward the other semiconductor electrode. This is known as the Fowler-Nordheim (FN) tunneling process. The equation for FN tunneling current density is proportional to

$$J_{\text{FN}} = C \exp(-m^{1/2} V_b^{3/2} T_{ox}) = D \exp(-m^{1/2} V_b^{3/2} K) \quad (4)$$

where  $C$  and  $D$  are pre-exponential factors. From this equation, one can observe that the barrier height is the dominating factor in controlling the FN tunnel current density.

Table 1 compares the exponent (the product of  $m$ ,  $V_b$ , and  $K$ ) shown in the equations of direct tunneling (low field) and FN tunneling (high field) for insulator materials with different  $V_b$  and  $K$  values. The results show the following:

1. Although oxynitride processed by incorporating nitrogen into  $\text{SiO}_2$  was developed to increase the dielectric constant, the reduction of leakage current density is not enough to be used for highly scaled devices such as for the 45 nm technology node. Even for pure nitride ( $\text{Si}_3\text{O}_4$ ) shown in the table, the exponent shown in the direct tunneling

equation is only about two times greater than that for SiO<sub>2</sub> while the exponent shown in the FN tunneling equation is similar to that of SiO<sub>2</sub>.

- On the other hand, it is clear that an insulator with a *K* value of 25 reduces the exponent significantly in the direct tunneling Eq. [1] and more than two times in the FN tunneling Eq. [2].

Material	V <sub>b</sub> (Volts)	K	Low Field	High Field
SiO <sub>2</sub>	3.0	3.9	-6.75	-20.3
Si <sub>3</sub> N <sub>4</sub>	2.0	7.8	-11.0	-22.1
Ta <sub>2</sub> O <sub>6</sub> , HfO <sub>2</sub> , ZrO <sub>2</sub>	1.5	25	-30.6	-45.9

Table 1.

## 1.2 Motivation for implementing metal gates for advanced CMOS scaling

### 1.2.1 SiO<sub>2</sub>/Polysilicon stack

Figure 1 shows a schematic of a MOSFET in which the gate oxide is SiO<sub>2</sub> and the gate electrode is doped polysilicon. Figure 2 shows the equivalent circuit of an MOS capacitor. The total MOS capacitance C<sub>g</sub> can be expressed as

$$C_g^{-1} = C_{ox}^{-1} + C_s^{-1} + C_p^{-1} \tag{5}$$

where C<sub>ox</sub> is the oxide capacitance, C<sub>s</sub> is the silicon capacitance, and C<sub>p</sub> is the polysilicon gate electrode depletion capacitance.

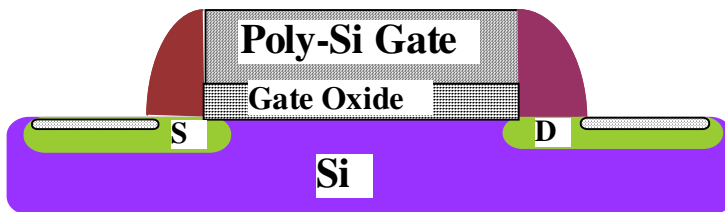


Fig. 1.

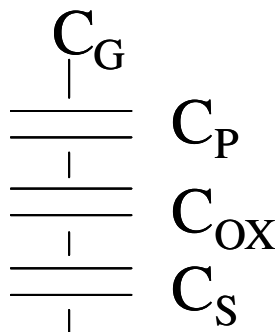


Fig. 2.

When the MOSFET is operated in inversion mode, the doped polysilicon gate energy band bending and charge distribution form a thin space-charge region. This results in a finite, bias-dependant value of  $C_p$  and causes polysilicon depletion. The  $C_p$  will reduce the value of the  $C_{ox}$  for an applied gate voltage ( $V_g$ ), which, in term, will degrade the MOSFET performance. Although the  $C_p$  can be reduced by increasing the dopant concentration in the polysilicon gate electrode, a high dopant concentration would result in dopant penetrating the gate oxide and induce a threshold voltage ( $V_t$ ) instability problem. On the other hand, using a metal gate as the gate electrode could eliminate the polysilicon gate depletion problem without  $V_t$  instability concern because there is no need for dopant to be incorporated into the gate electrode. Another advantage of a metal gate is that the resistance of the metal gate electrode is less than a polysilicon gate.

### 1.2.2 High dielectric constant insulator compatibility with gate electrode

The compatibility of polysilicon gate electrodes with high dielectric constant (high-k) insulators raises some concern. Most metal oxides with a high dielectric constant used as a gate insulator react with polysilicon and degrade the gate dielectric. Furthermore, this interaction makes it difficult to control the MOSFET threshold voltage. On the other hand, a metal gate is more compatible with high-k metal oxides.

## 2. Materials screening of high dielectric constant insulators and metal gates

### 2.1 High-k gate dielectric screening

#### 2.1.1 Issues of high-k gate dielectric

Some fundamental issues with implementing a high-k gate dielectric in MOSFETs are as follows:

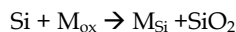
- Thermodynamic stability of high-k on silicon
  - Trade-off between the dielectric constant (K) and band gap ( $E_g$ )
  - Film microstructure: crystalline vs. amorphous
  - $O_2$  and dopant diffusion through the grain boundary
  - Impact of the amorphous interfacial layer (IL) on the overall dielectric constant of the film, EOT scalability, interfacial roughness, and MOSFET mobility
  - Possible mobility degradation and high fixed charge caused by a high-k insulator
  - Compatibility with the gate electrode
- a. Thermodynamic stability of high-k on silicon

An analysis of the Gibbs free energies governing the following chemical reactions for metal-Si-oxygen ternary systems is important in predicting stability.

To avoid instability with Si to form  $SiO_2$ ,



To avoid silicide formation,



- b. Trade-off between the Dielectric Constant (K) and Band Gap ( $E_g$ )
- From the direct tunneling Eq. [1], it is desirable to find an insulator with a high dielectric constant and high barrier to ensure low gate leakage current density. Since the barrier height values for most high-k metal oxides are not reported, the closest and most readily available indicator for the band offset is the band gap values. Figure 3 shows the plot of band gap versus dielectric constant for various metal oxides.

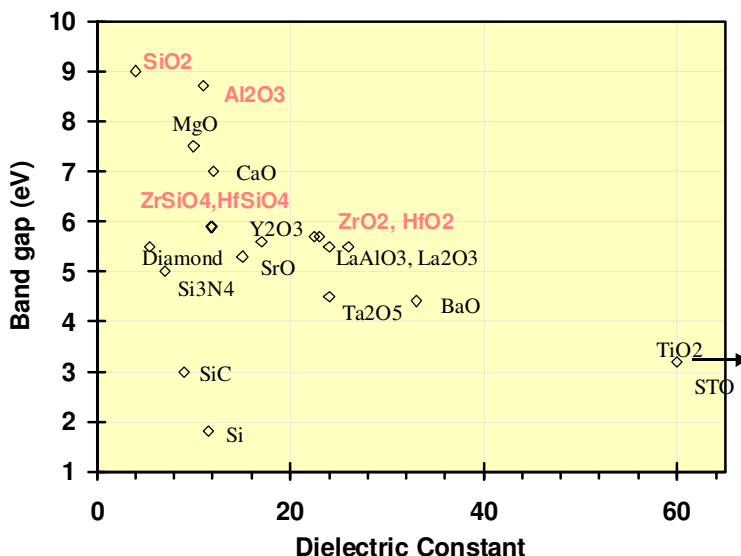


Fig. 3. The trade-off between dielectric constant and band gap limits the choice of metal oxides.

c. Film Microstructure: Crystalline versus Amorphous

For polycrystalline metal oxide, the triple point may generate defects/voids, which will cause a device yield issue. In addition, oxygen, dopant, and impurities diffuse swiftly in the polycrystalline structure primarily through the grain boundary and degrade the electrical properties of the gate stack. Another potential concern is controlling the grain size among small devices and wafers. Amorphous metal oxides can reduce O<sub>2</sub> and dopant diffusion and lower defectivity; however, they usually have a lower dielectric constant than those metal oxides with a polycrystalline structure.

d. Oxygen Diffusion through the Grain Boundary of Metal Oxide

There is a distinct processing difference between the metal oxides and conventional thermal oxide SiO<sub>2</sub>. Metal oxides are deposited on the silicon substrate instead of thermally grown like SiO<sub>2</sub>. The intrinsic quality of the deposited film is inferior to thermally grown film. A post-deposition anneal under dilute oxygen ambient is necessary for high performance devices. Most metal oxides with a high dielectric constant, however, form a crystalline structure after a relatively high temperature anneal. Therefore the oxygen contained in the ambient of the post-metal oxide deposition anneal diffuses through the grain boundaries of the metal oxides and reacts with silicon substrate, which forms a SiO<sub>2</sub> interfacial layer (IL).

e. Impact of the Amorphous Interfacial Layer (IL) on the Overall Dielectric Constant of the Insulator, EOT Scalability, Interfacial Roughness, and MOSFET Mobility

The SiO<sub>2</sub>-like interfacial layer reduces the overall dielectric constant of the bi-layer gate dielectric (high-k on top of a SiO<sub>2</sub> IL). The IL is about 1 nm thick, which would make scaling the EOT to less than 1 nm difficult. The interface between the IL and silicon substrate is rougher than the interface between conventional thermally grown SiO<sub>2</sub> and

silicon, which may degrade channel carrier mobility and generate interface state defects. Figure 4 shows a transmission electron microscopy (TEM) image of the metal oxide MOS structure and the key concerns about the gate stack.

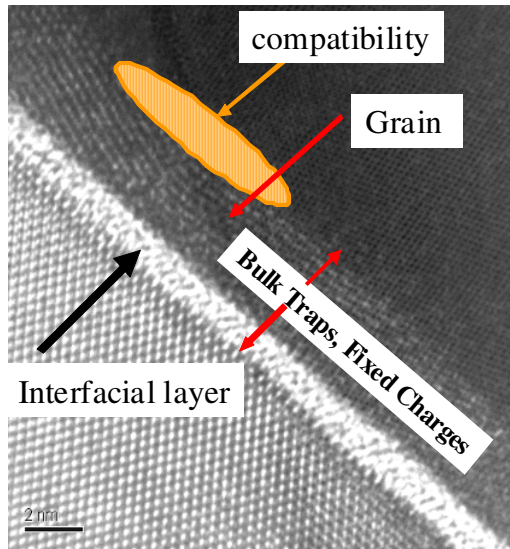


Fig. 4.

- f. Possible Mobility Degradation and High Fixed Charge Caused by the High-k Insulator  
Soft phonons in the metal oxide bonding structure contribute to the high dielectric constant property of metal oxides. Soft phonons are generated by high atomic number atoms resonating in their bonding structures. These phonons make a lattice contribution to the overall polarizability and therefore the high dielectric constant. There is a concern that the mobility of the channel carriers may be degraded by interactions with these soft phonons.

### 2.1.2 High-k Gate Dielectric Candidates

#### a. Metal Oxide

After eliminating the metal oxides that are thermodynamically reactive with silicon substrates or that have a relatively low dielectric constant or small band gap, the remaining candidates fall under group IVB, IIIA, and IIIB of the periodic table.

#### i. Metal Oxides Used for Memory Capacitors [1, 2, 3, 4]

Candidates such as  $\text{TiO}_2$  and  $\text{Ta}_2\text{O}_5$  have the advantage of having a relatively high dielectric constant and a history of processing in the industry. However, the following concerns make them unattractive for logic devices:

- Small band gap
- Instability with silicon substrates
- High density of oxygen vacancies
- Require an oxygen anneal to improve film quality, which results in oxidation of bottom leading to an undesirable increase in EOT

- Unstable microstructure
- ii. Group IIIA and IIIB Metal Oxides:  $\text{Al}_2\text{O}_3$  and  $\text{La}_2\text{O}_3$  [5, 6, 7]  
Both  $\text{Al}_2\text{O}_3$  and  $\text{La}_2\text{O}_3$  are thermodynamically stable with silicon substrates. In addition,  $\text{Al}_2\text{O}_3$  is amorphous at  $1000^\circ\text{C}$  and has a relatively high band gap (8.7 eV  $\sim$   $\text{SiO}_2$ 's value). However, it has a relatively low dielectric constant; high oxygen, B, and P diffusion; and easily absorbs  $\text{H}_2\text{O}$ .  $\text{La}_2\text{O}_3$  has a relatively high dielectric constant ( $K \sim 27$ ), but the band gap is small (4.3 eV) and it very easily absorbs moisture from the ambient.
- iii. Group IVB Metal Oxides:  $\text{HfO}_2$  and  $\text{ZrO}_2$  [8-18]  
These metal oxides have reasonably high dielectric constants and band gaps (see Figure 3). Both  $\text{ZrO}_2$  and  $\text{HfO}_2$  devices have demonstrated a many orders of magnitude reduction in gate leakage with an EOT around 1.0 nm and well-behaved transistors. However, they have high  $\text{O}_2$  and dopant diffusivity due to their crystalline microstructure.  $\text{ZrO}_2$  has a relatively stronger interaction with polysilicon gates than  $\text{HfO}_2$ . Figure 6 shows the interfacial layer thickness beneath  $\text{ZrO}_2$  increases as the post-deposition anneal temperature increases from 550 to  $650^\circ\text{C}$ .

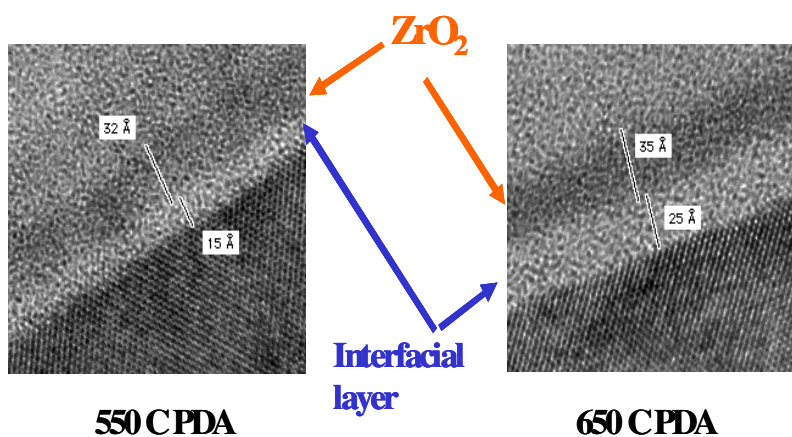


Fig. 6. [13]

Figure 7 shows the x-ray photoelectron spectroscopy (XPS) spectra of the interface between  $\text{ZrO}_2$  and the polysilicon gate. The polysilicon gate was deposited in situ on  $\text{ZrO}_2$ . XPS reveals that  $\text{ZrO}_2$  decomposes into a Zr metal compound when the gate stack is annealed in nitrogen at  $950^\circ\text{C}$  under ultra-high vacuum leading to a high gate leakage current. It also shows the formation of interfacial  $\text{SiO}_2$  between  $\text{ZrO}_2$  and the polysilicon gate during polysilicon deposition. These results suggest a strong interaction between  $\text{ZrO}_2$  and  $\text{SiH}_4$  during polysilicon deposition at 550 to  $620^\circ\text{C}$ .

On the other hand,  $\text{HfO}_2$  metal oxide is thermodynamically more stable with silicon than  $\text{ZrO}_2$ . Figure 8 shows the XPS spectra of the interface between  $\text{HfO}_2$  and the polysilicon gate. Unlike the  $\text{ZrO}_2$  film, the  $\text{HfO}_2$  film remains stable after polysilicon deposition and a post-anneal in nitrogen up to  $950^\circ\text{C}$ .

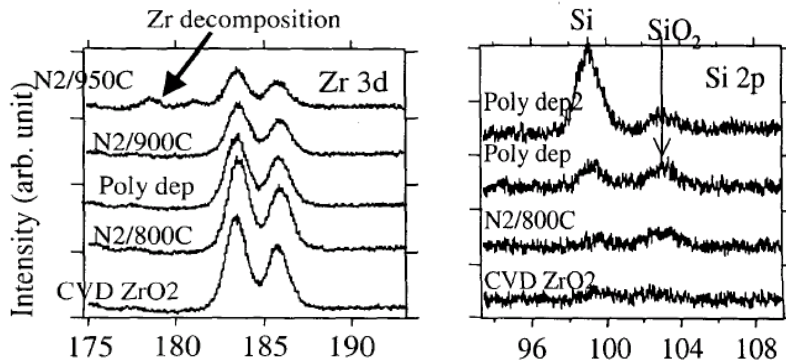


Fig. 7. [14]

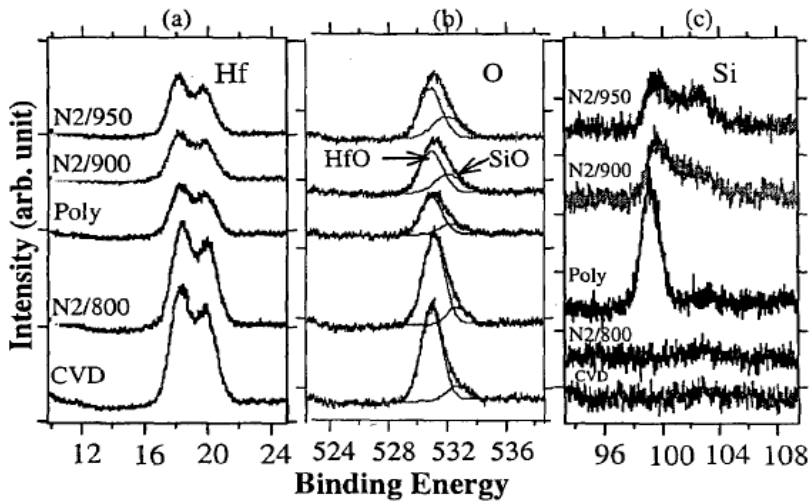


Fig. 8. [9]

b. Metal Silicates (M-Si-O) [19-22]

Adding silicon to metal oxide can maintain the amorphous phase up to a medium temperature such as 800°C depending on the silicon concentration. These metal silicates are thermodynamically stable with the silicon substrate. Figure 9 shows the TEM cross-sections of a gate stack composed of  $ZrSi_xO_y$  silicate deposited on a silicon substrate with an aluminum metal electrode. No interfacial layer forms between the zirconium silicate and the silicon substrate after annealing at 800°C for 30 minutes in nitrogen ambient. The interface is atomically sharp, and the film remains amorphous after the anneal. However, there is a possible phase separation with a high temperature anneal and the dielectric constants are lower than metal oxide candidates such as  $ZrO_2$  and  $HfO_2$ .



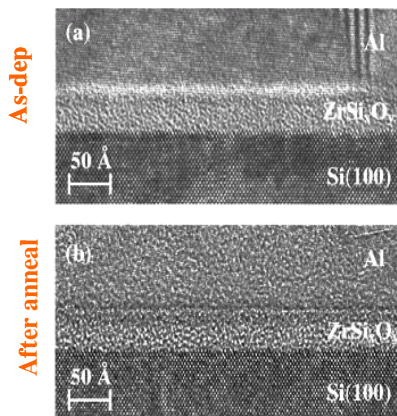


Fig. 9. [21, 22]

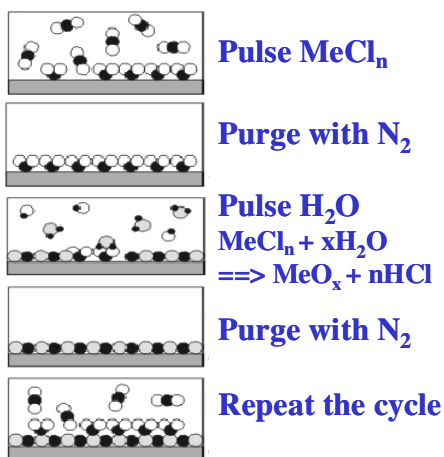


Fig. 10.

### 2.1.3 High-k dielectric deposition techniques

An important factor in determining the final choice of high-k dielectric is the deposition process, which must be compatible with current CMOS processing, cost, and throughput. In general, there are four major deposition techniques:

- Metal organic chemical vapor deposition (MOCVD) is commonly used, but the C, H, and OH impurities contained in the film are a major concern.
- Physical vapor deposition (PVD) is good for evaluating new materials. However, the purity of the target and plasma-induced damage are common concerns.
- Molecular beam epitaxy (MBE) is good for interfacial control, but the throughput is rather low.
- Atomic layer deposition (ALD) has high uniformity control and good conformality. However, throughput is low and the process is sensitive to surface preparation.

Potential contamination with Cl, C, H, and OH impurities is also a concern. Figure 10 shows a typical ALD process to fabricate metal oxide [23, 24]. In summary, same high-k materials fabricated by different deposition tools, processes, and precursors result in different properties. The final choice of the deposition technique needs to balance cost, throughput, tool reliability, film properties, and device performance and reliability.

#### 2.1.4 High-k gate dielectric device integration issues [17]

##### a. Device Size Dependence of Gate Current Density

Figure 11 shows that the gate current density of the  $ZrO_2$ /polysilicon gate stack has a strong dependence on device size. At 2 V, the leakage current density for the 14  $\mu m$  NMOS (PMOS) device is 9X (7X) that of a 1.4  $\mu m$  device. Figure 12 shows the TEM cross-section of the PMOS capacitor with a longer gate length. It is clear that some reactions have occurred at the polysilicon/ $ZrO_2$  interface. The TEM cross-section (Figure 13) shows a nodule extending above and below the polysilicon/ $ZrO_2$  interface. The penetration into  $ZrO_2$  creates a conduction path that results in a high gate leakage current. The longer gate length results in a higher probability that conduction paths will be formed.

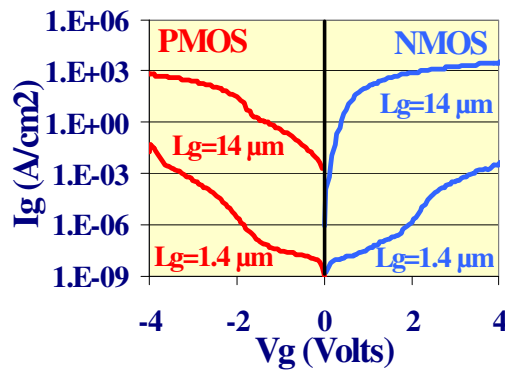


Fig. 11.

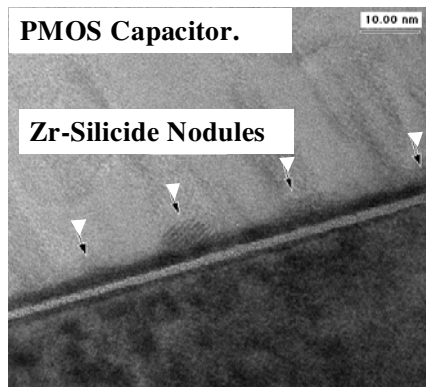


Fig. 12.

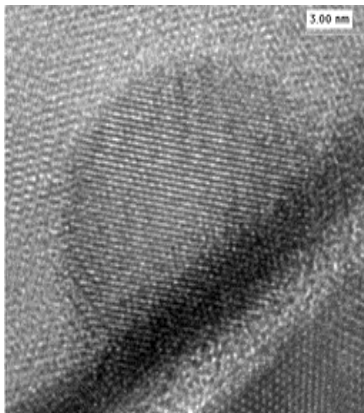


Fig. 13.

b. Lateral Oxidation Model [17]

Figure 14 shows that no nodule is observed at the edge of the devices. A detailed XTEM analysis found the first nodules located  $\sim 2\text{--}3\ \mu\text{m}$  from the edge of the polysilicon gate. This observation suggests that devices with  $4\text{--}6\ \mu\text{m}$  or smaller gate lengths are nodule-free. It is proposed that active oxygen diffuses through the metal oxide and grows an oxide ( $\text{SiO}_2$ ) at the polysilicon interface (Figure 15). The oxide prevents nodule formation during a high temperature anneal such as a source/drain anneal. Oxidation at the center of large devices is insufficient to prevent the formation of nodules, which cause high leakage current.



Fig. 14.

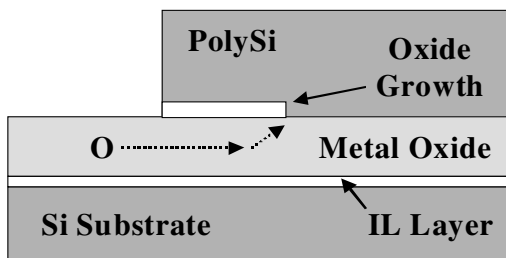


Fig. 15.

### 2.1.5 High-k dielectric summary

Select high-k metal oxides with thin EOTs have demonstrated an orders of magnitude lower gate leakage than SiO<sub>2</sub>. However, it is still a challenge to achieve an EOT thinner than 1.0 nm after transistor fabrication. Degradation in device mobility is observed when using a high-k dielectric. This is more problematic for low EOT applications. Since compatibility with polysilicon gate electrodes is a major concern for some potential metal oxides and metal gate has several advantages, a high-k/metal gate stack is the choice for advanced devices.

## 2.2 Metal gate electrode materials screening

### 2.2.1 Materials constraints

A key issue for metal gate materials research is controlling the work function of metal gate electrodes after CMOS processing. There are two choices of metal gate implementation. The first type is a single metal electrode with a work function near the mid-gap (~ 4.6 eV) using additional processing or incorporating additional materials to control the work function of CMOS devices. The second type is a dual metal gate electrode with one metal having a work function (4.1 eV) near the conduction band of the silicon substrate (E<sub>C</sub>) for NMOS and the other one having work function (~5.2 eV) near the valence band of the silicon substrate (E<sub>V</sub>) for PMOS (Figure 16). The metal electrode materials should have thermal, chemical, and mechanical stability with the high-k gate dielectric and surrounding material during CMOS processing. It is desirable to have a metal gate with a low sheet resistance that is compatible with CMOS process integration, either a conventional “gate first” or replacement “gate last” approach. Metallic elements, compounds (nitrides, silicides, carbides, borides, etc.), and solid solutions are possible candidates.

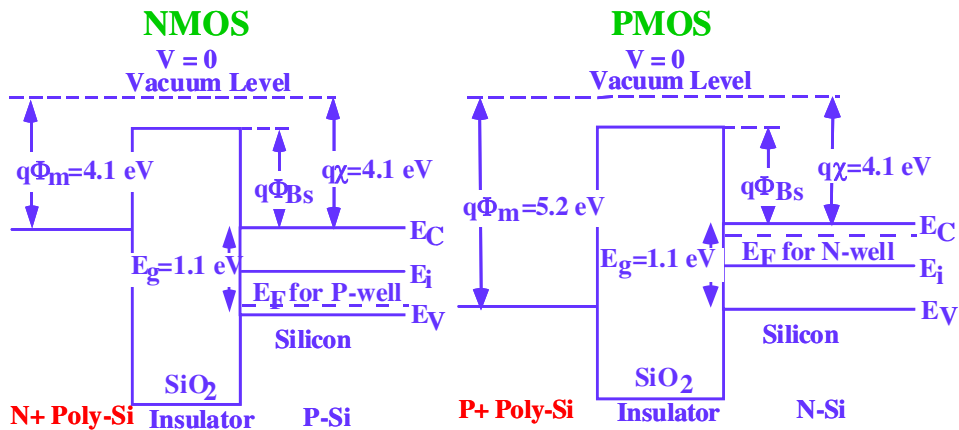


Fig. 16.

Work functions can be obtained from MOSCAPs of various oxide thicknesses using the following equation:

$$V_{fb} = \phi_{MS} + Q_F / C_{OX} \tag{6}$$

An intersect in the Y-axis of the V<sub>fb</sub> versus EOT plot is the work function (Figure 17). Table 2 shows the work function values for some potential metal gate electrode candidates.

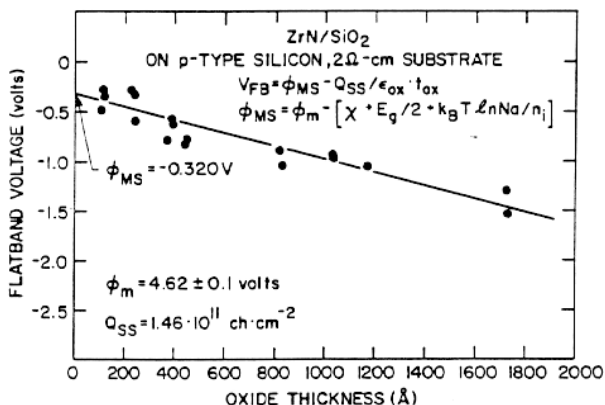


Fig. 17. [25]

Gate Material	Work Function (MOS) (eV)
Ti	4.17, 4.33, 4.6
TiN	4.95
TiSi2	3.67-4.25
Zr	4.05
ZrN	4.6
ZrSi2	-
Ta	4.25, 4.6, 4.15-4.25
TaN	5.41
TaSi2	4.15
Nb	4.3, 4.02-4.3
NbN	-
NbSi2	4.35-4.53
W	4.75, 4.72, 4.55-4.63
WNx	5
WSi2	4.55-4.8
Mo	4.64, 4.53-4.6
MoN	5.33
MoSi2	4.6-4.8, 4.9
Al	4.1

Table 2.

### 2.2.2 Metal electrode material deposition method and film properties

Metal deposition processing parameters and post-deposition processing affect the metal film properties such as resistivity, microstructure (grain size and orientation), stress, and adhesion. Deposition processes such as CVD and PVD are common methods. In general, CVD films provide better conformality and negligible damage compared to PVD films, but the process may incorporate contaminants. Atomic layer deposition (ALD) shows excellent conformality, but throughput is low. Figures 18 and 19 show the impact of the metal gate deposition process on device performance and gate leakage current, respectively. The device with a SiO<sub>2</sub>/PVD TiN metal gate stack results in lower mobility than CVD TiN or polysilicon gated devices. The devices with a SiO<sub>2</sub>/PVD TiN gate stack result in a 100X higher gate leakage current than devices fabricated with CVD and ALD.

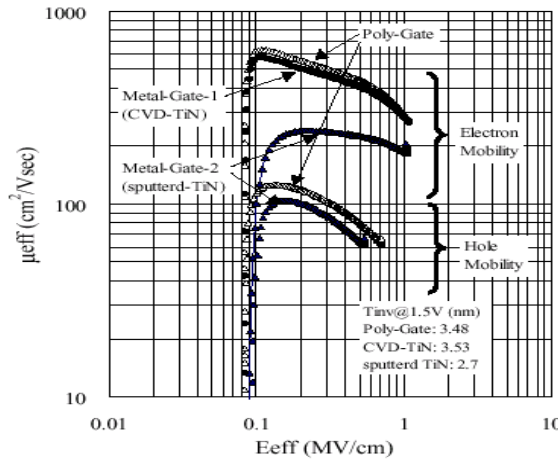


Fig. 18. [26]

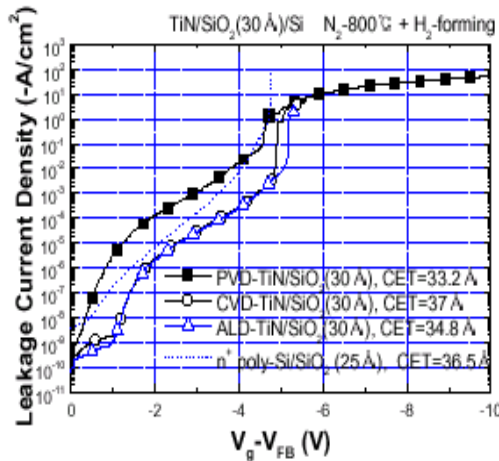


Fig. 19. [27]

### 2.2.3 Metal gate device integration issues

The dual metal gate approach that needs different metal gate materials for NMOS and PMOS, respectively, increases process complexity dramatically. Contamination (mostly from CVD) and plasma damage (mostly from PVD) affect gate device parameters such as  $Q_t$ ,  $D_{it}$ ,  $V_t$  stability, and gate oxide integrity. Another concern with metal gates is poor oxidation resistance. The etchability of metal materials, especially selectivity to metal oxides, is a key area for process development.

a. Conventional “Gate First” CMOS Integration

Conventional gate first integration involves the ability to etch the gate material. For example, Figure 20 shows a nitride/W/TiN gate electrode stack on top of gate oxide. The gate electrode materials must be protected from oxidation or attack by wet chemicals. The gate electrode materials must also be stable with their surrounding materials during high temperature steps. These requirements may limit the choices of materials for metal gate materials along with alternative high-k dielectrics.

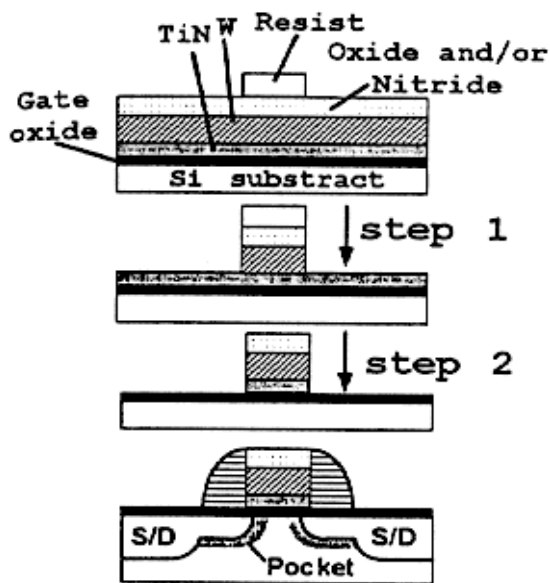


Fig. 20. [28, 29]

b. Replacement “Gate Last” CMOS Integration

This integration eliminates many constraints posed by conventional “gate first” integration such as process-induced damage, the requirement to etch new materials, thermal/chemical stability concerns, stress-induced diffusion issues. After completing conventional MOSFET fabrication with replacement polysilicon, gate oxide is deposited and using chemical-mechanical polishing (CMP) technique to flatten the top surface (Figure 20a). A wet etch or dry etch process is used to etch off the polysilicon gate (Figure 20b) followed by a new metal gate electrode material and a new gate dielectric deposition (Figure 20c). Another CMP process or a second patterning of the gate is used to form the final structure.

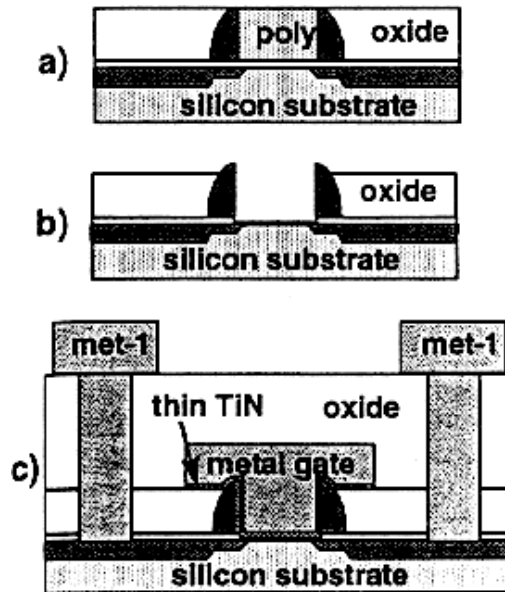


Fig. 20. [30]

c. Summary

A single metal gate with a mid-gap work function may not be able to achieve a low MOSFET threshold voltage and boost performance; however, it has potential for fully depleted silicon-on-insulator (FDSOI) applications. Dual metals with work functions similar to  $n^+$  polysilicon and  $p^+$  polysilicon pose significant integration challenges. Thermodynamic and mechanical stability is an important issue in the choice of metal gate materials. Both the gate first and gate last integration have advantages and disadvantages. The final choice of integration scheme will be decided by performance, yield, and cost.

### 3. Device characteristics using High-k/Metal Gate (HKMG) stack

#### 3.1 Impact of defects in the HKMG stack on device performance and reliability

As mentioned in section 2.1.1.d, the deposited high-k gate dielectric contains a high defect density in the bulk even after a post-deposition anneal (PDA). The quality of the interface between the silicon substrate and interfacial layer (IL) is not as good as the interface between silicon and conventional thermally grown gate oxide  $\text{SiO}_2$ . A TEM cross-section of the HKMG gate stack, shown in Figure 21, highlights the different regions of the gate stack. The defects in the bulk of the high-k gate dielectric and at the interface between the silicon substrate and IL have a significant impact on device performance and reliability, such as threshold voltage stability. As discussed in Section 2.1.2.a.iii, the best candidate for a high-k dielectric is Hf-based metal oxide. Therefore the following discussion is based on  $\text{HfO}_2$ /metal gate stacks.



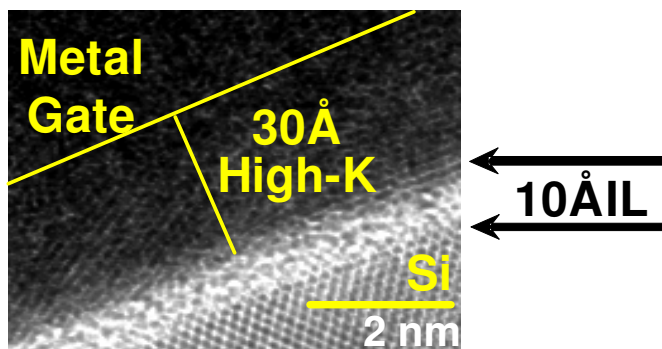


Fig. 21.

### 3.1.1 Si/IL interface improvement – stressed relaxed pre-oxide [31]

Depositing high-k on top of thick, high quality, thermally grown SiO<sub>2</sub>, taking the advantage of its better interface quality, is not desirable because we need a thin gate dielectric to increase transistor speed. To solve this problem, a stress relieved pre-oxide (SRPO) process has been developed to improve the interfacial properties between the high-k dielectric and silicon substrate while maintaining the required thinness to meet the speed enhancement requirement for integrated circuits. The experiment discussed here is as follows. The SRPO is formed by growing a relatively thick thermal oxide with a high temperature anneal (higher than the SiO<sub>2</sub> glass flow temperature of ~ 980°C) for stress relief followed by etching the thermal oxide back to 10 Å using a diluted 700:1 hydrofluoric acid: H<sub>2</sub>O solution. The HfO<sub>2</sub> is then deposited by ALD. After the high-k dielectric undergoes a PDA, a TaSiN metal gate is deposited. A commercial CMOS process technology with a source/drain anneal at 1000°C was used to fabricate metal gate/high-k stack nMOSFETs on bulk silicon [32]. Fig. 22 compares the threshold voltage ( $V_t$ ) shift under constant voltage stress for the control split using the standard process (an RCA clean followed by ALD HfO<sub>2</sub> with a TaSiN metal gate) and the new SRPO process with a TaSiN/HfO<sub>2</sub> gate stack for short channel devices ( $W/L = 10 \mu\text{m}/0.15 \mu\text{m}$ ). The SRPO with a TaSiN/HfO<sub>2</sub> stack results in a 3X smaller  $V_t$  shift than the standard process. These results suggest that devices with the standard process suffer process-induced gate edge damage during transistor fabrication, which increases the  $V_t$  shift due to greater trap generation. The process-induced gate edge damage is reduced significantly when using SRPO due to the high quality interfacial layer under the HfO<sub>2</sub>, which suppresses interface trap and border trap generation during constant voltage stress. To assess process-induced gate edge damage, the charge pumping current was measured on short channel devices using a pulse string with a fixed base level and varying pulse heights [33] under drain or source bias to detect local charge at the gate edge. The results show less interface and border state trap density for HfO<sub>2</sub>/SRPO devices than for HfO<sub>2</sub>/RCA devices. The stressed charge pumping results clearly show that the SRPO pre-treatment is much more robust than the RCA pre-treatment under process-induced local charge generation near gate edges. Fig. 23 shows that the normalized transconductance ( $G_m$ ) of TaSiN-gated short channel devices with SRPO is higher than the standard pre-treatment due to better interface properties with the SRPO process. The fundamental difference between a chemical

oxide formed after an RCA clean and SRPO is as follows. The quality of the chemical oxide is poor and has a lower density than thermally grown SiO<sub>2</sub>. It is susceptible to process-induced gate damage. On the other hand, for thermally grown SiO<sub>2</sub>, a mechanical stress builds up as the SiO<sub>2</sub> becomes thicker during oxidation caused by the molar volume mismatch between Si and SiO<sub>2</sub> and their different expansion coefficients. The stress degrades the Si-O bonding configuration near the interface between SiO<sub>2</sub> and the silicon substrate. The quality of the sub-oxide layer underneath the bulk SiO<sub>2</sub> is poor. It is therefore important to relieve the stress build-up during oxidation to have a high quality sub-oxide. Annealing the oxide at a temperature higher than the SiO<sub>2</sub> glass flow temperature (~980°C) allows the SiO<sub>2</sub> to “flow” and the bonding configuration near the interface to be rearranged, improving the sub-oxide quality. The SRPO process grows a relatively thick thermal oxide during a high temperature (~ 980°C) anneal, resulting in a high quality sub-oxide followed by an etch back to 10 Å using a diluted HF solution. The 10 Å SiO<sub>2</sub> serving as a pre-oxide before high-k deposition thus becomes a high quality film. Excellent cross-wafer inversion T<sub>ox</sub> uniformity is demonstrated using the SRPO pretreatment for an array of twenty-eight 10 μm × 10 μm (W/L) devices as shown in Fig. 24.

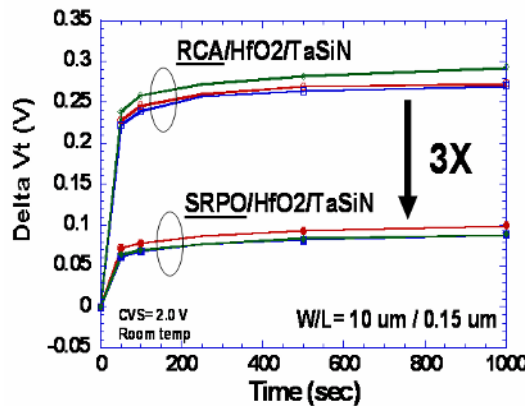


Fig. 22.

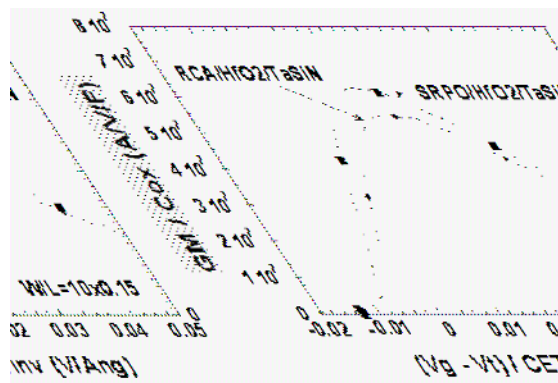


Fig. 23.

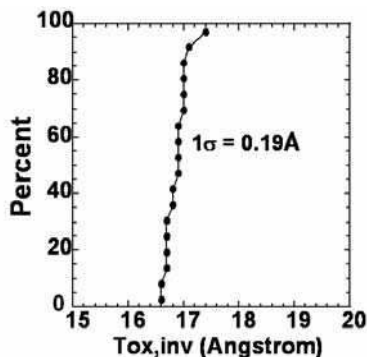


Fig. 24.

### 3.1.2 Si/IL interface improvement – deuterium incorporation [34]

The other approach to improve interface robustness is to incorporate deuterium into the interface between the silicon substrate and IL because the Si-D bonds are much harder to break than Si-H bonds. One effective way to incorporate deuterium is to use D<sub>2</sub>O instead of H<sub>2</sub>O as the oxidant precursors during ALD [34]. Introducing deuterium in situ during ALD is an effective way to passivate the Si dangling bonds because it does not require the pre-existing hydrogen to be replaced. Hydrogen can be introduced easily from the processes after high-k gate dielectric deposition. Fig. 25 compares the threshold shift for nMOSFETs under positive bias stressing at 25°C and 125°C. A significant reduction in V<sub>t</sub> shift is observed for D<sub>2</sub>O-processed HfO<sub>2</sub> devices. The presence of deuterium at the interface is supported by the low energy secondary ion mass spectroscopy (SIMS) analysis (Fig. 26), which reveals a spike of deuterium at the 7E17 at/cm<sup>3</sup> level. To improve the depth resolution of SIMS, we used 100 Å D<sub>2</sub>O-processed HfO<sub>2</sub> to prepare the test wafers. The SIMS analysis of another sample prepared by using 100 Å H<sub>2</sub>O-processed HfO<sub>2</sub> shows no deuterium at the bottom interface.

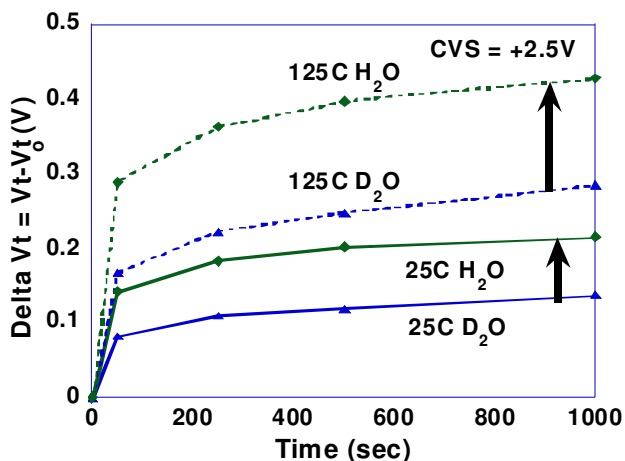


Fig. 25.

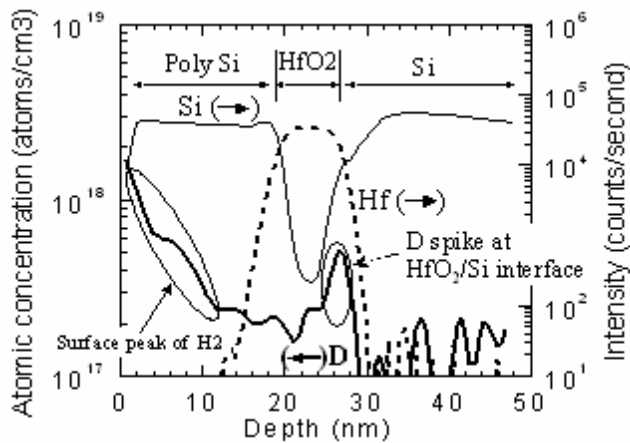


Fig. 26.

### 3.1.3 Fluorine passivation coupled with SRPO [35]

In addition to the defects at the interface, defects contained in the bulk HfO<sub>2</sub> will degrade device reliability and performance. Incorporating fluorine into the bulk HfO<sub>2</sub> and interfaces can passivate the defects, thus improving the device robustness and speed. Combining SRPO interface engineering and defect passivation with fluorine in a high-k/Ta<sub>x</sub>C<sub>y</sub> stack showed excellent  $V_t$  stability [35]. The positive bias temperature instability (PBTI) time to failure (TTF)-lifetime extraction using stress voltages in the direct tunneling regime is shown in Fig. 27. Fluorinated devices exceed the  $V_t$  TTF lifetime target (<30 mV  $V_t$  shift in 10 years at 105°C for  $V_{dd} = 1$  V) with a sufficient margin and reveal about a four orders of magnitude longer PBTI lifetime than the control that does not incorporate fluorine. SIMS analysis results confirmed the incorporation of fluorine at the interfaces and bulk high-k [35], which is expected to reduce the defect density and thus reduce charge trapping. It has been shown that oxygen vacancies are the major defects in the bulk HfO<sub>2</sub> [36]. Table 3 shows the results of atomistic calculations of the formation energies of fluorine-passivated oxygen vacancies in the bulk of the Hf-based high-k using density functional theory (DFT) [37, 38] as implemented in the local orbital SIESTA code [39]. The results show that the fluorine passivation of threefold (V3) or fourfold (V4) oxygen vacancies is energetically favorable and can therefore lead to less trapping. Fig. 28 shows the structure used to calculate a fluorine atom at a V3 site. The structure of the fluorine-passivated V4 defect (not shown) is similar. To electrically support the bulk trap density reduction from fluorine incorporation, stress-induced leakage current (SILC) was measured. Fig. 29 compares the SILC of fluorinated devices with the control. Fluorine incorporated in the bulk reduces the SILC significantly. The results are consistent with bulk defect passivation by incorporating fluorine. Finally, Fig. 30 shows the gate leakage for the fluorinated high-k/Ta<sub>x</sub>C<sub>y</sub> stack devices is over 4 orders of magnitude lower than that of silicon oxynitride. The CET<sub>inv</sub> is the sum of EOT and the quantum mechanical effect in the silicon substrate, which is around 0.4 nm.

Reaction	Energy Gain (eV)	F Coordination #	F Charge
Hf-V3-Hf + F(interstitial) → Hf-F-Hf	-7.66	3	7.18
Hf-V4-Hf + F(interstitial) → Hf-F-Hf	-7.66	3-4	7.18

Table 3.

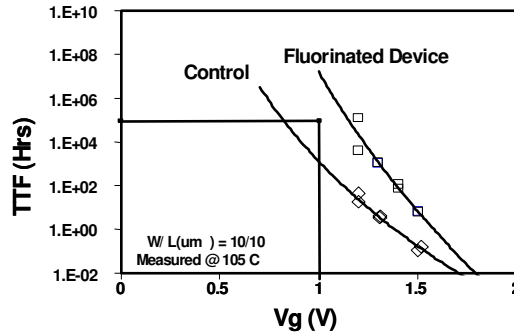


Fig. 27.

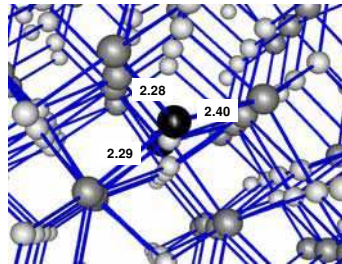


Fig. 28.

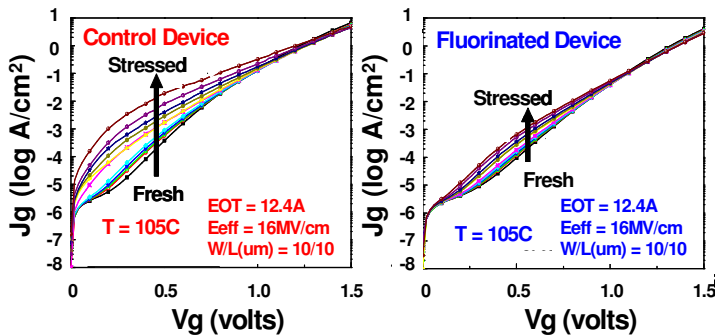


Fig. 29.

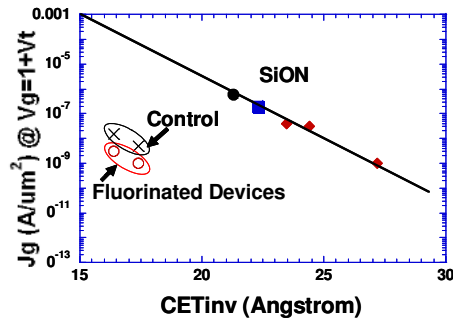


Fig. 30.

### 3.2 Threshold voltage turning

#### 3.2.1 Effective work function of metal gates

In an nMOSFET device, threshold voltage ( $V_t$ ) is the voltage at which electrons in the inversion layer formed at the substrate Si/dielectric interface are sufficient to produce a conducting path between the MOSFET source and drain (S/D). In CMOS applications, the effective work function (EWF) of metal gate electrodes is an important parameter as it determines the flatband voltage ( $V_{fb}$ ) and, subsequently, the  $V_t$  of MOSFETs. If no charge is present in the oxide or at the Si/dielectric interface, the  $V_{fb}$  equals the work function difference between the gate metal and the semiconductor substrate as shown in Eq. [7]. The work function values shown in Table 2 are based on this simple method. However, the work function of the metal, and thus the  $V_t$  obtained after the CMOS processing, is likely different from that obtained from Eq. [7]. The work function obtained after the CMOS processing is called the EWF, which determines the final  $V_t$  of CMOS.

A precise measurement of the metal gate EWF is crucial to identifying the optimal electrode material. However, EWF measurements of metal electrodes on high- $k$  dielectrics have shown a dependence on the particular dielectric material and are further complicated by Fermi-level pinning at the high- $k$ /metal interface [40]. Insufficient understanding of metal-electrode systems and their interactions with underlying dielectrics has contributed to inconsistent EWF values. It has further been reported that factors such as specific processing and associated thermal budgets affect the final EWF of high- $k$ /metal electrode systems [41] due to composition variations and the temperature-driven crystalline phase production of metal (metal oxides, metal nitrides, and metal oxynitrides) electrodes.

The EWF of metal electrodes on high- $k$  material may be extracted more precisely from MOS capacitors fabricated by depositing and patterning the high- $k$  dielectric and metal gate capacitor structures on a "terraced" oxide layer consisting of incrementally thicker layers of thermally grown  $\text{SiO}_2$  [42]. The multiple oxide thicknesses (1.0, 1.5, 2.5, 3.5 nm) on a single wafer are achieved by growing a relatively thick oxide and selectively etching regions with diluted hydrofluoric acid. Complete details of this etch process and evaluated work function results have been described previously [42]. Fig. 31 illustrates the bottom  $\text{SiO}_2$  terrace step thickness measurements recorded by spectroscopic ellipsometry (SE) in a diameter scan across the wafer. The wafer image insert in Fig 30 illustrates the concentric thickness bands. To evaluate metal gate work functions on high- $k$  films, a fixed amount of high- $k$  ( $\sim 2.0$  nm) is deposited on the terraced oxide followed by ALD of a 10 nm TiN (or other metal) gate

electrode. The EWFs for terraced oxide stacks were extracted using Eq. [7b] [42], which is a simplified form of the general model given by R. Jha [43] (Eq. [7a]) to enable linear extraction of the  $V_{fb}$ -EOT relationship:

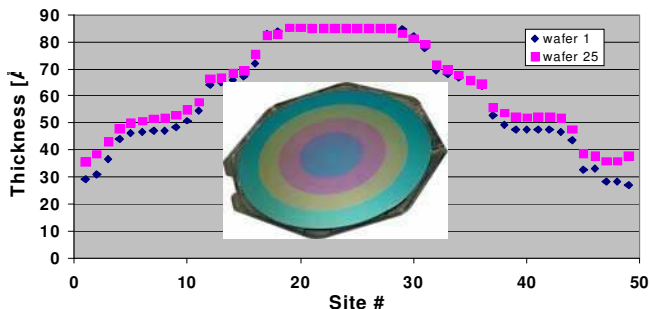


Fig. 31. Illustration of etched oxide thickness as a function of position across the diameter of a 200 mm wafer. [42]

$$\begin{aligned}
 a) V_{fb} &= \Phi'_{ms} - \frac{Q_f * EOT}{\epsilon_{ox}} - \left( \frac{Q_i * t_h}{\epsilon_h} - \frac{1}{\epsilon_h} \int_0^{t_h} x \rho_b(x) dx - \frac{1}{\epsilon_{ox}} \int_{t_h}^{t-t_h} x \rho_{ox}(x) dx \right), t_h = \frac{\epsilon_h}{\epsilon_{ox}} EOT h \\
 b) V_{fb} &= \left( \Phi'_{ms} - \frac{Q_i * EOT h}{\epsilon_{ox}} - \frac{\rho_b * \left( \frac{\epsilon_h}{\epsilon_{ox}} \right) * EOT h^2}{2 * \epsilon_{ox}} \right) - \frac{Q_f * EOT}{\epsilon_{ox}} \quad (7)
 \end{aligned}$$

With the terraced oxide structure, a constant fixed interface charge between the Si substrate and dielectric ( $Q_f$ ) is maintained across the varying oxide thicknesses, minimizing wafer-to-wafer variation associated with multiple wafer extraction methods.  $Q_f$  can be calculated from the slope of the  $V_{fb}$ -EOT relationship. The  $SiO_2$  bulk charge term in Ref. [43] can be neglected to simplify the extraction since this bulk charge contribution is far less than that of  $Q_f$  [44]. The extracted y-axis ordinate intercept value contains the contribution of the metal WF as well as the high-k/ $SiO_2$  interface charge ( $Q_i$ ) and high-k bulk charge density ( $\rho_b$ ) terms ( $t_h$ : high-k physical thickness,  $t_{ox}$ :  $SiO_2$  physical thicknesses,  $t$ : total physical thickness of high-k/ $SiO_2$  stack;  $EOT_h$ : high-k EOT; EOT: EOT of high-k/ $SiO_2$  stack,  $\epsilon_h$ : high-k dielectric constant,  $\epsilon_{ox}$ :  $SiO_2$  dielectric constant). The contributions of charges in the high-k on  $V_{fb}$  are controlled and can be minimized ( $\sim +50$  mV) by using a fixed and thinned high-k film (2–3 nm), thus enabling accurate extraction of the EWF. The resultant terraced oxide capacitors exhibit excellent linear  $V_{fb}$ -EOT fits with minimal effects from variations in fixed charge at the Si/ $SiO_2$  interface.

### 3.2.2 Dielectric capping for work function tuning

Although TaSiN (nMOS), TiN (pMOS), and Ru (pMOS) on  $HfO_2$  have been demonstrated in CMOS integration [45, 46], the use of dual metal gates must address the significant complexity of optimizing two different metal etch processes. A single metal gate approach for CMOS integration provides several advantages over the dual metal electrode process, specifically a more straightforward integration and less demanding gate etching process

optimization and control. A single metal gate, however, requires tuning the EWF value to obtain the proper n- and p-type threshold voltage. These tuning efforts have given rise to an extensive study of the impact of capping layer, a thin metal oxide incorporated between the Hf-based high-k dielectrics and metal gates, whereby a single metal gate CMOS process can be implemented with either single or dual cap layer approaches [47]–[52].

Thin cap layers ( $\leq 1$  nm) such as  $\text{Dy}_2\text{O}_3$  and  $\text{Al}_2\text{O}_3$  deposited on the high-k gate dielectric followed by thermal annealing drives the metal atoms of the cap layer into the high-k layer (and bottom  $\text{SiO}_x$  interface layer). Appropriate control of cap layer doping (depth of diffusion) has tuned the EWF of metal electrodes by dipole formation at the interface between the high-k and bottom interfacial  $\text{SiO}_x$  layer. The EWF of metal electrodes can be shifted toward the valence and conduction bands of Si using  $\text{AlO}_x$  and  $\text{LaO}_x$  capping layers, respectively [52]–[55]. Performance data suggests that  $\text{AlO}_x$  capping is also effective after high temperature processing, indicating that Al atoms need to diffuse to the interface between the  $\text{HfO}_2$  and the interfacial  $\text{SiO}_2$  layer to shift the EWF [56]. Modulating  $\text{LaO}_x$  within the  $\text{HfO}_2$  has been shown to contribute to this EWF shift as a result of La concentration at the  $\text{SiO}_x/\text{HfO}_2$  interface. The relative concentration trends with the amount of EWF shift [57]. Coincident Hf and La EELS element profiles and SIMS profiles in Fig. 32 and Fig. 33, respectively, verify that La migrates from a  $\text{La}_2\text{O}_3$  cap layer into un-annealed  $\text{HfO}_2$  [58]. These observations can make the dipole moment formed at the internal interface a more feasible explanation for EWF tuning.

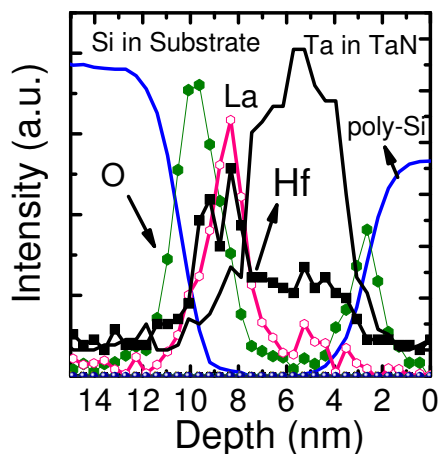


Fig. 32. EELS scan showing intermixing of  $\text{HfSiO}$  and  $\text{La}_2\text{O}_3$ .

Analysis of the energy band diagram of the multilayer dielectric stack suggests that the EWF of the gate stack can be modified by the dipole at the interface between two dielectric layers, typical of the high-k gate stack (i.e., the  $\text{Si}/\text{SiO}_x/\text{HfO}_2/\text{electrode}$ , where a  $\text{SiO}_2$ -like IL is formed). As indicated above, such a dipole layer can be formed by introducing metal ions into the IL near its interface with the high-k film. The electronegativity of the metallic elements with respect to Hf atoms presents a plausible case for a model explaining EWF tuning [59]. Fig. 34 illustrates the effect of a band offset change between the high-k and interfacial oxide induced by incorporating metal ions into the interfacial layer. A metallic element can be incorporated in the IL by diffusion during thermal processing, specifically



with a high temperature ( $\sim 1000^\circ\text{C}$ ) S/D dopant activation anneal. Based on their electronegativity relative to Hf, metallic elements can generate either “positive” (i.e., Al (Ti)-O-Hf) or “negative” dipoles resulting in a higher or lower EWF, respectively. Furthermore, ab initio calculations show that the Al-O-Hf dipole results from substituting Al for Si in  $\text{SiO}_2$  near its interface with  $\text{HfO}_2$ , thereby significantly reducing the  $\text{SiO}_2$ /high-k valence band offset and thus effectively increasing the EWF [60].

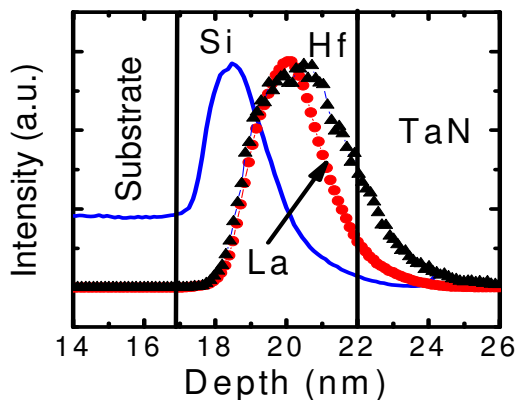


Fig. 33. SIMS profile confirms intermixing of  $\text{La}_2\text{O}_3$  with the HfSiO layer.

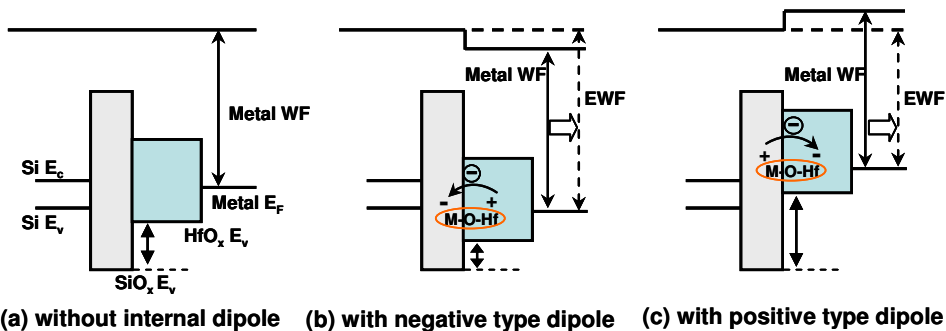


Fig. 34. Band diagram illustrating the EWF change of the metal gate depending on the type of dipole.

In nFETs, La is found to be the most effective dopant based on its overall effect on  $V_{th}$ , EOT scaling, mobility, and reliability [50, 53, 54]. An  $\text{Al}_2\text{O}_3$  cap has been widely used for pFETs, but it increased the EOT [52] (since it has a relatively lower dielectric constant value) as well as raises reliability concerns due to Al diffusing into the interfacial oxide layer [52]. In addition, the  $V_{th}$ -EOT roll-off phenomenon (see next section) was observed in  $\text{Al}_2\text{O}_3$ -capped gate stacks, making it even more difficult to achieve a proper  $V_{th}$  ( $V_i$ ) for pMOS.

### 3.2.3 $V_{th}$ -EOT Roll-Off

When gate stack film systems consisting of a metal electrode, high-k dielectric, and  $\text{SiO}_2$  IL were used in devices of practical interest with scaled EOTs, their  $V_{th}$  values at thin gate

stacks were found to be significantly less than those obtained in test structures with thicker gate stacks. This is most remarkable in gate stacks with high EWFs [61], as seen in Fig. 35 showing a grand plot of  $V_{fb}$  vs. EOT in pMOSCAPs with various metal gates fabricated on terraced oxide structures. The  $V_{fb}$  roll-off starts at a certain minimal thickness of the  $\text{SiO}_2$  IL and increases as the  $\text{SiO}_2$  becomes thinner. One can clearly see a gradual reduction of  $V_{fb}$  as the gate stack EOT scales below a certain value. It is more prominent in gate stacks annealed at higher temperatures and/or for a longer anneal time. This  $V_{fb}$ -EOT roll-off phenomenon is a thermally activated process that suggests an intrinsic relation to the EWF values of the gate stack and/or the change in electrical integrity of the physically scaled bottom interface layer.

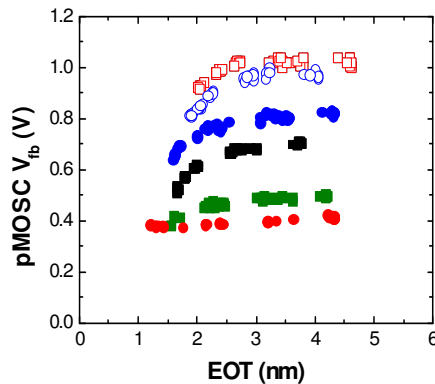


Fig. 35. Dependence of  $V_{fb}$  on EOT in high-k terraced oxide capacitors with metal electrodes of different WF values.

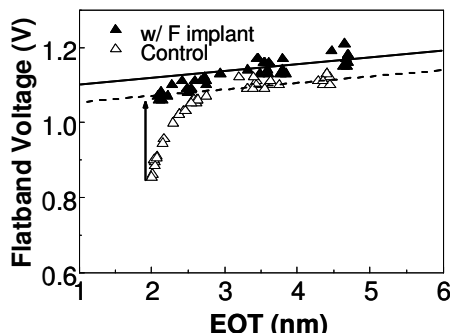


Fig. 36. Advantages of fluorine incorporation for  $V_{fb}$ -EOT roll-off reduction

The likely root cause of the  $V_{fb}$ -EOT roll-off problem in HKMG devices is the oxygen vacancies in the high-k stack, which trigger the generation of defects at the bottom of the  $\text{SiO}_2/\text{Si}$  interface. Therefore processes that can minimize the oxygen vacancy density in the high-k bulk and/or enhance the robustness of the  $\text{SiO}_2/\text{Si}$  interface are critical to reducing the  $V_{fb}$ -EOT roll-off in advanced HKMG devices. From the point of view of interface quality, stress in the transitional region of the  $\text{SiO}_2$  interfacial layer enhances the diffusion of oxygen up from the interface, which makes the  $V_t$  roll-off problem more severe. Therefore a stress-

relieved SiO<sub>2</sub>/Si interface is desirable to minimize V<sub>t</sub> roll-off. The SRPO process, deuterium incorporation, and the combination of SRPO with defect passivation with fluorine (see section 3.1.3) are effective approaches to minimize the V<sub>fb</sub>-EOT roll-off problem. Indeed, F<sup>+</sup> implanted in the gate stack with 1 nm SiO<sub>2</sub> under 2 nm HfSiO<sub>x</sub> followed by a 1000°C/10 sec. anneal [62] significantly reduces the roll-off (Fig. 36).

#### 4. Conclusion

The high-k/metal gate stack has been used for high performance and low power semiconductor products replacing the SiO<sub>2</sub>/polysilicon stack, which has been used for decades. The motivation for this replacement as well as materials screening for the high-k/metal gate stack have been discussed. Two major advantages of implementing HKMG stacks are that they contribute to reducing the gate leakage current and scaling the EOT of advanced CMOS. Progress in high-k/metal gate device threshold voltage tuning, including an evaluation of capping layers, has also been presented. While nMOS V<sub>t</sub> is acceptable for various applications of Si CMOS devices, achieving a targeted pMOS V<sub>t</sub> is still challenging due to V<sub>fb</sub>-EOT roll-off issues. Approaches to minimize the pMOS V<sub>fb</sub>-EOT roll-off problem have been outlined. Clearly, CMOS scaling will continue to provide opportunities for exciting research in high-k/metal gate modules in the future.

#### 5. References

- [1] X. Guo, X. Wang, Z. Luo, T. P. Ma, and T. Tamagawa, "High quality ultra-thin (1.5 nm) TiO<sub>2</sub>/Si<sub>3</sub>N<sub>4</sub> gate dielectric for deep sub-micron CMOS technology," IEDM Tech. Dig., pp. 137 - 140, December 1999
- [2] C. Hobbs, R. Hegde, B. Maiti, H. Tseng, D. Gilmer, P. Tobin, O. Adetutu, F. Huang, D. Weddington, R. Nagabushnam, D. O'Meara, K. Reid, L. La, L. Grove and M. Rossow, "Sub-Quarter Micron CMOS Process for TiN-Gate MOSFETs with TiO<sub>2</sub> Gate Dielectric formed by Titanium Oxidation," Symp. on VLSI Tech. Dig., 1999, P. 133-134
- [3] Donggun Park; Ya-chin King; Qiang Lu; Tsu-Jae King; Chenming Hu; Kalnitsky, A.; Sing-Pin Tay; Chia-Cheng Cheng, "Transistor characteristics with Ta<sub>2</sub>O<sub>5</sub> gate dielectric," IEEE EDL, P. 441-443, 1998
- [4] Campbell, S.A.; Gilmer, D.C.; Xiao-Chuan Wang; Ming-Ta Hsieh; Hyeon-Seag Kim; Gladfelter, W.L.; Jinhua Yan, "MOSFET transistors fabricated with high permittivity TiO<sub>2</sub> dielectrics," IEEE, TED, P. 104-109, 1997
- [5] D. A. Buchanan, E. P. Gusev, E. Cartier, H. Okorn-Schmidt, K. Rim, M. A. Gribelyuk, A. Mocuta, A. Ajmera, M. Copel, S. Guha, N. Bojarczuk, A. Callegari, C. D'Emic, P. Kozlowski, K. Chan, R. J. Fleming, P. C. Jamison, J. Brown, and R. Arndt, "80 nm Poly-silicon gated n-FETs with ultra-thin Al<sub>2</sub>O<sub>3</sub> gate dielectric for ULSI applications," IEDM Tech. Dig., pp. 223 - 226, December 2000.
- [6] J. H. Lee, K. Koh, N. I. Lee, M. H. Cho, Y. K. Kim, J. S. Jeon, K. H. Cho, H. S. Shin, M. H. Kim, K. Fujihara, H. K. Kang, and J. T. Moon, "Effect of polysilicon gate on the flatband voltage shift and mobility degradation for ALD-Al<sub>2</sub>O<sub>3</sub> gate dielectric," IEDM Tech. Dig., pp. 645 - 648, December 2000.

- [7] A. Chin, Y-H Wu, S. B. Chen, C. C. Liao, and W. J. Chen, "High quality  $\text{La}_2\text{O}_3$  and  $\text{Al}_2\text{O}_3$  gate dielectrics with equivalent oxide thickness 5-10 Å," Symp. on VLSI Tech. Dig., 2000, P. 16-19
- [8] Katsunori Onishi, Laegu Kang, Rino Choi, Easwar Dharmarajan, Sundar Gopalan, Yongjoo Jeon, Chang Seok Kang, Byoung Hun Lee, Renee Nieh, and Jack C. Lee, "Dopant Penetration Effects on Polysilicon Gate  $\text{HfO}_2$  MOSFET's," Symp. on VLSI Tech. Dig., 2001, P. 131
- [9] S. J. Lee, H. F. Luan, W. P. Bai, C. H. Lee, T. S. Jeon, Y. Senzaki, D. Roberts, and D. L. Kwong, "High quality ultra thin CVD  $\text{HfO}_2$  gate stack with poly-Si gate electrode," IEDM Tech. Dig., pp. 31 - 34, December 2000.
- [10] C. Hobbs, H.-H. Tseng, K. Reid, B. Taylor, L. Dip, L. Mebert, R. Garcia, R. Hegde, J. Grant, D. Gilmer, A. Granke, V. Dhandapani, M. Azrak, L. Prabhu, R. Rai, S. Bagchi, J. Conner, S. Backer, F. Dumbuya, B. Nguyen, and P. Tobin, "80 nm poly-Si gate CMOS with  $\text{HfO}_2$  gate dielectric," IEDM Tech. Dig., 2001, P. 651-654
- [11] W. Zhu and T. P. Ma, " $\text{HfO}_2$  and  $\text{HfAlO}$  for CMOS: thermal stability and current transport," IEDM Tech. Dig., 2001, P. 463-466
- [12] L. Kang, K. Onishi, Y. Jeon, B. H. Lee, C. Kang, W. Qi, R. Nieh, S. Gopalan, R. Choi, and J. C. Lee, "MOSFET Devices with polysilicon on single-layer  $\text{HfO}_2$  high-K dielectrics," IEDM Tech. Dig., pp. 35 - 38, December 2000.
- [13] W. Qi, R. Nieh, B. H. Lee, L. Kang, Y. Jeon, K. Onishi, T. Ngai, S. Banerjee, and J. C. Lee, "MOSCAP and MOSFET characteristics using  $\text{ZrO}_2$  gate dielectric deposited directly on Si," IEDM Tech. Dig., pp. 145 - 148, December 1999.
- [14] C. H. Lee, H. F. Luan, W. P. Bai, S. J. Lee, T. S. Jeon, Y. Senzaki, D. Roberts, and D. L. Kwong, "MOS Characteristics of ultra thin rapid thermal CVD  $\text{ZrO}_2$  and Zr silicate gate dielectrics," IEDM Tech. Dig., pp. 27 - 30, December 2000.
- [15] Z. J. Luo, T. P. Ma, E. Cartier, M. Copel, T. Tamagawa, and B. Halpern, "Ultra-thin  $\text{ZrO}_2$  (or Silicate) with High Thermal Stability for CMOS Gate Applications," Symp. on VLSI Tech. Dig., 2001, P. 135-136
- [16] W.-J. Qi, R. Nieh, B. H. Lee, K. Onishi, L. Kang, Y. Jeon, J. Lee, V. Kaushik, B-Y Neuyen, L. Prabhu, K. Eisenbeiser, and J. Finder, "Performance of MOSFETs with ultra thin  $\text{ZrO}_2$  and Zr silicate gate dielectrics," Symp. on VLSI Tech. Dig., 2000, P. 40-41
- [17] C. Hobbs, L. Dip, K. Reid, D. Gilmer, R. Hegde, T. Ma, B. Taylor, B. Cheng, S. Samavedam, H. Tseng, D. Weddington, F. Huang, D. Farber, M. Schippers, M. Rendon, L. Prabhu, R. Rai, S. Bagchi, J. Conner, S. Backer, F. Dumbura, J. Locke, D. Workman, and P. Tobin, "Sub-Quarter micron Si-gate CMOS with  $\text{ZrO}_2$  gate dielectric," Symp. on VLSI Technology, Systems, and Applications, Tech. Dig., P. 204-207, 2001, Taipei, Taiwan
- [18] H.-H. Tseng, P. J. Tobin, S. Kalpat, J. K. Schaeffer, M. E. Ramón, L. Fonseca, Z. X. Jiang, R. I. Hegde, D. H. Triyoso, and S. Semavedam, "Defect Passivation with Fluorine and Interface Engineering for Hf-based High-K/Metal Gate Stack Device Reliability and Performance Enhancement," IEDM Tech. Dig., 2005, P. 713-716
- [19] R. Beyers, "Thermodynamic considerations in refractory metal-silicon-oxygen systems," J. Appl. Phys. 56, 147 (1984)
- [20] S. Q. Wang and J. W. Mayer, "Reactions of Zr thin films with  $\text{SiO}_2$  substrates," Journal of Applied Physics Volume 64, Issue 9, Nov 1988 Page(s):4711 - 4716

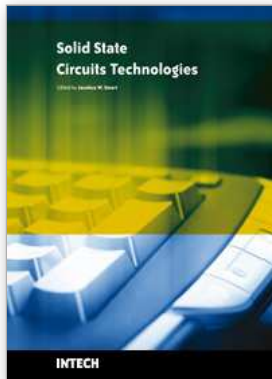
- [21] G. D. Wilk and R. M. Wallace, "Stable zirconium silicate gate dielectrics deposited directly on silicon," *Applied Physics Letters* Volume 76, Issue 1, Jan 2000 Page(s):112 - 114
- [22] G. D. Wilk, R. M. Wallace, and J. M. Anthony, "High- $\kappa$  gate dielectrics: Current status and materials properties considerations," *Journal of Applied Physics* Volume 89, Issue 10, May 2001 Page(s):5243 - 5275
- [23] E. P. Gusev et al., AVS Topical Conf. on Atomic Layer Deposition, May 14, 2001
- [24] M. Ritala and M. Leskela, "Atomic Layer Deposition," *Handbook of Thin Film Materials*, H. S. Nalwa ed., Academic Press, 2001, Vol.1, Chap. 2
- [25] L. Krusin Elbaum et al., *Mat. Res. Soc. Symp. Proc* Vol. 171, P. 351, 1986
- [26] S. Matsuda, H. Yamakawa, A. Azuma and Y. Toyoshima, "Performance Improvement of Metal Gate CMOS Technologies," *Symp. on VLSI Tech. Dig.*, 2001, P. 63-64
- [27] Dae-Gyu Park, Kwan-Yong Lim, Heung-Jae Cho, Tae-Ho Cha, Joong-Jung Kim, Jung-Kyu Ko, In-Seok Yeo, and Jin Won Park, "Novel Damage-free Direct Metal Gate Process Using Atomic Layer Deposition," *Symp. on VLSI Tech. Dig.*, 2001, P. 65-66
- [28] J. C. Hu, H. Yang, R. Kraft, A. L. P. Rotondaro, S. Hattangady, W. W. Lee, R. A. Chapman, C. Chao, A. Chatterjee, M. Hanratty, M. Rodder, and I. Chen, "Feasibility of using W/TiN as metal gate for conventional 0.13 $\mu\text{m}$  CMOS technology and beyond," *IEDM Tech. Dig.*, pp. 825 - 828, December 1997.
- [29] B. H. Lee, R. Choi, L. Kang, S. Gopalan, R. Nieh, K. Onishi, Y. Jeon, W. Qi, C. Kang, and J. C. Lee, "Characteristics of TaN gate MOSFET with ultrathin hafnium oxide (8  $\text{\AA}$  - 12  $\text{\AA}$ )," *IEDM Tech. Dig.*, pp. 39 - 42, December 2000.
- [30] A. Chatterjee, R. A. Chapman, G. Dixit, J. Kuehne, S. Hattangady, H. Yang, G. A. Brown, R. Aggarwal, U. Erdogan, Q. He, M. Hanratty, D. Rogers, S. Murtaza, S. J. Fang, R. Kraft, A. L. P. Rotondaro, J. C. Hu, M. Terry, W. Lee, C. Fernando, A. Konecni, G. Wells, D. Frystak, C. Bowen, M. Rodder, and I. Chen, "Sub-100nm gate length metal gate NMOS transistors fabricated by a replacement gate process," *IEDM Tech. Dig.*, pp. 821 - 824, December 1997.
- [31] H.-H. Tseng, C. C. Capasso, J. K. Schaeffer, E. A. Hebert, P. J. Tobin, D. C. Gilmer, D. Triyoso, M. E. Ramon, S. Kalpat, E. Luckowski, W. J. Taylor, Y. Jeon, O. Adetutu, R. I. Hegde, R. Noble, M. Jahanbani, C. El Chemali, and B. E. White, "Improved short channel device characteristics with stress relieved pre-oxide (SRPO) and a novel tantalum carbon alloy metal gate/HfO<sub>2</sub>/ stack," in *IEDM Technical Digest*, 2004, pp. 821-824
- [32] A. H. Perera, B. Smith, N. Cave, M. Sureddin, S. Chheda, R. Islam, J. Chang, S.-C. Song, A. Sultan, S. Crown, V. Kolagunta, S. Shah, M. Celik, D. Wu, K. C. Yu, R. Fox, S. Park, C. Simpson, D. Eades, S. Gonzales, C. Thomas, J. Sturtevant, D. Bonser, N. Benavides, M. Thompson, V. Sheth, J. Fretwell, S. Kim, N. Ramani, K. Green, M. Moosa, P. Besser, Y. Solomentsev, D. Denning, M. Friedemann, B. Baker, R. Chowdhury, S. Ufmani, K. Strozewski, R. Carter, J. Reiss, M. Olivares, B. Ho, T. Lii, T. Sparks, T. Stephens, M. Schaller, C. Goldberg, K. Junker, D. Wristers, J. Alvis, B. Melnick, and S. Venkatesan, "A versatile 0.13  $\mu\text{m}$  CMOS platform technology supporting high performance and low power applications," *IEDM Technical Digest*, 2000, pp571-574

- [33] W. Chen and T. P. Ma, "A new technique for measuring lateral distribution of oxide charge and interface traps near MOSFET junctions," *IEEE Electron Device Letters*, vol. 12, no. 7, pp. 393 – 395, July, 1991
- [34] H.-H. Tseng, M. E. Ramon, L. Hebert, P. J. Tobin, D. Triyoso, J. M. Grant, Z. X. Jiang, D. Roan, S. B. Samavedam, D. C. Gilmer, S. Kalpat, C. Hobbs, W. J. Taylor, O. Adetutu, and B. E. White, "ALD HfO<sub>2</sub> using heavy water (D<sub>2</sub>O) for improved MOSFET stability," *IEDM Technical Digest*, 2003, pp 83-86
- [35] H.-H. Tseng, P. J. Tobin, S. Kalpat, J. K. Schaeffer, M. E. Ramon, L. Fonseca, Z. X. Jiang, R. I. Hegde, D. H. Triyoso, and S. Semavedam, "Defect Passivation with Fluorine and Interface Engineering for Hf-based High-K/Metal Gate Stack Device Reliability and Performance Enhancement," *IEEE Transactions on Electron Devices*, Volume 54, Number 12, December 2007, pp. 3267-3275
- [36] X. Xiong and J. Robertson, "Defect energy levels in HfO<sub>2</sub> high-dielectric-constant gate oxide," *Applied Physics Letters*, vol. 87, 183505, 2005
- [37] P. Hohenberg and W. Kohn, "Inhomogeneous Electron Gas," *Phys Rev.* 136, B864-B871, 1964
- [38] W. Kohn and L. J. Sham, "Self-Consistent Equations Including Exchange and Correlation Effects," *Phys. Rev.* 140, A1133-A1138, 1965
- [39] J. M. Soler, E. Artacho, J. D Gale, A. Garcia, J. Junquera, P. Ordejón, and D. Sánchez-Portal, "The SIESTA method for ab initio order-N materials simulation," *J. Phys.: Condens. Matter* 14, pp. 2745-2779, 2002
- [40] Y.-C. Yeo, P. Ranade, T.-J. King, and C. Hu, "Effects of high- $\kappa$  gate dielectric materials on metal and silicon gate workfunctions," *IEEE Electron Device Lett.*, vol. 23, no. 6, pp. 342-344, Jun. 2002.
- [41] H. Y. Yu, C. Ren, Y.-C. Yeo, J. F. Kang, X. P. Wang, H. H. H. Ma, M.-F. Li, D. S. H. Chan, D.-L. Kwong, "Fermi Pinning Induced Thermal Instability of Metal Gate Work Functions," *IEEE Electron Device Letters*, vol. 25, p337, May 2004.
- [42] G. A. Brown, G. Smith, J. Saulters, K. Matthews, H.-C. Wen, H. AlShareef, P. Majhi, and B. H. Lee, "An improved methodology for gate electrode work function extraction in SiO<sub>2</sub> and high-k gate stack systems using terraced oxide structures," in *Proc. SISC*, 2004, p. 15. 2004.
- [43] R. Jha, J. Gurganos, Y. H. Kim, R. Choi, J. Lee, and V. Misra, "A capacitance-based methodology for work function extraction for metals on high-K," *IEEE Electron Device Letter*, vol. 25, pp. 420-423, 200
- [44] G. D. Wilk, M. L. Green, M.-Y. Ho, B. W. Busch, T. W. Sorsch, F. P. Klemens, B. Brijs, R. B. van Dover, A. Kornblit, T. Gustafsson, E. Garfunkel, S. Hillenius, D. Monroe, P. Kalavade, and J. M. Hergenrother, "Improved Film Growth and Flatband Voltage Control of ALD HfO<sub>2</sub> and Hf-Al-O with n<sup>+</sup> poly-Si Gates using Chemical Oxides and Optimized Post-Annealing," in *VLSI Symp. Tech. Dig.*, 2002, pp. 88-89.
- [45] S. B. Samavedam, L. B. La, J. Smith, S. Dakshina-Murthy, E. Luckowski, J. Schaeffer, M. Zavala, R. Martin, V. Dhandapani, D. Triyoso, H. H. Tseng, P. J. Tobin, D. C. Gilmer, C. Hobbs, W. J. Taylor, J. M. Grant, R. I. Hegde, J. Mogab, C. Thomas, P. Abramowitz, M. Moosa, J. Conner, J. Jiang, V. Arunachalam, M. Sadd, B.-Y. Nguyen, B. White, "Dual-metal gate CMOS with HfO<sub>2</sub> gate dielectric," in *IEDM Tech. Dig.*, 2002, pp. 433-436.

- [46] Z. B. Zhang, S. C. Song, C. Huffman<sup>1</sup>, J. Barnett, N. Moumen, H. Alshareef, P. Majhi, M. Hussain, M. S. Akbar, J. H. Sim, S. H. Bae, B. Sassman, and B. H. Lee, "Integration of Dual Metal Gate CMOS with TaSiN (NMOS) and Ru (PMOS) Gate Electrodes on HfO<sub>2</sub> Gate Dielectric," in VLSI Symp. Tech. Dig., 2005, pp.50-51.
- [47] S. Kubicek, T. Schram, V. Paraschiv, R. Vos, M. Demand, C. Adelman, T. Witters, L. Nyns, L.-Å. Ragnarsson, H. Yu, A. Veloso, R. Singanamalla, T. Kauerauf, E. Rohr, S. Brus, C. Vrancken, V. S. Chang, R. Mitsuhashi, A. Akheyar, H.-J. Cho, J. C. Hooker, B. J. O'Sullivan, T. Chiarella, C. Kerner, A. Delabie, S. Van Elshocht, K. De Meyer, S. De Gendt, P. Absil, T. Hoffmann and S. Biesemans, "Low V<sub>T</sub> CMOS using doped Hf-based oxides, TaC-based Metals and Laser-only Anneal," in IEDM Tech. Dig., 2007, pp. 49-52.
- [48] T. Schram, S. Kubicek, E. Rohr, S. Brus, C. Vrancken, S.-Z. Chang, V.S. Chang, R. Mitsuhashi, Y. Okuno, A. Akheyar, H.-J. Cho, J.C. Hooker, V. Paraschiv, R. Vos, F. Sebai, M. Ercken, P. Kelkar, A. Delabie, C. Adelman, T. Witters, L-A. Ragnarsson, C. Kerner, T. Chiarella, M. Aoulaiche, Moon-Ju Cho, T. Kauerauf, K.De Meyer, A. Lauwers, T. Hoffmann, P. P. Absil and S. Biesemans, "Novel Process To Pattern Selectively Dual Dielectric Capping Layers Using Soft-Mask Only," in VLSI Symp. Tech. Dig., 2008, pp.44-45.
- [49] X. Chen, S. Samavedam, V. Narayanan, K. Stein, C. Hobbs, C. Baiocco, W. Li, D. Jaeger, M. Zaleski, H. S. Yang, N. Kim, Y. Lee, D. Zhang, L. Kang, J. Chen H. Zhuang, A. Sheikh, J. Wallner, M. Aquilino, J. Han, Z. Jin, J. Li, G. Massey, S. Kalpat, R. Jha, N. Moumen, R. Mo, S. Kirshnan, X. Wang, M. Chudzik, M. Chowdhury, D. Nair, C. Reddy, Y. W. Teh, C. Kothandaraman, D. Coolbaugh, S. Pandey, D. Tekleab, A. Thean, M. Sherony, C. Lage, J. Sudijono, R. Lindsay, J. H. Ku, M. Khare, A. Steegen, "A Cost Effective 32nm High-K/ Metal Gate CMOS Technology for Low Power Applications with Single-Metal/Gate-First Process," in VLSI Symp. Tech. Dig., 2008, pp. 88-89.
- [50] P. Kirsch, M. A. Quevedo-Lopez, S. A. Krishnan, C. Krug, H. AlShareef, C. S. Park, R. Harris, N. Moumen, A. Neugroschel, G. Bersuker, B.H. Lee, J.G. Wang, G. Pant, B. E. Gnade, M. J. Kim, "Band Edge n-MOSFETs with High-k/Metal Gate Stacks Scaled to EOT=0.9nm with Excellent Carrier Mobility and High Temperature Stability," in IEDM Tech. Dig., 2006, p.639-642.
- [51] J. Huang, P. D. Kirsch, D. Heh, C. Y. Kang, G. Bersuker, M. Hussain, P. Majhi, P. Sivasubramani, D. C. Gilmer, N. Goel, M.A. Quevedo-Lopez, C. Young, C. S. Park, C. Park, P. Y. Hung, J. Price, H. R. Harris, B.H. Lee, H.-H. Tseng and R. Jammy, "Device and Reliability Improvement of HfSiON+LaOx/Metal Gate Stacks for 22nm," Node Application in IEDM Tech. Dig., 2008, pp. 45-48.
- [52] S. C. Song, Z. B. Zhang, M. M. Hussain, C. Huffman, J. Barnett, S. H. Bae, H. J. Li, P. Majhi, C. S. Park, B. S. Ju, H. K. Park, C. Y. Kang, R. Choi, P. Zeitsoff, H. H. Tseng, B. H. Lee, and R. Jammy, "Highly manufacturable 45 nm LSTP CMOSFETs using novel dual high-κ and dual metal gate CMOS integration," in VLSI Symp. Tech. Dig., 2006, pp. 16-17.
- [53] V. Narayanan, V. K. Paruchuri, N. A. Bojarczuk, B. P. Linder, B. Doris, Y. H. Kim, S. Zafar, J. Stathis, S. Brpwn, J. Arnold, M. Copel, M. Steen, E. Cartier, A. Callegari, P. Jamison, J.-P. Locquet, D. L. Lacey, Y. Wang, P. E. Batson, P. Ronsheim, P. Jammy, M. P. Chudzik, M. Jeong, S. Guha, G. Shahidi, and T. C. Chen , "Band-edge high-

- performance High-k/metal gate n-MOSFETs using cap-layers containing group IIA and IIB elements with gate-first processing for 45 nm and beyond," in VLSI Symp. Tech. Dig., 2006, pp. 224-225.
- [54] H. Alshareef, M. Quevedo-Lopez, H. Wen, R. Harris, P. Kirsch, P. Majhi, B. Lee, R. Jammy, D. Lichtenwalner, J. Jur, and A. Kingon, "Work function engineering using lanthanum oxide interfacial layers," *Appl. Phys. Lett.*, vol. 89, no. 23, pp. 232 103-1-232 103-3, Dec. 2006.
- [55] L.-Å. Ragnarsson, V. S. Chang, H.Y. Yu, H.-J. Cho, T. Conard, K. M. Yin, A. Delabie, J. Swerts, T. Schram, S. De Gendt, and S. Biesemans, "Achieving conduction band-edge effective work functions by La<sub>2</sub>O<sub>3</sub> capping of hafnium silicates," *IEEE Electron Device Lett.*, vol. 28, no. 8, pp. 486-488, Jun. 2007.
- [56] H.-C. Wen, S. C. Song, C. S. Park, C. Burhamn, G. Bersuker, O. Sharia, A. Demkov, B. S. Ju, M. A. Quevedo-Lopez, H. Niimi, K. Choi, H. B. Park, P. S. Lysaght, P. Majhi, B. H. Lee, and R. Jammy, "Highly manufacturable MoAlN PMOS electrode for 32 nm low standby power applications," in VLSI Symp. Tech. Dig., 2007, pp. 160-161.
- [57] Y. Yamamoto, K. Kita, K. Kyuno, and A. Toriumi, "Study of La concentration dependent VFB shift in metal/HfLaO<sub>x</sub>/Si capacitors," in Proc. Ext. Abs. of SSDM, 2006, pp. 212-213.
- [58] C. S. Park, P. Lysaght, M. M. Hussain, J. Huang, G. Bersuker, P. Majhi, P. D. Kirsch, H. H. Tseng, and R. Jammy, "Advanced High-k/Metal Gate Stack Progress and Challenges - A Materials and Process Integration Perspective," accepted to be published in *International Journal of Materials Research*, 2010
- [59] P. Sivasubramani, T. S. Böske, J. Huang, C. D. Young, P. D. Kirsch, S. A. Krishnan, M. A. Quevedo-Lopez, S. Govindarajan, B. S. Ju, H. R. Harris, D. J. Lichtenwalner, J. S. Jur, A. I. Kingon, J. Kim, B. E. Gnade, R. M. Wallace, G. Bersuker, B. H. Lee, and R. Jammy, "Dipole moment model explaining nFET V<sub>t</sub> tuning utilizing La, Sc, Er, and Sr doped HfSiON dielectrics," in VLSI Symp. Tech. Dig., 2007, pp. 68-69.
- [60] O. Sharia, A. A. Demkov, G. Bersuker, B. H. Lee, "Theoretical study of the insulator/insulator interface: Band alignment at the SiO<sub>2</sub> /HfO<sub>2</sub> junction," *Phys. Rev. B*, v. 75, p. 035306, 2007.
- [61] B. H. Lee, J. Oh, H. H. Tseng, R. Jammy and H. Huff, "Gate stack technology for nanoscale devices," *Materials Today*, Vol. No. 9, p. 36, 2006.
- [62] K. Choi, T. Lee, S. Kweon, C.D. Young, H. Harris, R. Choi, S.C. Song, B.H. Lee, and R. Jammy, "Impact of the bottom interfacial layer on the threshold voltage and device reliability of fluorine incorporated pMOSFETs," in Proc. IEEE IRPS, 2007, p. 374.





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The evolution of solid-state circuit technology has a long history within a relatively short period of time. This technology has led to the modern information society that connects us and tools, a large market, and many types of products and applications. The solid-state circuit technology continuously evolves via breakthroughs and improvements every year. This book is devoted to review and present novel approaches for some of the main issues involved in this exciting and vigorous technology. The book is composed of 22 chapters, written by authors coming from 30 different institutions located in 12 different countries throughout the Americas, Asia and Europe. Thus, reflecting the wide international contribution to the book. The broad range of subjects presented in the book offers a general overview of the main issues in modern solid-state circuit technology. Furthermore, the book offers an in depth analysis on specific subjects for specialists. We believe the book is of great scientific and educational value for many readers. I am profoundly indebted to the support provided by all of those involved in the work. First and foremost I would like to acknowledge and thank the authors who worked hard and generously agreed to share their results and knowledge. Second I would like to express my gratitude to the InTech team that invited me to edit the book and give me their full support and a fruitful experience while working together to combine this book.

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