Chapter 1

Design Concepts of Low-Noise Amplifier for Radio Frequency Receivers

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Additional information is available at the end of the chapter

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Abstract

The development of high-performance radio frequency (RF) transceivers or multi-standard/reconfigurable receivers requires an innovative RF front-end design to ensure the best from a good technology. In general, the performance of front-end and/or building blocks can be improved only by an increase in the supply voltage, width of the transistors or an additional stage at the output of a circuit. This leads to increase the design issues like circuit size and the power consumption. Presently, the wireless market and the need to develop efficient portable electronic systems have pushed the industry to the production of circuit designs with low-voltage power supply. The objective of this work is to introduce an innovative single-stage design structure of low noise amplifier (LNA) to achieve higher performance under low operating voltage. TSMC 0.18 micron CMOS technology scale is utilized for realizing LNA designs and the simulation process is carried out with a supply voltage of 1.8 V. The LNA performance measures are analyzed by using an Intel Core2 duo CPU E7400@2.80GHz processor with Agilent's Advanced Design System (ADS) 2009 version software.

Keywords: CMOS, RF circuits, VLSI design

1. Introduction

Today, there is an increased market demand for portable wireless communication devices and high-speed computing devices. This is true because low cost and high integration have resulted in the commercial success in wireless communication integrated circuits. But these devices are operated by batteries which have only a limited lifetime. The battery technology has not improved on par with electronics technology. As the developments in battery technology have failed to keep up with an increasing current consumption in wireless communication

devices, innovative circuit design techniques are required in order to reduce the power consumption and to utilize the low voltage. Radio frequency ICs are the basic building blocks of portable wireless communication systems. The use of a manufacturing technology for implementing and integrating these circuits is very important. The decision is based mainly on cost and integration levels. In the radio frequency circuit design, the technologies such as GaAs (Gallium Arsenide), SiGe (Silicon Germanium), and BiCMOS (Bipolar CMOS) provide good performance in high-frequency characteristics. But these processes lead to an increase in cost and process complexity [1]. In recent years, CMOS technology has been used as it is the best for implementation of low cost and high integration level systems on the chip.

Another aspect for the realization of analog circuits in CMOS technology is the possibility of reduction in supply voltage with each technology generation. The development of low-voltage analog RF circuits is means economy. At the same time, the existing circuit topologies cannot conform to the required high-performance wireless specifications under low-voltage operation. Hence, it is of a great need to introduce new design evaluations of wireless direct conversion receiver front-end circuits that can successfully handle low-supply voltages. The choice of receiver architecture, circuit topology design, and systematic optimization of the front-end blocks is always important. The choice of the receiver architecture, fundamental receiver front-end parameters needed in RF circuit design, the significance of CMOS technology, and MOS transistors high-frequency characteristics are discussed briefly. IEEE 802.11b/g wireless standards and its front-end specifications are the main target applications for the designs evaluated and are then presented.

2. Review of receiver architectures

The purpose of the receiver in wireless communication system is to perform certain operations required for the received signal such as amplification, frequency translation, and analog-to-digital conversion with adequate signal-to-noise ratio before subjected to digital signal processing. The performance of a receiver is analyzed by the ability to receive the strong or weak signal in the presence of strong interferences. The performance measures are expressed in terms of sensitivity, selectivity, fidelity, and dynamic range. The selection of receiver architecture is based on performance, cost, and power dissipation. The integration level along with the number of off-chip components determines the cost of the receiver. The existing receiver topologies in RF transceivers are Zero-IF, Heterodyne, Low-IF, and Wide-band IF. The description of these receiver architectures is briefly given in this thesis.

2.1. Direct conversion receiver

A direct conversion receiver (DCR) is also named as homodyne, synchrodyne, or zero-IF receiver. It was developed in 1932 by a team of British scientists. This receiver provides the most natural solution to detect information transmitted by a carrier in just a single conversion stage. The simplified block diagram of a typical direct conversion receiver is shown in **Figure 1**.

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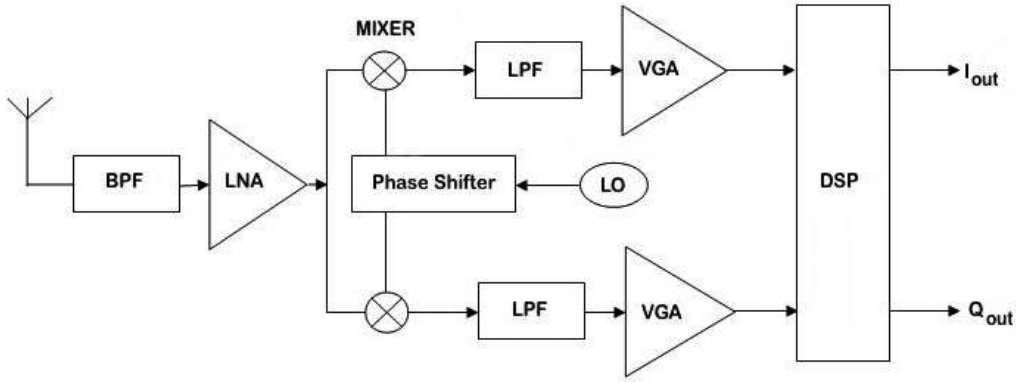

Figure 1. Direct conversion receiver.

A synchrodyne receiver is a radio receiver that demodulates the incoming radio signal using a synchronous detection driven by a local oscillator. The signal conversion (RF to IF) to baseband is done in a single-frequency conversion. The RF signal from the antenna is pre-filtered by a bandpass filter (BPF) to suppress the signals out of the reception band. The signal is amplified at the low-noise amplifier (LNA) stage and down-converted into zero intermediate frequency (IF) by the mixer stage. The resulting IF signal frequency is the difference between the RF and local oscillator signal frequencies. In the case of the phase and frequency-modulated signals, the down-conversion process should be performed in quadrature to prevent signal sidebands from aliasing on one another. As the local oscillator is centered in the desired channel, it requires signal and noise to occupy both the upper and lower sidebands. The down-conversion architecture produces an image at zero-IF frequency, and thus no image filter is required.

The important characteristic of the direct-conversion receiver is that amplification and filtering are mostly performed at the baseband rather than at the RF. The required signal is selected with the help of a low-pass-type baseband filter (BBF). The low-pass filter with a bandwidth of a half of the symbol rate removes the adjoining channels at baseband. As the filtering is performed at low frequencies, filters can be realized in on-chip without using external high-Q components. Most of the signal processing action takes place at low frequencies, thereby minimizing power consumption. The DCR eliminates the image rejection problem existing in other radio architectures [2]. However, an inadequate amplitude and phase balance between in-phase and quadrature-phase signals can increase the bit-error rate [3, 4]. It has its own disadvantages such as a highly sensitive to flicker noise and DC offsets. These problems can be eliminated in the wideband system design by making use of high-pass filters. The DCR avoids the complexity of the superheterodyne's two or more frequency conversions, IF stages, and image rejection issues. Recent research works proved that the zero-IF is always popular and is widely used for RF applications due to its simplicity, fewer off-chip components, and minimized power. Most of the receivers use the same RF front-end which includes LNA, mixer, and an oscillator. As per the constructional and performance point of view, direct conversion receivers are more suitable to satisfy the following constraints such as simplicity,

integration level, less off-chip components, and power dissipation. The described front-end circuits are all targeted for direct conversion receivers.

CMOS is always cheap in processing cost and one of the best technologies for the implementation of analog design without any adaptations. Further, it can provide better integration of digital circuitry with high-performance analog circuits. Also, it provides the possibility of complete system on-chip, entire analog front-end, and the digital demodulator implemented on the same die. CMOS technology has the capability to operate at a lower supply voltage than the BiCMOS technology. This is due to the fact that each transistor has a typical switch on voltage of 0.7–0.8 V, and thus the minimum supply voltage required for BJT circuits is about 2–3 V. But modern CMOS processes provide many different threshold voltages (V_t) such as high, moderate, and low standards. For instance, MOS transistors with a lower threshold can be utilized in analog or digital circuits, where speed is important.

On the other hand, devices with a higher threshold are useful when the low-power consumption of the digital circuits is affected by leakage currents. This feature enables the circuitry design under low operating voltage even when technology is scaled down toward deep submicron CMOS processes.

Technology scaling is the primary factor in achieving high-performance circuit designs and systems. Each reduction in CMOS technology scaling has a reduced gate delay, doubled the device density, and a reduced energy per transition. To achieve this, each transistor width, length, and oxide dimensions are also scaled by 30%. Taiwan Semiconductor Manufacturing Company (TSMC) is the world's largest dedicated semiconductor foundry, providing the industry's leading process technology. TSMC 0.18 micron CMOS logic process is widely used for various electronic systems such as microprocessors, microcontrollers, and high-speed processors. It provides the device models under the operating voltage of 1.8 V. Therefore, this technology scale is utilized for realizing front-end designs. TSMC 0.18-μm RF CMOS models used in this research work are shown in **Figure 2**. The simplified device specifications are given in **Table 1**. The benefits and drawbacks of silicon technologies are highlighted in this section. The availability of accurate simulation models, high-frequency models, and noise models of devices are essential for accurately predicting the performance of RF circuits.

2.2. Overview of wireless standards

Currently, wireless applications in 2.4/5 GHz frequency range are receiving greater attention because it is relatively economical and its potential for system on-chip integration. IEEE 802.11a/b/g is a set of promising standard in the market of portable/wireless communication devices such as cellular phones, WLANs, RFID, global positioning systems, etc. In the 5-GHz frequency range, the IEEE 802.11a standard is purely based on orthogonal frequency division multiplexing (OFDM) modulation technology, and it is compatible with data rates up to 54 Mbps. It provides nearly four to five times the data rate and has 10 times the overall system capacity as currently available in IEEE 802.11b wireless systems [5, 6].

The IEEE 802.11b/g operates in the 2.4–2.5 GHz ISM band, which use the direct sequence, spread spectrum signaling (DSSS) with a maximum data rate of 11Mbps, and occupies the

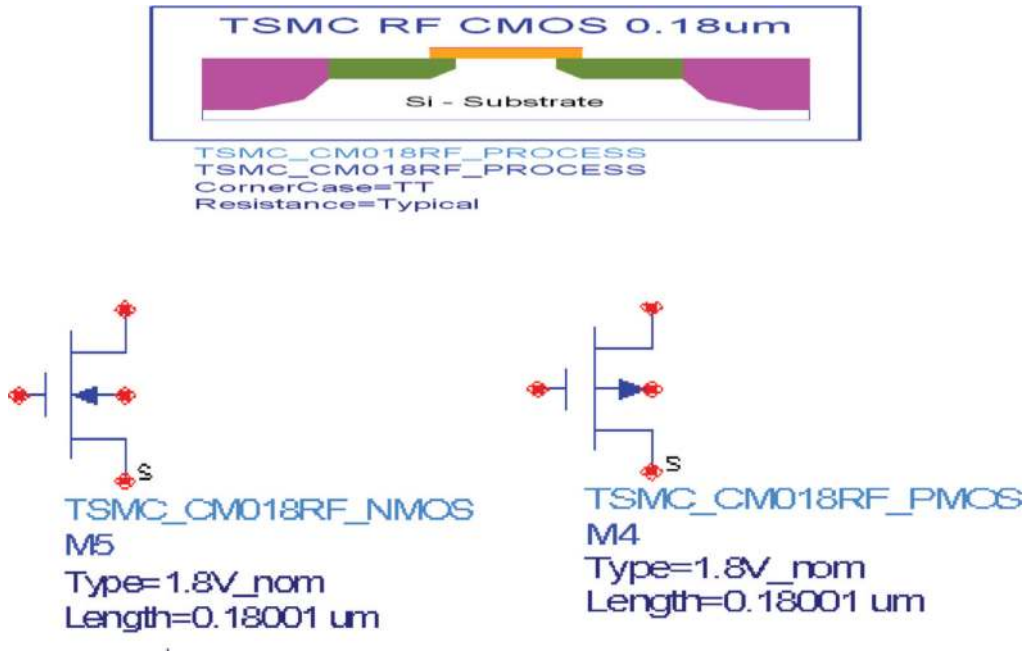

Figure 2. TSMC 0.18-μm RF CMOS models.

Blocks	Gain	Noise figure	IIP3
LNA	16 dB	3 dB	−5 dBm
MIXER	10 dB	4 nV/√Hz	10 dBm

Table 1. IEEE 802.11b/g DCR front-end specifications.

same frequency spectrum with a data rate of 54 Mbps with orthogonal frequency division multiplexing (OFDM) modulation methods, respectively. The proposed work is mainly highlighted to meet the direct conversion specification of IEEE 802.11b/g applications as shown in **Table 1**.

2.3. Research issues

Recently, reported designs are based on inductively degenerated cascode LNAs which do not satisfy an optimum gain, a lowest NF, and a better impedance matching. The evaluation of an active mixer with moderate linearity is one of the challenges in low-voltage design and has become an important issue in most analog IC applications. Gilbert mixer is the commonly used double-balanced, active mixer configuration. A better performance can be achieved using this structure. But this needs increase in the current through the transconductance stage and switching stage, and therefore a higher supply voltage will be required. It has a stacked structure which limits its use in low-voltage applications. In general, two types of oscillators namely LC tank and ring oscillators are often used to generate a local frequency. In GHz frequency applications, ring topology is usually preferred because of its improved noise

performance and lower-power consumption. It avoids the use of spiral inductors which are employed in LC tank oscillators. But these oscillators need to be realized by using digitally controlled logics with efficient delay elements for a high-frequency generation.

Reported LC oscillator designs provided changes only to the elements in tuned circuitry and analyzed the performance. It is clearly understood that the performance of front-end blocks can be improved either by increasing the supply voltage or by providing additional stages at the output. The abovementioned problem motivated to introduce an innovative single-stage design of front-end blocks under low operating voltage for 2.4 GHz/5GHz wireless applications. The simplified block diagram of a direct conversion receiver (DCR) front-end used in this research work is shown in **Figure 3**. It represents the process of incoming 2.4 GHz RF signal frequency (f_{RF}) by the LNA and down-converted into 150-MHz intermediate frequency (f_{IF}) by the mixer. The first stage of a receiver front-end is typically a low-noise amplifier (LNA) whose main function is to provide sufficient gain in order to overcome the noise of next stages. The receiver's sensitivity mainly depends upon the LNA noise figure and gain. A down-conversion mixer is always followed by the RF low-noise amplifier. It is one of the most important parts and used to translate one frequency into another. It changes the RF signal into an IF output signal. Intermediate frequency (IF) is the difference between RF and LO signal frequencies.

Mixer plays an important role in improving the overall system linearity. Oscillator is a signal generation circuit where tuned and amplifier blocks only decide the required frequency of oscillation. The digital revolution and higher growth of portable wireless devices market require many changes to the analog front-ends. It also requires new architectures, techniques, and high integration level. The CMOS design is chosen in this research because it can provide an attractive solution for RF analog circuits in terms of cost and integration level. The technology scaling in CMOS has increased the cutoff frequency of transistors and allows the improved performance of analog circuits. This chapter describes the importance of front-end blocks along with the necessity of low-voltage design and then discusses the known techniques and structures for the performance of front-end circuits. As can be seen from **Figure 4**, front-end is

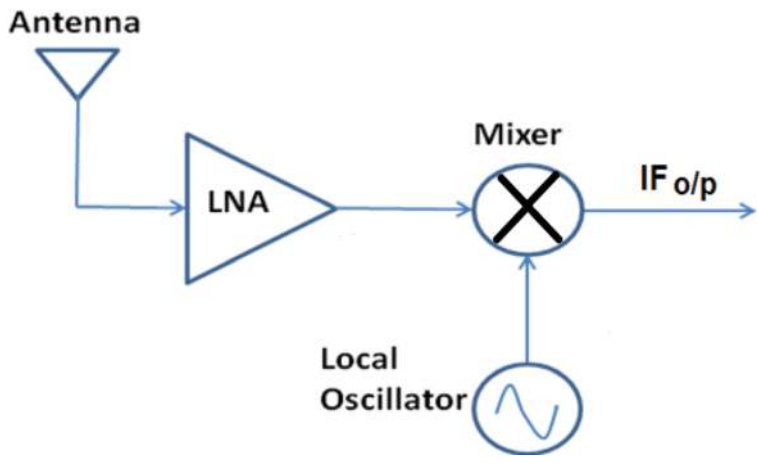

Figure 3. Block diagram of DCR front-end.

an interface between the antenna and the digital signal-processing unit of the wireless receiver. Basically, front-ends are responsible for tracking weak signal (RF) at a high frequency and translating into IF signal for transmitting with high power levels. It needs high-performance analog circuits like RF amplifier (LNA), mixer, and an oscillator. Recently, the wireless market and the need to develop efficient portable electronic systems have pushed the industry to the production of circuit designs with a low-voltage power supply. In the past years, low-power consumption usually was less considered among key design specifications. But today, both increased device/circuit density of current CMOS technology and battery-operated portable systems necessitate low-voltage, low-power system/circuit design [7–9].

Figure 5 represents the channel length and supply voltage variation in deep sub-micron CMOS technologies [6]. It is observed that CMOS technology leads to smaller and smaller channel lengths, and the performance of RF communication circuit design will continue to improve with the reduction of supply voltage. One common technique for reducing power in analog or digital circuits is to reduce the supply voltage. In this research, front-end designs are evaluated under the supply voltage of 1.8 V. The constraint toward the low-voltage design is the

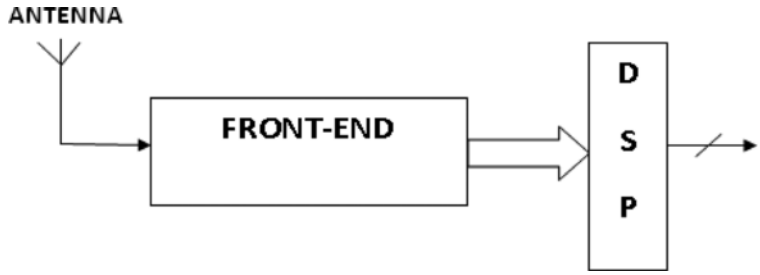

Figure 4. Front-end in wireless receiver.

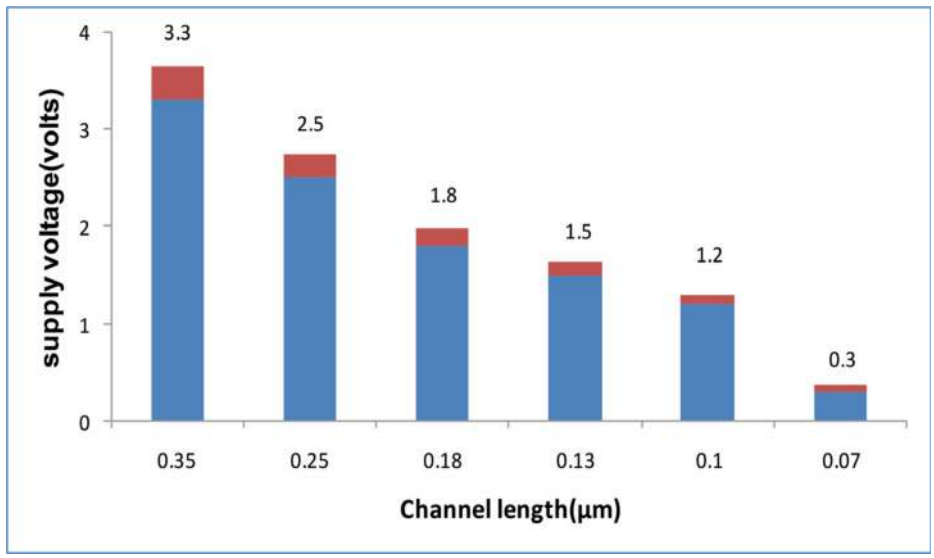

Figure 5. CMOS voltage scaling.

threshold voltage and drain-source saturation voltage which do not scale down at an exact rate as the supply voltage or do not scale under a low-supply voltage. It is a problem as well as a challenge to face for analog designer due to the limited voltage headroom. Some circuit designs can only operate under a higher supply voltage with desirable properties and lose their high performance in a low-voltage environment. Therefore, alternative circuit structures or even system topologies need to be investigated. In modern CMOS processes, critical analog and RF circuits can be implemented with dual-gate, multi-threshold, and thick-oxide MOSFETs, which tolerate higher supply voltages, but this solution increases the cost, since additional processing masks are required [10–15]. The development of low-voltage CMOS analog and RF front-end circuits is essential and economically advantageous.

2.4. Low-noise amplifier design

A low-noise amplifier is the first stage of the receiver front-end and it is used to increase the signal power coming from the antenna while introducing less noise by the same LNA. **Figure 6** shows the block diagram of LNA. In general, the LNA structure is composed of impedance matching block for input/output section (IMN, OMN) and amplification block (AMP). Matching networks account for performing part of filtering, optimum noise performance, and provides stability at the input as well as output. The matching elements are passive, consisting of strip lines, inductors, capacitors, and resistors. R_S and R_L represent the source and load impedances, respectively.

The cascode structure is popularly used in LNA for narrow-band wireless applications. It is a two-stage amplifier consisting of common source and common gate (CS-CG) stages. The following are the basic characteristics of a cascode amplifier such as a higher input-output isolation, a higher input/output impedance, and a higher gain with bandwidth. **Figure 7** represents the simplified cascode structure. It is a combination of an amplifying device (CS transistor- M_1) with a load device (CG transistor- M_2).

CS transistor M_1 is considered as input stage driven by a signal source V_{in}. It is also used to drive a CG transistor M_2 as output stage, with output signal V_{out}. L_g and L_s are the gate, source inductors of M_1, respectively, responsible for impedance matching. L_d is the drain inductor of M_2, responsible for output impedance matching. The importance of CS and CG stages has been highlighted by design equations and is given subsequently.

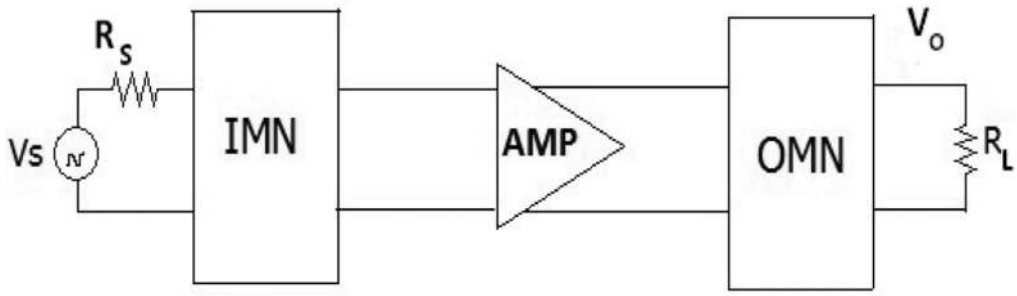

Figure 6. Block diagram of LNA.

2.4.1. Single-ended dual-CS low-noise amplifier (SDC LNA)

The amplification block (CS stage) of the cascode amplifier is revised in this research to achieve an optimized performance in single-ended and differential topologies using ADS software. These LNAs are titled as SDC and DDC LNA. The amplification block is altered by dual nMOS transistors at the CS stage. The purpose of this structure is to eliminate the use of an additional stage at the output for further amplification. It does not occupy much area in implementation and reduce the design complexity than two-stage LNA designs. **Figure 8** represents the dual CS stage of LNA. An inter-stage inductor is added in between the CS and CG stages for improving the impedance matching. **Figure 9** represents the schematic of SDC LNA architecture. It comprises input stage inductor L_g, inter-stage inductor L_{IS}, dual CS transistors M1 - M2, single CG transistor M3, and output impedance matching inductor L_d. The bias current is chosen to provide the optimum overdrive voltage for dual CS transistors using transistor M4 and resistor R, C_{in} and C_o are blocking capacitors used to block DC signal and allow only AC signal.

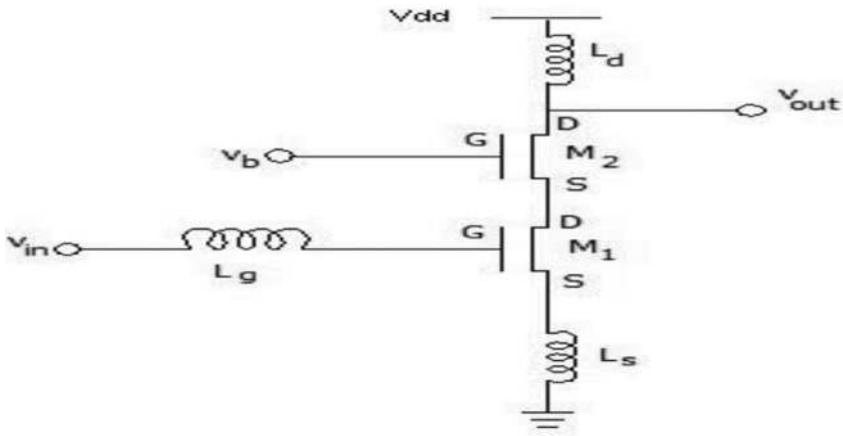

Figure 7. Cascode structure.

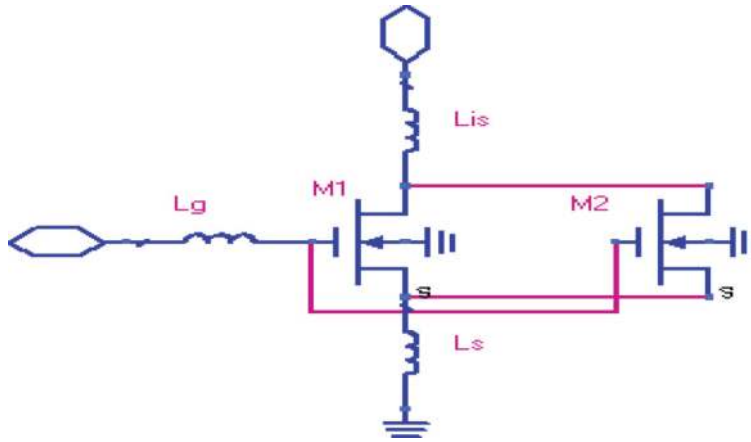

Figure 8. Structure of dual CS stage.

From the schematics, an equivalent model of input stage is developed for determining the simplified theoretical expressions of input impedance and output impedance of the dual CS stage and it is shown in **Figure 10**. The gate-source capacitances and drain-source currents are paralleled in this model. C_{gs1}, C_{gs2}, and $G_{m1,2}$ V_{gs} represent the gate-to-source capacitances of nMOS transistors M1, M2 and drain-source currents of both transistors. $G_{m1,2}$ is the sum of transconductances g_{m1} and g_{m2}. The input impedance of the MOSFET's without feedback is usually capacitive due to the gate-source capacitance. In order to get the resistive input impedance, an inductive feedback (L_s) is added to the source.

The input impedance seen at the gate of M1 and M2 is expressed in Eq. (1). At resonance, inductive and capacitive impedances are canceled out, and hence the input impedance becomes purely resistive.

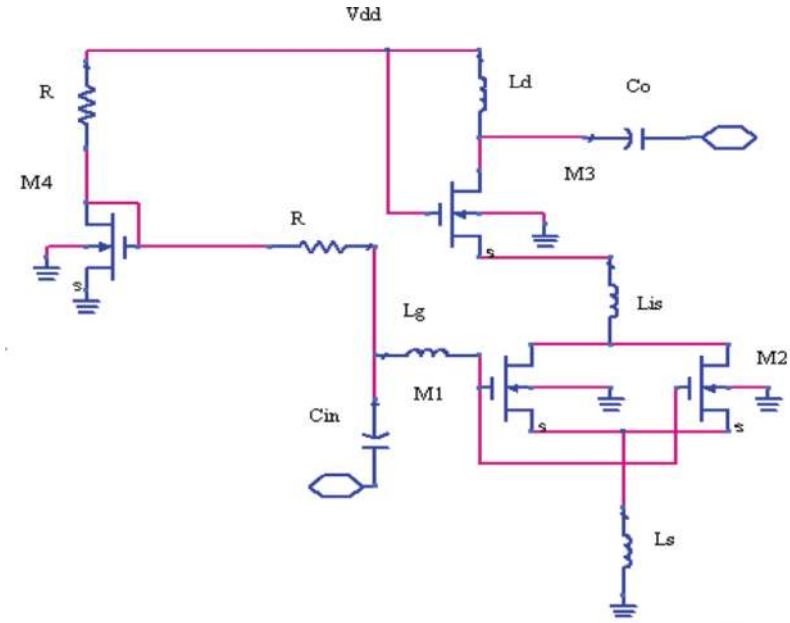

Figure 9. Schematic of SDC LNA.

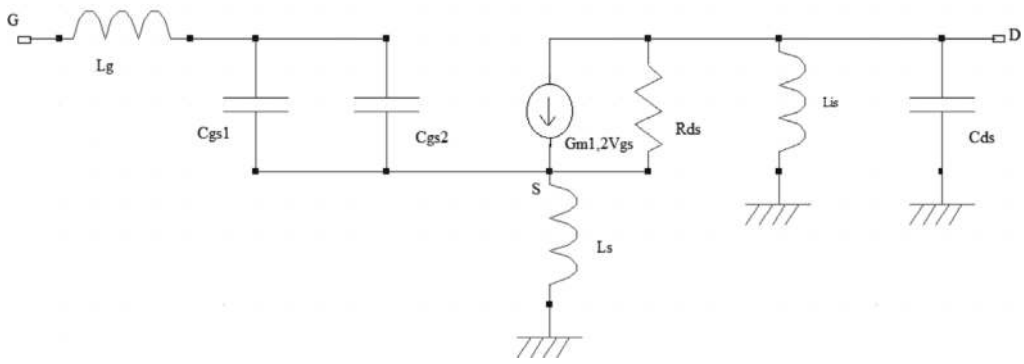

Figure 10. Equivalent model of input stage.

$$Z_{in} = \frac{L_s(g_{m1} + g_{m2})}{C_{gs1} + C_{gs2}} = \omega_T L_s \tag{1}$$

The required gate inductor (L_g) and source inductor (L_s) cancel out the imaginary part of the input impedance at 9 and 1 nH, respectively. The optimum quality factor (Q) for the best NF is about 8, with a corresponding F_{min} of 1.77 dB. An inter-stage matching inductor of 3 nH is placed in between the dual CS and CG stages.

The output impedance of the common source stage with inter-stage matching inductor is derived by using Eq. (2)

$$Z_{out} = SL_{is} + \frac{1}{S(C_{ds1} + C_{ds2})} + \frac{(g_{m1} + g_{m2})L_s}{(C_{ds1} + C_{ds2})} \tag{2}$$

where C_{ds1}, C_{ds2} are the drain-to-source capacitances of the transistors M1, M2. In the design of RF front-end, the mixer directly follows the LNA. Hence, the output impedance matching of LNA is not an issue. If the LNA output load is either an external filter or there is a need to measure the performance of the LNA alone, then the output of the LNA needs to be matched with certain impedance.

The selection of the cascode topology simplified the analysis by neglecting the gate-drain capacitance. The on-chip spiral inductor L_d and output capacitor C_o with values of 15 nH and 0.5 pF are used for output matching. The LNA circuit is designed by minimizing the noise figure for a gain constraint of 20 dB and an input and output matching constraints of −10 dB at 2.4 GHz. The width of the transistors in dual CS stage is assumed to be equal in the design analysis. The W/L ratio of cascode transistor (M3) is the same as that of a common source stage. The bias transistors width and current are arbitrarily selected as one-tenth of that of the CS transistor. With the help of operating frequency (ω_o) and the gate-to-source capacitance, the optimized width of the transistors can be computed at a particular frequency of interest. The optimized LNA performance is achieved by the transistor width values of 70–100 μm. The LNA performance is evaluated for radio frequencies of 2.4 and 5 GHz, respectively. The design analysis with suitable formulae has been expressed in the next section.

2.4.2. Differential dual CS low-noise amplifier (DDC LNA)

A differential topology approach is usually preferred in RF design due to its well-known characteristics of immunity to common mode disturbances, rejection to parasitic couplings, and an increased dynamic range. It produces a differential output which is more flexible for feeding signal information to the second stage of front-end. Here, the LNA is evaluated in differential topology, and its novel design is given in detail. **Figure 11** shows the schematic of DDC CMOS LNA. Each common source (CS) stage of cascode structure is built by two parallel transistors instead of one, and called as dual CS stage. It comprises an input stage formed by inductors L_g and L_s, two inter-stage inductors (L_{is}), four common source transistors (M1, 2 - M3, 4), and two common gate transistors (M5-M6). Two drain inductors L_D are used for output impedance matching. This structure is suitable for multiple demands of LNA such as gain,

noise figure, and linearity. The equivalent circuit of the single cascode stage is shown in **Figure 12**, where the transistors M1, M2 are replaced by gate-source capacitances (C_{gs1}, C_{gs2}), channel currents ($g_{m1}V_{gs1}$, $g_{m2}V_{gs2}$), and gate-drain capacitances (C_{gd1}, C_{gd2}). r_{o1} and r_{o2} are the output resistances of two nMOS transistors M1, M2, respectively.

The cascoding transistors (M5, M6) reduce the interaction of the tuned output with the tuned input and nullify the effect of gate-drain capacitances of dual-CS transistors. The simplified expressions of input and output impedance have already been dealt in the previous section.

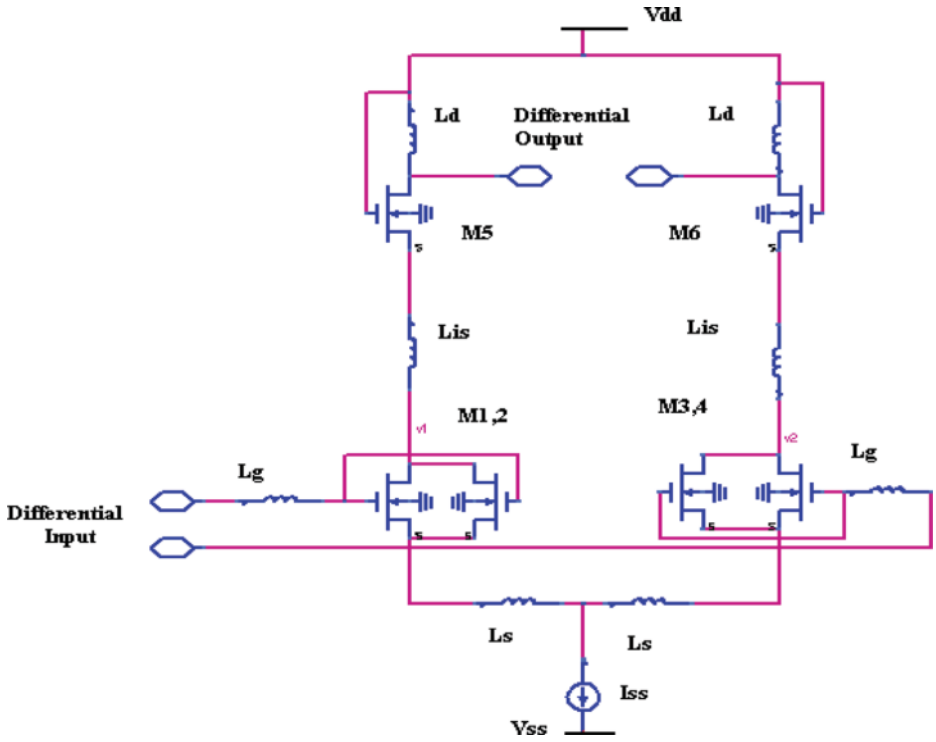

Figure 11. Schematic of DDC LNA.

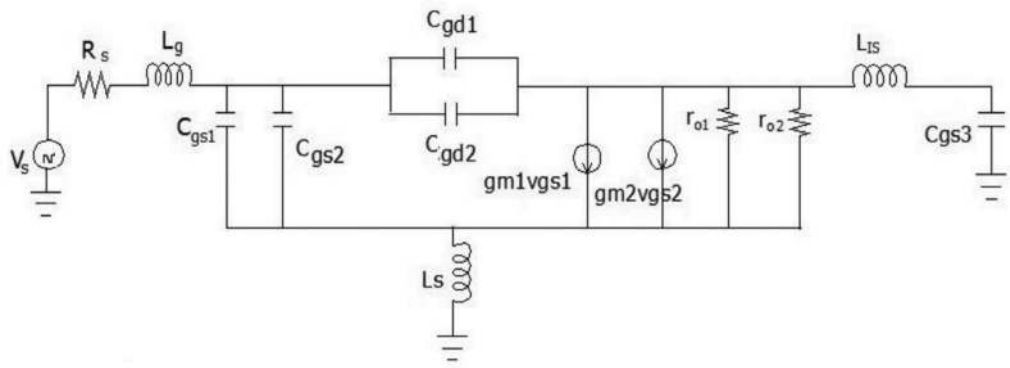

Figure 12. Equivalent circuit for input stage of DDC LNA.

The design increased the complexity in a differential structure. But the degree of design choice is satisfied with the multiple objectives such as gain, NF, and 1-dB gain compression point.

With reference to **Figure 10**, the theoretical expressions of performance factors are derived and highlighted. The total current flowing through the dual CS stage is represented by assuming that the transistors are operated in a saturation region, and it is shown in Eq. (3)

$$I_t = \frac{K}{L}\left[W_1\left(V_{gs1} - V_t\right)^2 + W_2\left(V_{gs2} - V_t\right)^2\right] \tag{3}$$

where K is the process-dependent term, L is the channel length, W_1 and W_2 are the gate widths of M1, M2, and V_{gs1}, V_{gs2}, V_t are the gate-source voltages and threshold voltage of transistors, respectively.

2.5. Design methodology

The structure of DDC LNA is a differential representation of two SDC LNAs. The design procedure is commonly described for SDC LNA and DDC LNA. Inductors and transistors are the basic building elements of LNA. Inductors are reactive and do not add noise into the circuit. The LC resonance always improves the gain and noise performance of LNA. The optimized width of the transistors and an inductance value of inductors are calculated by using appropriate design equations. The calculations are highlighted at design frequency (f_o) of 2.4 GHz with an essential feature of TSMC RF CMOS 0.18-μm technology scale. The design steps are elaborated through these design factors as follows:

1. gate inductance (L_g)
2. gate-source capacitance (C_{gs})
3. width of the transistor (W)

The center frequency

$$\omega = 2\pi f_o \tag{4}$$

where f_o is 2.4 GHz.

$$= 2\pi \times 2.4 \times 10^9 = 15.079 \times 10^9 \text{ rad/s.}$$

is calculated by using Eq. (4).

The value of gate inductor L_g is realized by means of Eq. (5). The Q of an inductor value is selected as 8, based on 0.18-μm CMOS scale characteristics. The source impedance is assumed to be 50 Ω

$$\begin{aligned} L_g &= \frac{Q_L R_s}{\omega_o} \\ &= \frac{(8 \times 50)}{15.079 \times 10^9} = 14.078\text{nH} \end{aligned} \tag{5}$$

It is observed in simulation, whenever the L_g value is reduced below 8 nH, the design frequency is shifted between 2 and 3 GHz and becomes very difficult to achieve the narrowband

performance. At high frequencies, the careful design impact only reduces the component variations against the performance of LNAs.

The gate-source capacitance (C_{gs}) is expressed in terms of RF frequency, shown in Eq. (6). L_s is assumed to be 0.5–1 nH

$$\begin{aligned} C_{gs} &= \frac{1}{4\pi^2 f_o^2 (L_g + L_s)} \\ &= \frac{1}{227.4 \times 10^{18} (14.078 \times 10^{-9} + 1 \times 10^{-9})} \\ &= 0.10050 \times 10^{-12} \\ C_{gs} &= 0.1\ pF \end{aligned} \tag{6}$$

From the technology-scale characteristics, the channel length (L) of 0.18 μm and oxide thickness (T_{ox}) of 4.1 × 10^{-9} m is observed. The permittivity of oxide is calculated by using this Eq. (7),

$$\varepsilon_{ox} = \varepsilon_o \varepsilon_s \tag{7}$$

where ε_0 is the dielectric constant of free space of 8.854 × 10^{-14} F/cm and εs the dielectric constant of silicon equal to 3.9. Therefore, the oxide capacitance or gate-oxide-specific capacitance is calculated by using Eq. (8)

$$\begin{aligned} C_{ox} &= \frac{\varepsilon_{ox}}{T_{ox}} \\ &= \frac{3.9 \times 8.85 \times 10^{-14}}{4.1 \times 10^{-9}} = 8.641 \times 10^{-8}\ \mathrm{F/mm^2} \end{aligned} \tag{8}$$

The optimized width of the transistors is calculated by substituting all the values in Eq. (9). The sizes of the transistors are assumed to be equal in dual CS stage

$$\begin{aligned} W &= \frac{3C_{gs}}{2C_{ox}L_{\min}} \\ W &= \frac{3 \times 0.1 \times 10^{-12}}{2 \times 8.64 \times 10^{-3} \times 0.18 \times 10^{-6}} \\ W &= 96.99\mathrm{mm} \end{aligned} \tag{9}$$

For DDC LNA, an additional design requirement is drain inductance of output stage inductors whose values are calculated by assuming C_{out} as 1 pF in Eq. (10). The inductance values of gate inductor L_d (10–15 nH) have been adjusted to vary the gain of the LNA

$$L_D = \frac{1}{4\pi^2 f_o^2 C_{out}} \tag{10}$$

The calculated values of components are used in the LNA design schematic with S-parameter test setup and simulated the performance of the designed circuit. With the transistor width of

97 μm, the DDC LNA achieved the optimum performance in terms of gain, NF, and impedance matching for this design. Both SDC and DDC LNA designs are also realized at a 5-GHz frequency by adopting the same procedure.

2.5.1. Performance metrics

The performance metrics namely gain and NF are derived commonly and used to analyze the circuit activity of the LNA design.

With reference to **Figure 12**, the overall dual CS stage transconductance can be expressed as

$$G_m = (g_{m1} + g_{m2})Q_{in} \tag{11}$$

where Q_{in} is the effective Q of the amplifier input circuit. The increase in quality factor Q does not reduce the device transconductance, and therefore the overall stage transconductance remains unchanged. In general, the gain of a circuit is characterized by effective transconductance and load impedance.

At resonance frequency, the gain of LNA is expressed in terms of device transconductances g_{m1} and g_{m2} in Eq. (12),

$$A_V = \frac{(g_{m1} + g_{m2})Q_L}{\omega_o C_{gs}} = \frac{g_m Q_L}{\omega_o C_{gs}} = \frac{\omega_T Q_L}{\omega_o} \tag{12}$$

where Q_L is the quality factor of the load element. The unity gain frequency is specified by, $\omega_T = \frac{g_m}{C_{gs}}$ and $g_m = g_{m1} + g_{m2}$. The device transconductance is evaluated in terms of unity gain frequency and gate-source capacitance.

The impact of Q on performance factors can be observed not only in theory but also in simulation. Using linearity test setup, the simulated value of gain saturation of SDC LNA is observed from the output 1-dB compression point of +6.16 dBm at 2.4 GHz RF frequency and with −2 dBm input referred value. **Figure 13** represents the equivalent noise model of the

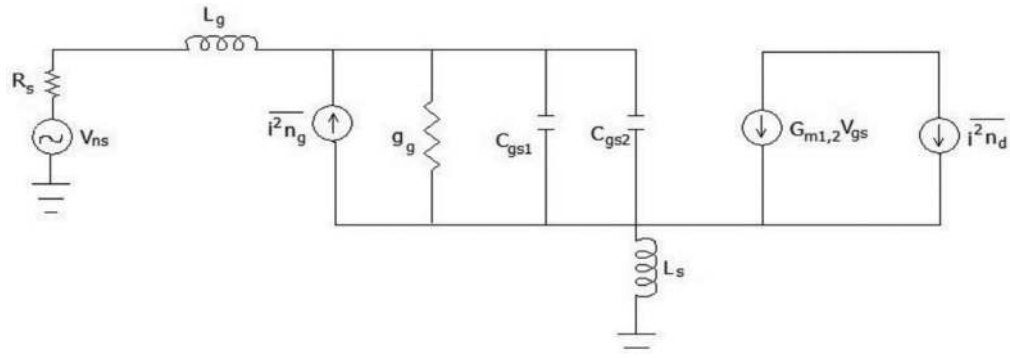

Figure 13. Equivalent noise model of input stage.

input stage of designed LNAs. The gate- and drain-induced noise current sources are shown with gate-source capacitances of the RF nMOS transistors.

The expressions for noise current densities have already been explained in previous sections. With reference to **Figure 13**, the noise factor is evaluated in terms of power spectral densities of drain noise current and gate noise current. It can be expressed as,

$$F = \frac{S_{Rs} + S_d + S_g}{S_{Rs}} \tag{13}$$

where S_{Rs} is the output noise power density due to the source impedance.

At series resonance condition, the output noise power density S_d due to the drain noise current can be written as

$$S_d = \frac{4kT\gamma g_{do}}{\left(1 + \frac{L_s}{R_s}\omega_T\right)^2} = \frac{4kT\gamma g_{do}}{\left(1 + \frac{g_m}{C_{gs}}\frac{L_s}{R_s}\right)^2} \tag{14}$$

where R_s is the source resistance and ω_T is the cutoff angular frequency.

In the same way, the output noise power density due to gate noise current, S_g, can be written as

$$S_g = \frac{4kT\gamma g_{do}}{\left(1 + \frac{L_s}{R_s}\frac{g_m}{C_{gs}}\right)^2}\frac{\delta\alpha^2}{5\gamma}\left(1 - \|c^2\|\right)\left(1 + Q^2\right) \tag{15}$$

where c is the correlation factor between the gate and the channel noise current sources. The quality factor Q is a function of the source resistance and the gate-source capacitance of the MOSFETs.

By substituting Eqs. (14) and (15) in Eq. (16), the noise factor F can be expressed as

$$F = 1 + \frac{2\gamma}{\sqrt{5}\alpha}\left(\frac{f_o}{f_T}\right) \tag{16}$$

where f_o and f_T are design frequency and unity-gain frequency, respectively, and γ, α are channel noise factors.

Continuous improvement in technology will definitely lead to improve the noise performance at frequency of interest. The LNA can be designed to get NF equal to a minimum noise factor of the transistor, but also the lowest NF can be enumerated with the given CMOS technology scale.

Further, the NF of the DDC LNA is simplified, and it is given in Eq. (17)

$$NF = 10\log_{10}\left(1 + 2.4\left(\frac{f_o}{f_T}\right)\right) \tag{17}$$

By using Eqs. (12) and (17), the theoretical gain and noise figure of DDC LNA are calculated and are validated through simulations.

2.5.2. Performance analysis

SDC and DDC LNAs are designed and its performance is analyzed at 2.4- and 5-GHz frequencies. The devices and its characteristics used in designs are based on TSMC 0.18-μm RF CMOS process. Agilent's Advanced Design System (ADS) electronic design automation (EDA) tools are used for performance analysis. The various parameters analyzed here are S parameters, NF, and linearity to describe LNA performance with a supply voltage of 1.8 V. Scattering parameter (SP) analysis is the most useful linear small signal analysis for LNA. It is test setup by specifying the input, output ports, and the range of sweep frequencies. It is used for the characterization of forward gain (S_{21}), input impedance matching (S_{11}), output impedance matching (S_{22}), and reverse gain (S_{12}).

The graphs of S_{11} and S_{21} are provided in dB scale for both LNAs. SDC and DDC LNA graph of S parameter analysis with respect to RF frequency lies between the ranges of 1.0–3.0 GHz which are shown in **Figures 14** and **15**. The value of the input impedance matching of SDC LNA can be obtained from **Figure 14**. The results are indicated by markers m1 and m2. Simulation result gives the input matching value as −10.99 dB which satisfies the requirement

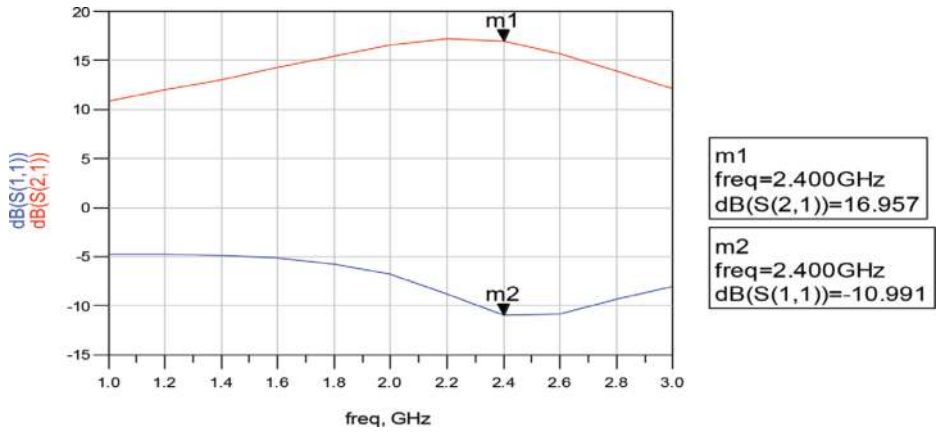

Figure 14. S-parameters of SDC LNA.

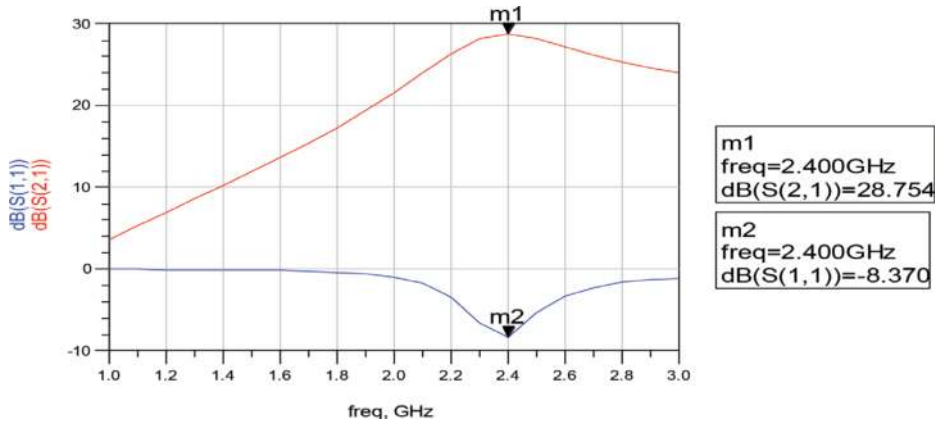

Figure 15. S-parameters of DDC LNA.

of matching constraint of LNA that is $S_{11} < -10$ dB at 2.4 GHz. The value of forward gain S_{21} is reached as 16.957 dB. Normally, the requirement of gain at 2.4 GHz is in the range of 15–30 dB. LNA satisfies the gain constraint but still the value is less. Moreover, it needs balun circuit additionally to process its output to the mixer as in the case of front-end design analysis. The graphs of S_{12}, S_{22} are not mentioned to avoid overlapping but traced during simulation.

To suppress the noise of the succeeding stages of front-end, the gain of LNA should be high. If the gain is too small, LNA cannot amplify the incoming weak signal to a desired value. If the gain is too large, LNA cannot degrade the linearity of the following mixer. It is one of the most important performance factors of LNA design. Therefore, DDC LNA satisfies the highest gain constraint at 2.4 GHz with optimized matching, and its performance is better than that of SDC LNA which is observed from results of **Figure 15**. The gain of DDC LNA is 28.75 dB. It is possible to feed the signal into the mixer directly due to its differential structure.

2.5.3. Noise figure

Noise figure is defined as the ratio of the total input noise to the total output noise due to the source. In general, the noise figure of LNA should remain below 5 dB to prevent inducing

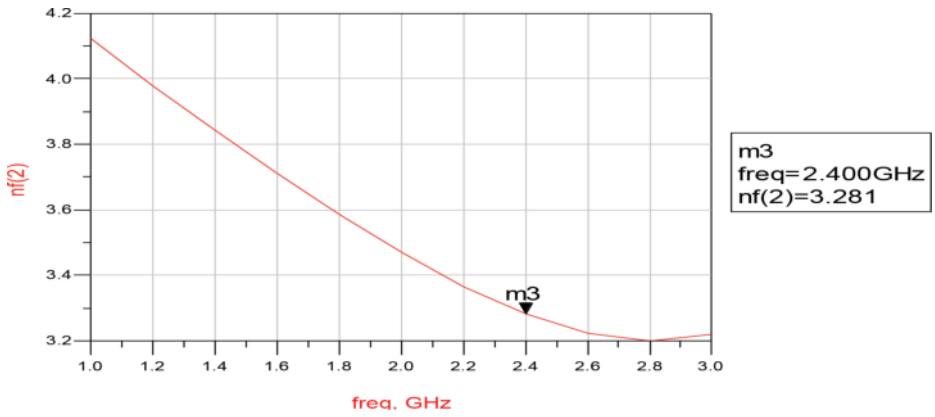

Figure 16. NF of SDC LNA.

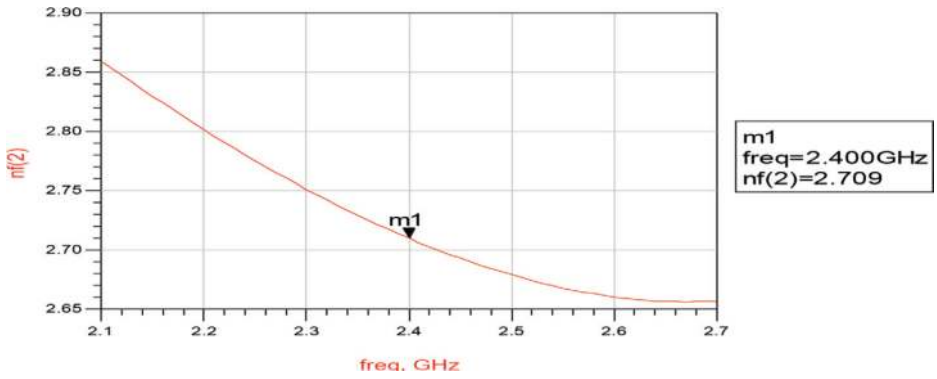

Figure 17. NF of DDC LNA.

noise problems in other stages of the receiver, like mixer, IF amplifier, etc. The NF graphs of the proposed LNA designs are given in **Figures 16** and **17**. The values of NF for SDC and DDC LNA are 3.281 and 2.7 dB, respectively. These values are highly desirable in wireless receiver. Typically, an NF of less than 4 dB is required in most standard CMOS LNAs. Both designs produce better NF and satisfy the noise reduction constraint. By making use of a single-stage structure, both SDC and DDC LNA designs satisfied the objectives of LNA. Simulation results show that DDC LNA structure presented here achieve better performances in what concerns S21, NF, and impedance matching at 2.4-GHz frequency. This analysis has also proved that DDC LNA achieved comparably good performance than other LNAs. This performance study helped us to select proper LNA architecture for front-end design.

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