# Low-C ESD Protection Design in CMOS Technology

*Chun-Yu Lin*

## Abstract

Electrostatic discharge (ESD) protection design is needed for integrated circuits in CMOS technology. The choice for ESD protection devices in the CMOS technology includes diode, MOSFET, and silicon controlled rectifier (SCR). These ESD protection devices cause signal losses at high-frequency input/output (I/O) pads due to the parasitic capacitance. To minimize the impacts from ESD protection circuit on high-frequency performances, ESD protection circuit at I/O pads must be carefully designed. A review on ESD protection designs with low parasitic capacitance for high-frequency applications in CMOS technology is presented in this chapter. With the reduced parasitic capacitance, ESD protection circuit can be easily combined or co-designed with high-frequency circuits. As the operating frequencies of high-frequency circuits increase, on-chip ESD protection designs for high-frequency applications will continuously be an important design task.

**Keywords:** CMOS, ESD protection, high frequency, high speed, low capacitance

## 1. Introduction

The integrated circuits (ICs) operated at higher frequency are needed. For example, the transceivers operated in gigahertz (GHz) bands are the good candidate for the demand of faster data transmission [1]. CMOS technology is a promising way to implement the GHz integrated circuits with the advantages of high integration capability and low cost for mass production [2, 3]. However, the transistors in CMOS and even FinFET technologies are inherently susceptible to the electrostatic discharge (ESD) events [4, 5]. Once any transistor is damaged by ESD, it cannot be recovered, and the IC functionality will be lost. Therefore, the ESD protection design must be equipped on the chip. Nevertheless, the ESD protection devices cause the IC performance degradation. The ICs operated in GHz frequencies are very sensitive to the parasitic capacitance [6, 7]. To mitigate the performance degradation caused by ESD protection device, the low-capacitance (low-C) ESD protection designs are needed [8, 9].

## 2. ESD protection requirement

To adequately protect the ICs, the ESD protection circuit must shunt ESD current with limited voltage drop [10–12]. **Figure 1** shows the ESD design window of an IC, which is defined by the power-supply voltage ($V_{DD}$ and $V_{SS}$) and the
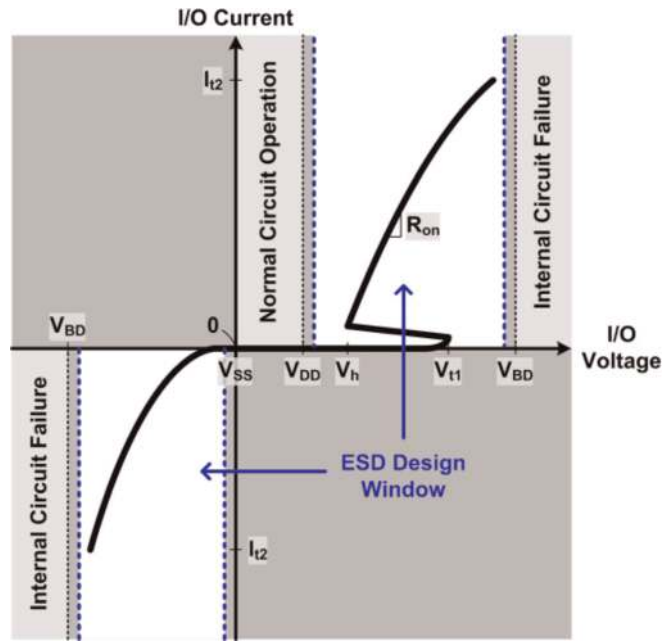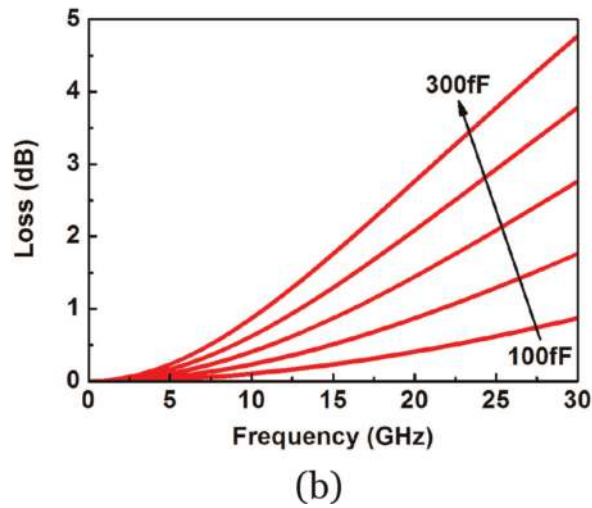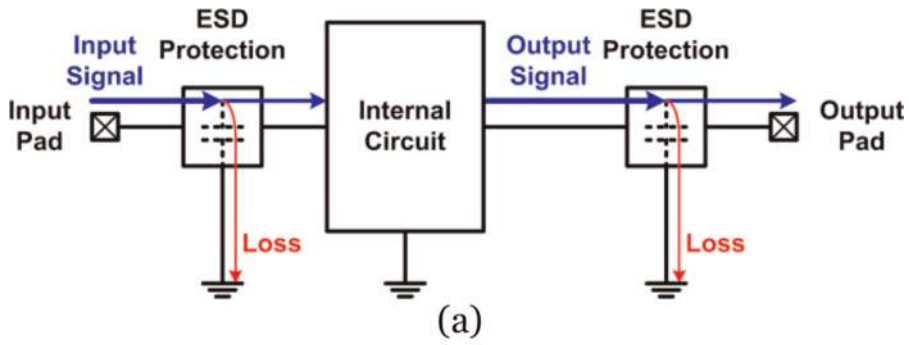
**Figure 1.**
*ESD design window.*



**Figure 2.**
*(a) Parasitic capacitances seen at I/O pads cause signal loss to ground and (b) Simulated loss of parasitic capacitances.*

breakdown voltage ($V_{BD}$) of internal circuit. First, the internal circuit normally operates between $V_{DD}$ and $V_{SS}$, and the ESD protection circuit cannot turn on in this normal circuit operation region. Second, the internal circuit causes failure beyond the positive or negative $V_{BD}$, so the ESD protection circuit becomes invalid in this internal circuit failure region. Besides, it usually reserves some safety margin. Therefore, the ESD protection circuit must shunt ESD current with the voltage within ESD design window as shown in **Figure 1**. As ESD stresses at the I/O pad, the ESD protection circuit turns on at its trigger voltage ($V_{t1}$) and clamps to the holding voltage ($V_h$). The turn-on resistance ($R_{on}$) should be minimized to reduce the joule heat generated in the ESD protection circuit and enhance the current-handling ability, that is the secondary breakdown current ($I_{t2}$).

A typical method to enhance the current-handling ability is to widen the ESD device dimension; however, the large ESD protection device has too large parasitic capacitance to be tolerable for the high-frequency ICs. As shown in **Figure 2(a)**, the parasitic capacitances seen at the input and output (I/O) pads cause signal loss to ground. The parasitic capacitances come from not only the ESD protection circuits but also the pads and the metal connections [13, 14]. If the parasitic capacitance increases, the signal loss dramatically increases at high frequency, as shown in **Figure 2(b)**. To mitigate the performance degradation caused by the parasitic capacitance, the ESD protection circuit must carefully design. For example, a typical specification for the parasitic capacitance of input terminal of a gigahertz IC is 200fF [15].

## 3. ESD protection strategy

At an I/O pad of IC, it may be stressed by positive or negative ESD with grounded $V_{DD}$ or $V_{SS}$. A whole-chip ESD protection design must provide the ESD current paths of all possible combinations, including the positive I/O-to-$V_{DD}$ (PD), positive I/O-to-$V_{SS}$ (PS), negative I/O-to-$V_{DD}$ (ND), and negative I/O-to-$V_{SS}$ (NS) [16]. Since the common ESD protection devices in CMOS technologies include diode, MOSFET, and silicon controlled rectifier (SCR), they are used to implement the ESD protection circuits [17]. To achieve the whole-chip ESD protection, three types of ESD protection schemes are introduced in this chapter.

Type I ESD protection circuit uses one bidirectional ESD protection device between I/O pad and $V_{SS}$ and one bidirectional power-rail ESD clamp circuit between $V_{DD}$ and $V_{SS}$, as shown in **Figure 3(a)**. The bidirectional ESD protection device could be an NMOS or SCR device. Both PS and NS ESD currents can be discharged through the ESD protection device. Besides, PD and ND ESD currents can be discharged through the ESD protection device and the power-rail ESD clamp circuit.

Type II ESD protection circuit uses two unidirectional ESD protection devices from I/O pad to $V_{DD}$ and from $V_{SS}$ to I/O pad, respectively, and one bidirectional power-rail ESD clamp circuit between $V_{DD}$ and $V_{SS}$, as shown in **Figure 3(b)**. The unidirectional ESD protection device was a diode. Both PD and NS ESD currents can be discharged through one unidirectional ESD protection device. For the PS and ND ESD currents, they can be discharged through one ESD protection device and the power-rail ESD clamp circuit.

Type III ESD protection circuit uses a two-branched ESD protection device and an unidirectional ESD protection device between I/O pad and $V_{SS}$ and one bidirectional power-rail ESD clamp circuit between $V_{DD}$ and $V_{SS}$, as shown in **Figure 3(c)**. The two-branched ESD protection device was usually an SCR device. The PS and PD ESD currents can be discharged through the two-branched ESD protection device, and NS and ND ESD currents can be discharged through the unidirectional ESD protection device and the power-rail ESD clamp circuit.
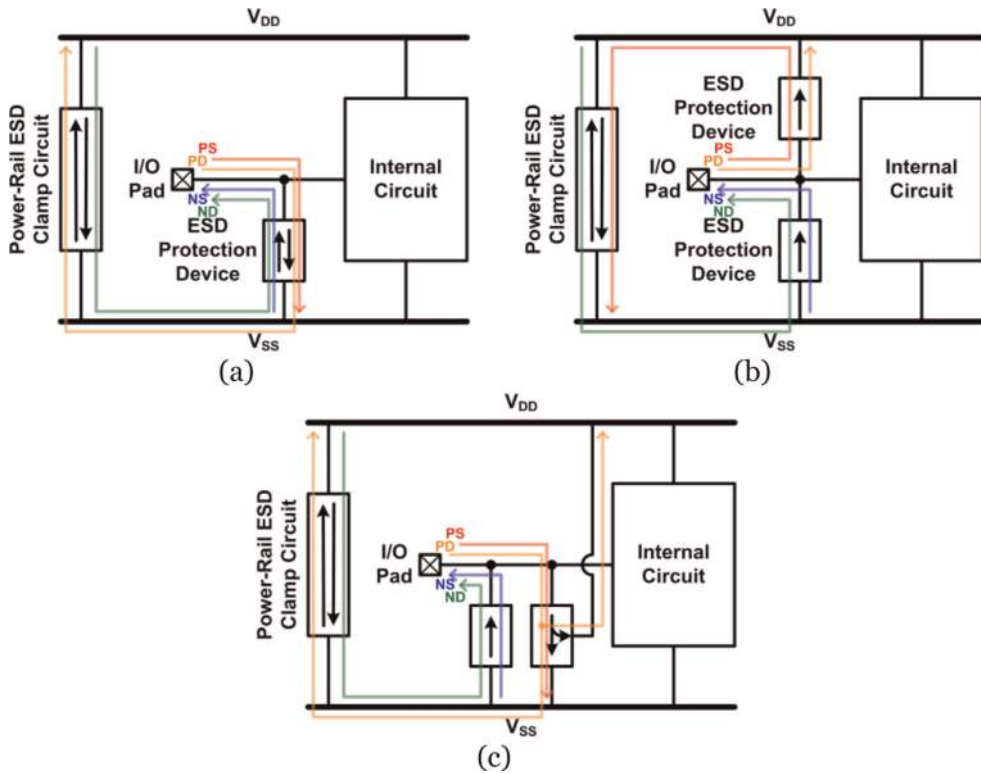
**Figure 3.**
*ESD protection schemes: (a) type I, (b) type II, and (c) type III.*

All the ESD protection devices at I/O pad should be shrunk to lower the parasitic capacitance, while the power-rail ESD clamp circuit could be as large as possible. The large-sized power-rail ESD clamp circuit can help to reduce $R_{on}$ during ESD current discharging, but it will not cause the parasitic capacitance to the I/O pad.

## 4. ESD protection circuit design: Type I

A common ESD protection circuit used in CMOS technology is the grounded-gate NMOS (GGNMOS), as shown in **Figure 4(a)** [18, 19]. In this ESD protection circuit, the NMOS's gate is grounded to keep it off during normal circuit operation.
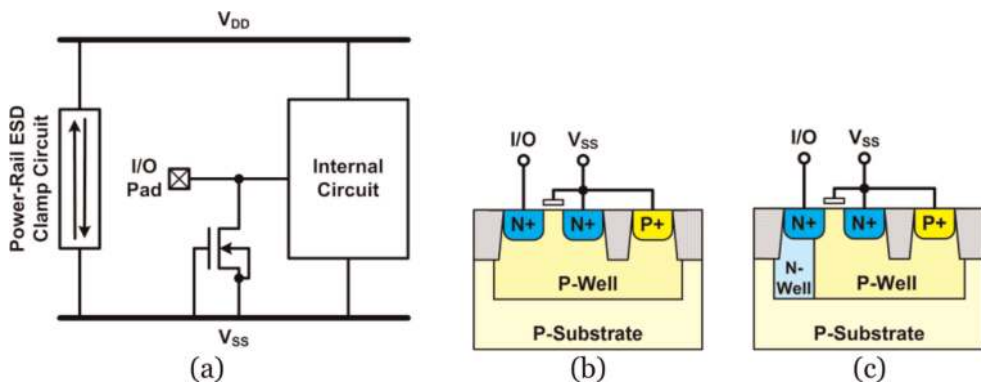


**Figure 4.**
*(a) ESD protection circuit with GGNMOS. Device cross-sectional view of (b) GGNMOS and (c) GGNMOS with additional N-well.*
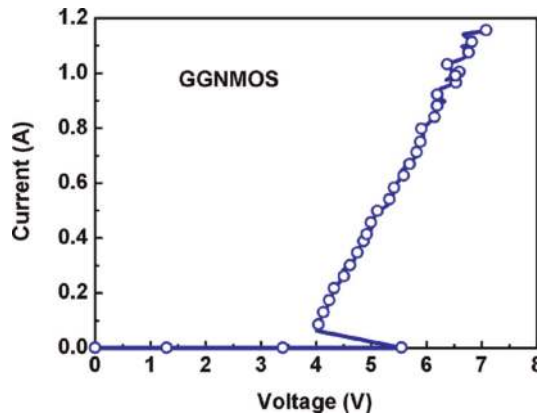
**Figure 5.**
*TLP-measured I-V curve of a GGNMOS (W = 120 μm) in 0.18 μm CMOS technology.*

The GGNMOS turns on as the positive voltage excursions above the trigger voltage ($V_{t1}$). **Figure 5** shows the positive I-V curve of a GGNMOS in 0.18 μm CMOS technology, which is measured by a transmission-line-pulsing (TLP) system. The TLP system with a 10 ns rise time and a 100 ns pulse width is used to investigate the turn-on behavior and the I-V characteristics in high-current regions of the test devices [20]. The trigger voltage ($V_{t1}$), holding voltage ($V_h$), and secondary break-down current ($I_{t2}$) of test devices in the time domain of HBM ESD event can be extracted from the TLP-measured I-V curves. This GGMOS triggers on at 5.6 V, snapbacks to 4.0 V, and discharges ESD current until 1.1A. The GGNMOS with the help of parasitic junction diode turns on as the I/O voltage excursions below the $V_{SS}$ voltage.

The GGNMOS is generally drawn in the multi-finger structure with central drain to save total layout area [21]. **Figure 4(b)** shows the device cross-sectional view of a single-finger GGNMOS. The multi-finger structure can be realized by combining such single-finger structures with sharing drain and source regions between every two adjacent fingers. For the high-frequency applications, the parasitic capacitance of GGNMOS has to be considered. For a given drain width ($W_n$) and length ($L_n$), the total capacitance of a GGNMOS ($C_n$) is given by the drain-gate overlap capacitance ($C_{overlap}$), the N+/P-well bottom junction capacitance ($C_j$), and the N+/P-well sidewall capacitance ($C_{jsw}$), according to the following equation:

$$C_n = C_{overlap} \times W_n + C_j \times W_n \times L_n + C_{jsw} \times 2 \times (W_n + L_n)$$

All the parasitic capacitance ($C_{overlap}$, $C_j$, and $C_{jsw}$) are given by the process. Besides the drain width, the $L_n$ strongly affects the total capacitance. For high-frequency applications, the $L_n$ needs to be optimized by reducing the contact rows, the enclosure of contacts, and the extension of silicide [22, 23]. Also the extension of silicide on drain side increases the ESD robustness of GGNMOS, it implies a larger junction area and thus induces additional parasitic capacitance of the N+/P-well bottom junction. Therefore, a trade-off between the ESD robustness and the parasitic capacitance has to be found. A possible solution to reduce the bottom capacitance with the given $L_n$ is to use an N-well implant below the N+ drain, as shown in **Figure 4(c)**. Most of the bottom N+/P-well capacitance is then replaced by an N-well/P-well sidewall capacitance and N-well/P-substrate bottom capacitance.

Instead of GGNMOS, gate-coupled NMOS and substrate-coupled NMOS have also been used as ESD protection circuit [24]. However, the parasitic capacitance of

MOS-based ESD protection device is usually too large to be tolerable for the high-frequency circuits.

An alternative ESD protection device used in Type I ESD protection circuit is a silicon controlled rectifier (SCR) [25]. The SCR device has been reported to be useful for ESD protection in high-frequency circuits due to its higher ESD robustness within a smaller layout area and lower parasitic capacitance [22]. Besides, the SCR device can be safely used without latchup danger in advanced CMOS technologies with low supply voltage [26]. The equivalent circuit of the SCR consists of a PNP BJT and an NPN BJT, as shown in **Figure 6(a)**. As ESD zapping from I/O to $V_{SS}$, the positive-feedback regenerative mechanism of PNP and NPN results in the SCR device highly conductive to make SCR very robust against ESD stresses. The device structure of the SCR device is illustrated in **Figure 6(b)**. The I/O pad is connected to the first P+ and the pickup N+, which is formed in the N-well. The $V_{SS}$ pad is connected to the second N+ and the pickup P+, which are formed in the nearby P-well. The SCR path between I/O and $V_{SS}$ consists of P+, N-well, P-well, and N+. Besides, the parasitic diode path from $V_{SS}$ to I/O consists of P-well and N-well. The SCR with the help of P-well/N-well junction diode turns on as the I/O voltage excursions below the $V_{SS}$ voltage.

**Figure 7** shows the TLP-measured positive I-V curve of an SCR in 0.18 μm CMOS technology. This SCR triggers on at 16.7 V, snapbacks to 2.1 V, and discharges ESD current until 9.5A. The main drawback of SCR device is the higher trigger voltage and thus the slower turn-on speed. Research works have demonstrated that separation of the N-well and P-well junction can play an important role. The typical SCR device uses the shallow trench isolation (STI) to separate the N-well and P-well. To reduce the trigger voltage of an SCR device, a gate-bounded SCR has been reported, as shown in **Figure 6(c)** [27].
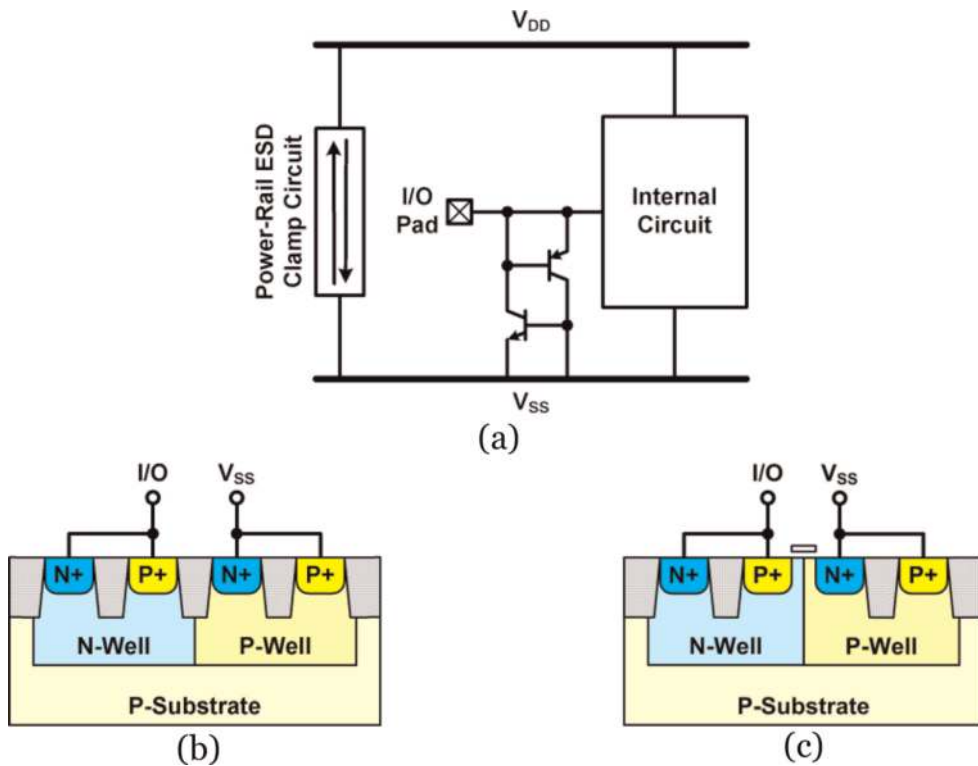


**Figure 6.**
*(a) ESD protection circuit with SCR. Device cross-sectional view of (b) STI-bounded SCR and (c) gate-bounded SCR.*
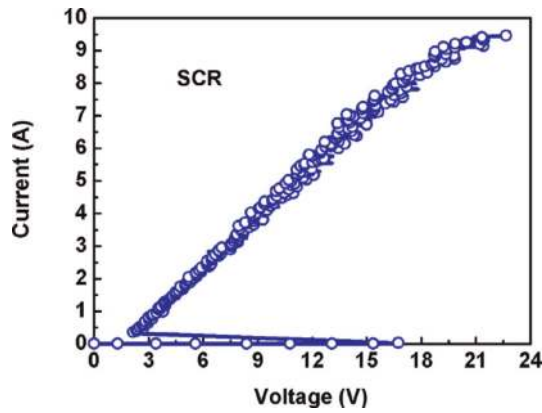
**Figure 7.**
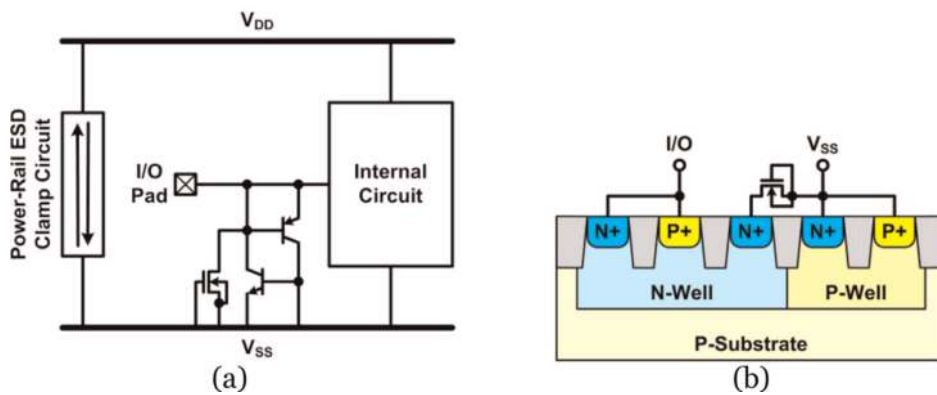*TLP-measured I-V curve of an SCR (W = 120 μm) in 0.18 μm CMOS technology.*



**Figure 8.**
*(a) ESD protection circuit with GGNMOS-triggered SCR and (b) device cross-sectional view of GGNMOS-triggered SCR.*

Another alternative method to reduce the trigger voltage of an SCR device uses the substrate-triggered technique. The trigger signal can be sent into the base terminal of PNP or NPN to enhance the turn-on speed. Some circuit design techniques are reported to enhance the turn-on efficiency of SCR devices, such as the gate-coupled, substrate-triggered, diode-triggered, and gate-grounded-NMOS-triggered (GGNMOS-triggered) techniques [28–30]. **Figure 8(a)** shows the schematic of a GGNMOS-triggered SCR device, and **Figure 8(b)** shows its device cross-sectional view. The GGNMOS is connected between the second N+ in the N-well and $V_{SS}$. The trigger current is drawn from the N-well (base of PNP) to $V_{SS}$ through the GGNMOS. Similarly, the trigger device can be connected between I/O pad and the base and NPN, but the trigger device will also add the parasitic capacitance to I/O. A diode string could also be used as the trigger device, and its parasitic capacitance is lower than the GGNMOS.

Recently, an inductor-assisted diode-triggered SCR (LASCR) has been presented to further reduce the parasitic capacitance [31]. As shown in **Figure 9**, the LASCR consists of an SCR, an inductor, and a diode string. The ESD current path from I/O to $V_{SS}$ consists of P+/N-well/P-well/N+ SCR. The diode string drawn the trigger current from the N-well (base of PNP) to $V_{SS}$ is used to enhance the turn-on efficiency of SCR. As the I/O voltage excursions below the $V_{SS}$ voltage, the ESD current path consists of P-well/N-well diode and inductor.

Under normal circuit operating condition, the inductor can resonate with the parasitic capacitance, and hence the signal loss can be compensated.
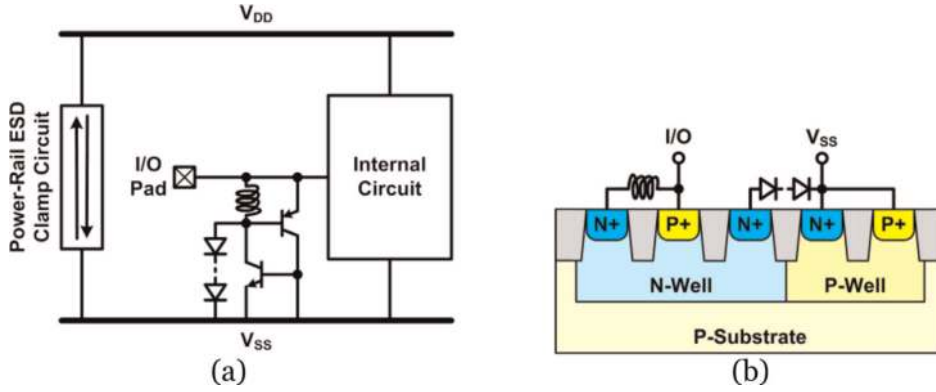
**Figure 9.**
*(a) ESD protection circuit with LASCR and (b) device cross-sectional view of LASCR.*

Once the dimension of SCR has been chosen, the inductance (*L*) can be designed to minimize the high-frequency performance degradation by using the following equation:

$$L = \frac{1}{C_{P+/N-well} \times (2\pi f_o)^2}$$

where $C_{P+/N-well}$ is the parasitic capacitance of P+/N-well junction, and $f_o$ is the operating frequency. For example, the dimension of SCR is selected to be 30 μm, and the $C_{P+/N-well}$ in a 0.18 μm CMOS process is ∼60fF around 30GHz. Therefore, the required *L* for 30GHz applications is 460pH.

**Figure 10(a)** shows the TLP-measured I-V curves of LASCR with 3 and 5 diodes in diode string (LASCR_3D and LASCR_5D) in a 0.18 μm CMOS process. The LASCR_3D triggers on at 5.2 V, snapbacks to 2.9 V, and discharges ESD current until 2.4A, while LASCR_5D triggers on at 7.6 V, snapbacks to 2.9 V, and discharges ESD current until 2.1A. The trigger voltage can be adjusted by adding or reducing the diode numbers. The holding voltage of both LASCR devices exceed $V_{DD}$ (1.8 V in the given CMOS process), which is safe from latchup event.

The signal losses of both LASCR devices are measured through the on-wafer two-port measurement. The measured loss versus frequencies of both LASCR
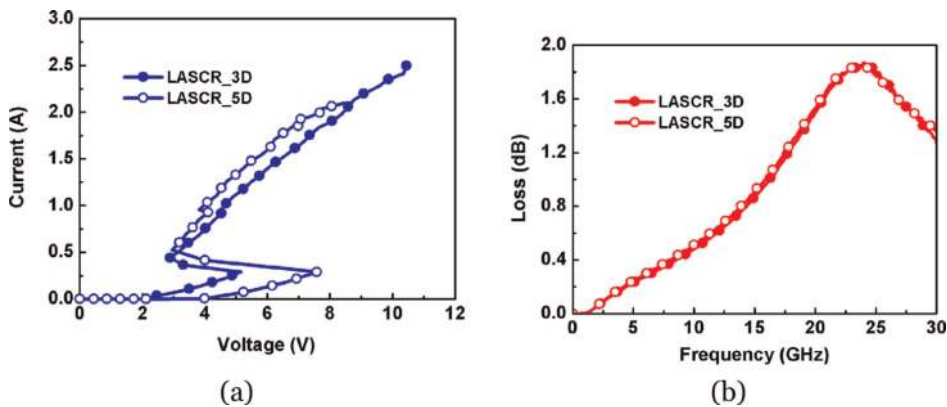


**Figure 10.**
*(a) TLP-measured I-V curves and (b) loss of LASCR (W = 30 μm) with 3 and 5 trigger diodes in 0.18 μm CMOS technology.*

devices is shown in **Figure 10(b)**. The LASCR devices exhibit sufficiently low loss even if the frequency is up to 30GHz. Therefore, LASCR can be a good solution for ESD protection of high-speed applications.

## 5. ESD protection circuit design: Type II

Diode is a typical ESD protection device with unidirectional discharging path [32, 33]. A dual-diode ESD protection circuit for high-frequency applications is shown in **Figure 11(a)**, where two ESD diodes at I/O pad are cooperated with the turn-on efficient power-rail ESD clamp circuit to discharge ESD current in the forward-biased condition [13, 34].

In the CMOS process, the choice for ESD protection diodes includes P+/N-well, N+/P-well, and N-well/P-well diodes. The P+/N-well diode, as shown in **Figure 11(b)**, is used between I/O pad and $V_{DD}$. For the N-well/P-well diode, it may occupy larger layout area than the N+/P-well diode. Thus, the N+/P-well diode, as shown in **Figure 11(c)**, is used between $V_{SS}$ and I/O pad.

The typical diodes use the STI to separate the PN junctions. Besides the STI-bounded diodes, the gate-bounded diodes have been reported, as shown in **Figure 11(d)** and **(e)**. The gate-bounded diodes were introduced by Voldman in order to improve the ESD robustness of STI bounded diodes [35].

In order to reduce the parasitic capacitance or provide the large signal-swing tolerance, the ESD protection diodes in stacked configuration have been presented [36, 37], as shown in **Figure 12(a)**. The device cross-sectional views of the conventional stacked diodes are shown in **Figure 12(b)** and **(c)**. Two P+/N-well diodes (stacked P diodes) can apply to I/O-to-$V_{DD}$, and two N+/P-well diodes (stacked N diodes) can apply to $V_{SS}$-to-I/O, as shown in **Figure 12(b)** and **(c)**, respectively. With the stacked diodes, the junction capacitances are connected in series, and the
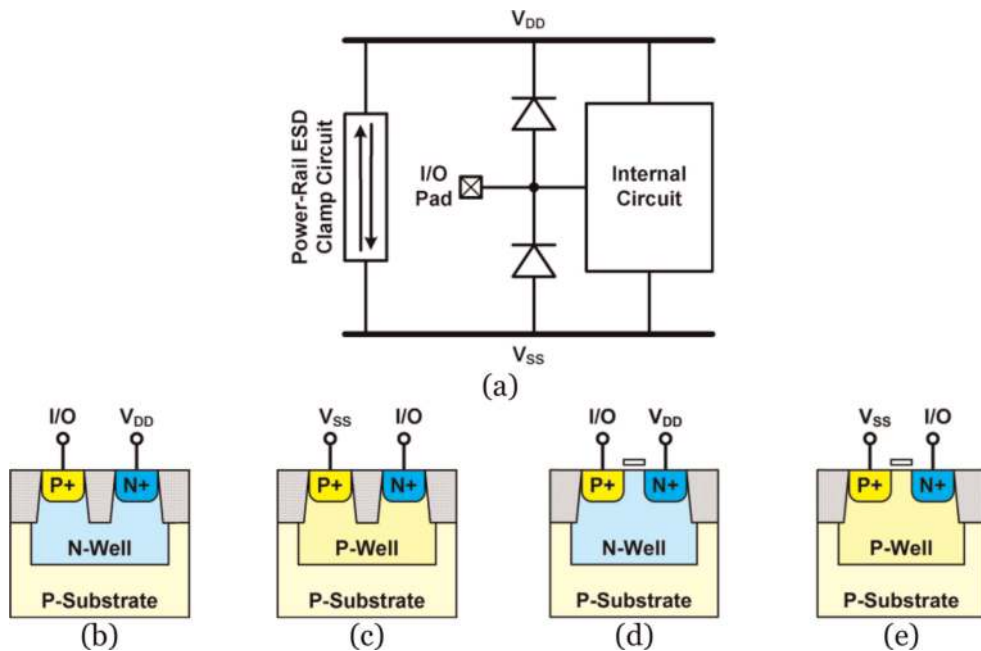


**Figure 11.**
*(a) ESD protection circuit with diodes. Device cross-sectional view of (b) STI-bounded P+/N-well diode, (c) STI-bounded N+/P-well diode, (d) gate-bounded P+/N-well diode, and (e) gate-bounded N+/P-well diode.*
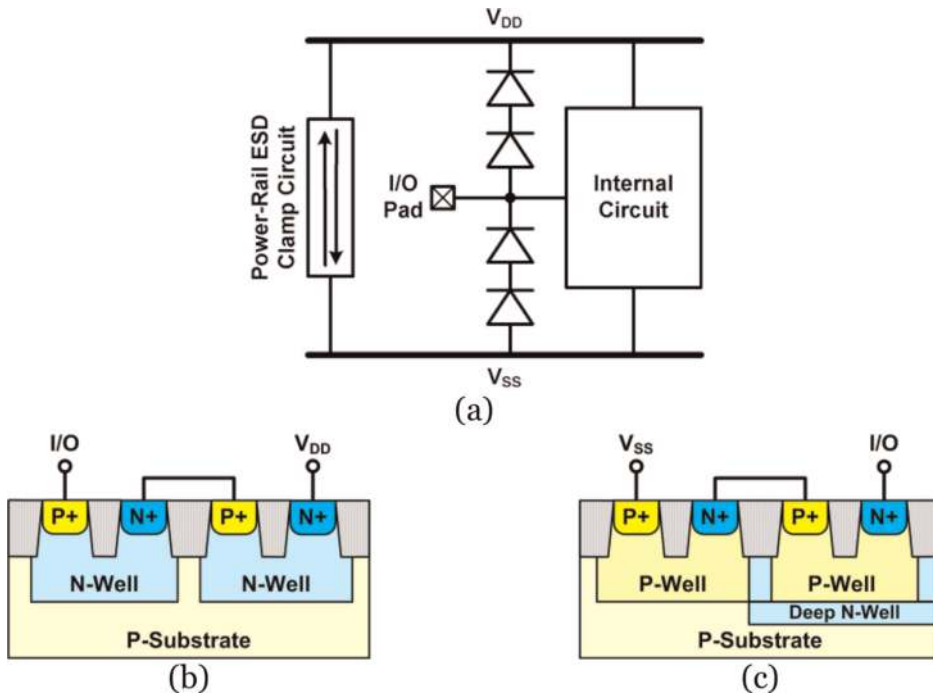
**Figure 12.**
*ESD protection circuit with stacked diodes. (a) ESD protection circuit with stacked diodes. Device cross-sectional view of (b) stacked P+/N-well diode and (c) stacked N+/P-well diode.*

overall parasitic capacitance becomes smaller. However, the stacked configuration is adverse to ESD protection because the overall turn-on resistance and the clamping voltage of the stacked diodes during ESD stresses are increased as well.

For effective ESD protection, the stacked diodes with embedded SCR (SDSCR) have been presented [38, 39]. The SCR device has been reported to be useful for ESD protection with low turn-on resistance, low parasitic effects, and high ESD robustness. The stacked diodes with embedded SCR are illustrated in **Figure 13**. In this design, a P+/N-well diode and an N+/P-well diode are stacked, and a P+/N-well/P-well/N+ SCR is embedded to form the ESD current path. A deep N-well structure is used to isolate the P-well region from the common P-substrate, so the SDSCR can apply to I/O-to-$V_{DD}$ or $V_{SS}$-to-I/O. In the beginning of ESD stress, the initial current will be discharged through the stacked diodes, and then the primary current will be discharged through the embedded SCR. The stacked diodes also play the role of trigger circuit of SCR, because the current drawn from N-well and
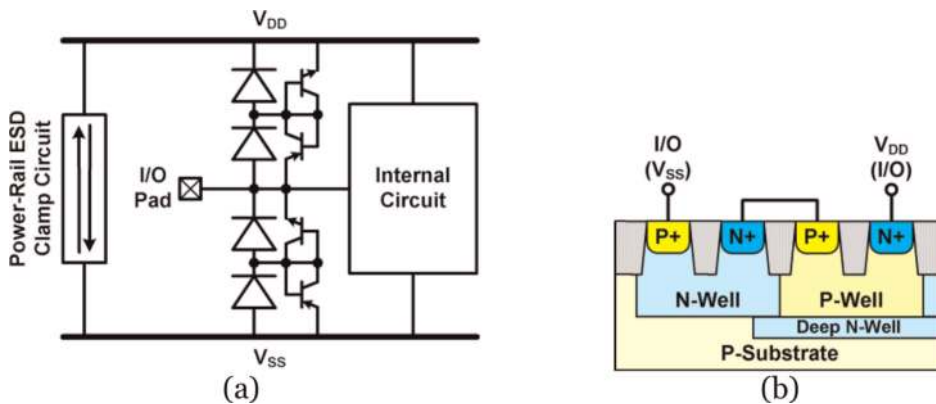


**Figure 13.**
*(a) ESD protection circuit with SDSCR and (b) device cross-sectional view of SDSCR.*
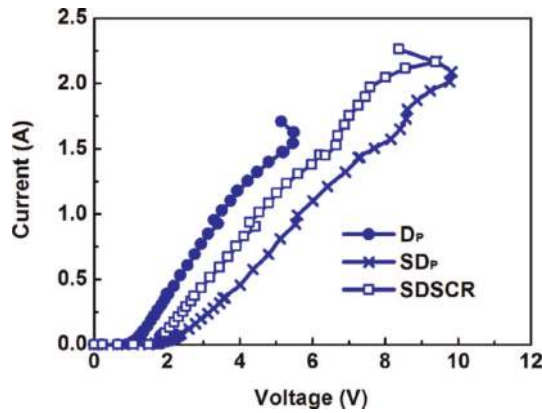
**Figure 14.**
*TLP-measured I-V curves of $D_P$, $SD_P$, and SDSCR (W = 20 μm) in 0.18 μm CMOS technology.*
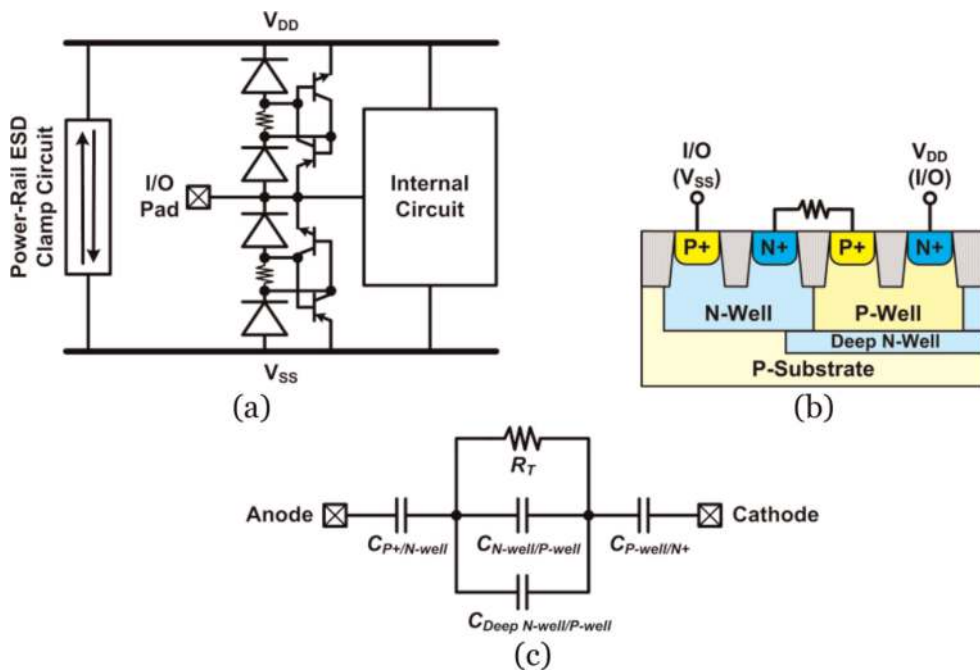


**Figure 15.**
*(a) ESD protection circuit with RTSCR. (b) device cross-sectional view and (c) simplified model of RTSCR.*

injected into P-well can also trigger the PNP and the NPN of SCR. **Figure 14** shows the TLP-measured I-V curves of P+/N-well diode ($D_P$), stacked P+/N-well diodes ($SD_P$), and stacked diodes with embedded SCR (SDSCR) in a 0.18 μm CMOS process. We can find that turn-on resistance or the clamping voltage of single diode is much lower than that of the stacked diodes. The embedded SCR can help to slightly reduce the turn-on resistance and the clamping voltage of the stacked diodes. In fact, some layout skills can be used to further improve the turn-on efficient of the stacked diodes with embedded SCR [40].

Recently, a similar structure of the stacked diodes with embedded SCR, where a resistor uses to separate two diodes, has been reported [41]. The resistor acts as the trigger element of SCR, so the device is named resistor-triggered SCR (RTSCR). **Figure 15(a)** and **(b)** shows the schematic and the device cross-sectional view of RTSCR. The resistor can also reduce the parasitic capacitance of the ESD protection

circuit. Considering the simplified SCR model by using junction capacitances, as shown in **Figure 15(c)**, the equivalent capacitance seen at anode or cathode of RTSCR can be calculated by the following equation:

$$C_{RTSCR} = \frac{Im(Y_{RTSCR})}{\omega} = \frac{Im\left(\frac{1}{\frac{1}{j\omega C_{P+/N-Well}} + \frac{1}{\frac{1}{R_T} + j\omega C_{P-Well/N-Well(Deep\ N-Well)}} + \frac{1}{j\omega C_{P-Well/N+}}}\right)}{\omega}$$

where $Y_{RTSCR}$ denotes the admittance of the RTSCR, $R_T$ is the resistance, and $C_{P+/N-Well}$, $C_{P-Well/N-Well(Deep\ N-Well)}$ and $C_{P-Well/N+}$ denote the junction capacitances. To simplify the above equation, the junction capacitance is rewritten to $C_J$, and then the parasitic capacitance of the RTSCR can be expressed by the following equation:

$$C_{RTSCR} = Im\left(\frac{1}{\frac{2}{jC_J} + \frac{1}{\frac{1}{\omega R_T} + jC_J}}\right) = \frac{\frac{2}{C_J} + \frac{\omega^2 R_T^2 C_J}{1+\omega^2 R_T^2 C_J^2}}{\left(\frac{2}{C_J} + \frac{\omega^2 R_T^2 C_J}{1+\omega^2 R_T^2 C_J^2}\right)^2 + \left(\frac{\omega R_T}{1+\omega^2 R_T^2 C_J^2}\right)^2} \approx \frac{C_J}{2 + \frac{3}{2}\omega^2 R_T^2 C_J^2}$$

It can be noted that the parasitic capacitance of the RTSCR can be reduced by adding the resistor. Generally, the capacitance reduction of RTSCR can be up to 30%. Therefore, the ESD protection circuit with dual RTSCRs can be used for high-frequency applications.

## 6. ESD protection circuit design: Type III

**Figure 16(a)** shows another SCR-based ESD protection circuit [13]. The typical SCR device in CMOS process consists of P+, N-well, P-well, and N+. Instead of connecting the N-well to I/O pad, connecting the N-well to $V_{DD}$ avoids the parasitic capacitance or noise coupling from P-substrate or P-well to N-well and I/O [42]. As shown in **Figure 16(b)**, the I/O pad is connected to the first P+, which is formed in the N-well. The pickup N+ in the N-well is biased to $V_{DD}$. The $V_{SS}$ pad is connected to the second N+ and the pickup P+, which are formed in the nearby P-well. The SCR path between I/O and $V_{SS}$ consists of P+, N-well, P-well, and N+. Besides, the parasitic diode path from I/O to $V_{DD}$ consists of P+ and N-well. In this structure, the PS and the PD ESD currents can be discharged through the SCR path and its parasitic diode path. The NS and the ND ESD currents need reverse diode and power-rail ESD clamp circuit to form their discharging paths.
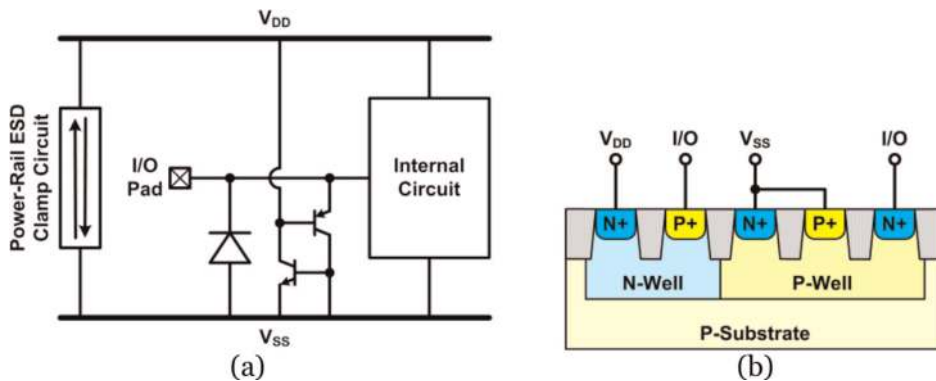


**Figure 16.**
*(a) ESD protection circuit with SCR and diode and (b) device cross-sectional view of SCR and diode.*
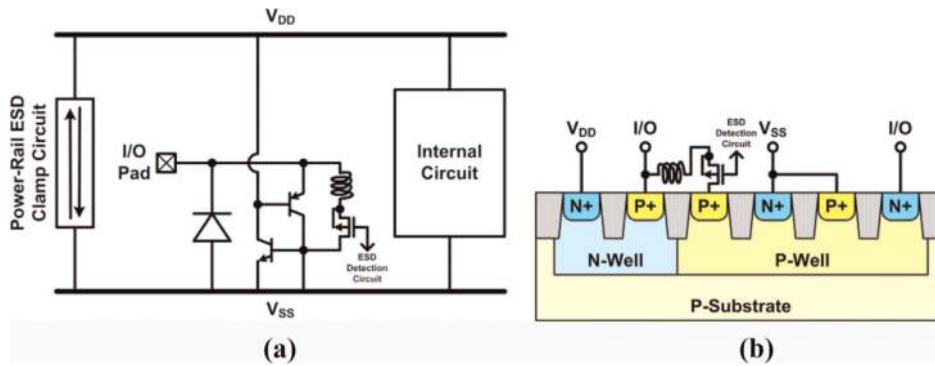
**Figure 17.**
*ESD protection circuit with LTSCR and reverse diode. (a) ESD protection circuit with LTSCR and reverse diode and (b) device cross-sectional view of LTSCR and reverse diode.*

The SCR device in this ESD protection circuit still has the drawbacks of higher trigger voltage and the slower turn-on speed. The circuit design techniques, including the gate-coupled, substrate-triggered, diode-triggered, and GGNMOS-triggered techniques can be used to enhance the turn-on efficiency of SCR device. Of course, the capacitive triggering device increases the total parasitic capacitance seen at the I/O pad, even if the triggering device is not directly connected to I/O. Recently, an SCR device with inductive triggering device has been presented [43]. That inductor-triggered SCR (LTSCR) is proposed for ESD protection of high-frequency applications to achieve low high-frequency performance degradation, low trigger voltage, and high ESD robustness. In this design, the inductor provides a current path to trigger the SCR device, and it can also compensate the parasitic capacitance of ESD protection devices.

**Figure 17(a)** shows the ESD protection circuit with an LTSCR and a reverse diode. This design consists of an SCR device and a reverse diode as the main ESD current path, and an inductor ($L_{trig}$), a MOS transistor ($M_{trig}$), and an RC-based ESD detection circuit as the trigger circuit. The initial-on PMOS transistor is selected for $M_{trig}$ to quickly pass the trigger current to SCR device [44]. The positive and negative ESD current discharging paths for the I/O pad are provided by the SCR and the reverse diode. **Figure 17(b)** shows the device cross-sectional view of inductor-triggered SCR. Under ESD stress conditions, the inductor and PMOS are used to provide the trigger path between the I/O pad and the base of NPN of the SCR device. When the trigger current is sent into the base of NPN of the SCR device, the SCR device can be quickly triggered on to discharge the ESD current from the I/O pad to $V_{SS}$. The ESD detection circuit usually uses RC timer to distinguish the ESD-stress conditions from the normal circuit operating conditions, and the PMOS transistor is well controlled to turn on or off by the ESD detection circuit. Under normal circuit operating conditions, the inductor can compensate the parasitic capacitance of SCR and diode.

In this circuit, the dimensions of the inductor ($L_{trig}$), PMOS transistor ($M_{trig}$), SCR device, and reverse diode can be designed to minimize the high-frequency performance degradation. Since the capacitor used in power-rail ESD clamp circuit is large enough to keep the node between R and C at AC ground under normal circuit operating conditions, the impedance of the trigger path ($Z_{trig}$) seen at the I/O pad to ground can be calculated as:

$$Z_{trig} \approx j\omega L_{trig} + \frac{1}{j\omega C_{trig}} = j\omega \left( L_{trig} - \frac{1}{\omega^2 C_{trig}} \right)$$

where $C_{trig}$ is the sum of gate-to-source, gate-to-body, and drain-to-body capacitances of the PMOS. The resonance angular frequency ($\omega_o$) can be obtained by

$$\omega_o = \frac{1}{\sqrt{\left(L_{trig} - \frac{1}{\omega_o^2 C_{trig}}\right) C_{ESD}}}$$

where $\omega_o$ is designed to be the operating frequency, and $C_{ESD}$ is the parasitic capacitance contributed by the SCR and diode. The sizes of SCR and diode depend on the required ESD robustness, while the size of $M_{trig}$ transistor depends on the required trigger current. Once the sizes of $M_{trig}$ transistor, SCR, and diode have been chosen, the required inductance ($L_{trig}$) can be determined.

## 7. Conclusion

A comprehensive review in the field of ESD protection design for high-frequency integrated circuits is presented in this chapter. Besides improving the ESD robustness, the parasitic effects from ESD protection devices must be minimized or canceled to optimize the high-frequency performance simultaneously. Furthermore, the ESD protection circuits and high-frequency circuits can be co-designed to achieve both good circuit performance and high ESD robustness. The on-chip ESD protection designs for high-frequency circuits will be continuously an important design task in CMOS technology.

## Author details

Chun-Yu Lin
Department of Electrical Engineering, National Taiwan Normal University, Taipei, Taiwan

*Address all correspondence to: cy.lin@ieee.org

IntechOpen

# References

[1] Rangan S, Rappaport T, Erkip E. Millimeter-wave cellular wireless networks: Potentials and challenges. Proceedings of the IEEE. 2014;**102**: 366-385

[2] Fritsche D, Tretter G, Carta C, Ellinger F. Millimeter-wave low-noise amplifier design in 28-nm low-power digital CMOS. IEEE Transactions on Microwave Theory and Techniques. 2015;**63**:1910-1922

[3] Abidi A. CMOS microwave and millimeter-wave ICs: The historical background. In: Proceedings of the IEEE International Symposium on Radio-Frequency Integration Technology (RFIT). 2014

[4] Gossner H. Design for ESD protection at its limits. In: Proceedings of the Symposium on VLSI Technology. 2013

[5] Li J, Mishra R, Shrivastava M, Yang Y, Gauthier R, Russ C. Technology scaling effects on the ESD performance of silicide-blocked PMOSFET devices in nanometer bulk CMOS technologies. In: Proceedings of the Electrical Overstress/ Electrostatic Discharge Symposium (EOS/ESD). 2011

[6] Wang A, Feng H, Zhan R, Xie H, Chen G, Wu Q, et al. A review on RF ESD protection design. IEEE Transactions on Electron Devices. 2005;**52**:1304-1311

[7] Natarajan M, Linten D, Thijs S, Jansen P, Trémouilles D, Jeamsaksiri W, Nakaie T, Sawada M, Hasebe T, Decoutere S, Groeseneken G. RFCMOS ESD protection and reliability. In: Proceedings of the International Symposium on the Physical and Failure Analysis of Integrated Circuits (IPFA); 2005. p. 59-66

[8] Voldman S. ESD: RF Technology and Circuits. Chichester: John Wiley & Sons; 2006

[9] Ker M, Lin C, Hsiao Y. Overview on ESD protection designs of low-parasitic capacitance for RF ICs in CMOS technologies. IEEE Transactions on Device and Materials Reliability. 2011; **11**:207-218

[10] Voldman S. ESD: Analog Circuits and Design. Chichester: John Wiley & Sons; 2015

[11] Amerasekera A, Duvvury C. ESD in Silicon Integrated Circuits. Chichester: John Wiley & Sons; 2002

[12] Li J, Chatty K, Gauthier R, Mishra R, Russ C. Technology scaling of advanced bulk CMOS on-chip ESD protection down to the 32nm node. In: Proceedings of the Electrical Overstress/Electrostatic Discharge Symposium (EOS/ESD). 2009

[13] Galy P, Jimenez J, Meuris P, Schoenmaker W, Dupuis O. ESD RF protections in advanced CMOS technologies and its parasitic capacitance evaluation. In: Proceedings of the IEEE International Conference on IC Design & Technology (ICICDT); 2011

[14] Peng B, Lin C. Low-loss I/O pad with ESD protection for K/Ka-bands applications in nanoscale CMOS process. IEEE Transactions on Circuits and Systems II: Express Briefs. 2018;**65**: 1475-1479

[15] Soldner W, Streibl M, Hodel U, Tiebout M, Gossner H, Schmitt-Landsiedel D, et al. RF ESD protection strategies: Codesign vs. low-C protection. In: Proceedings of the Electrical Overstress/Electrostatic Discharge Symposium (EOS/ESD). 2005

[16] Ker M. Whole-chip ESD protection design with efficient VDD-to-VSS ESD clamp circuit for submicron CMOS

VLSI. IEEE Transactions on Electron Devices. 1999;**46**:173-183

[17] Voldman S. ESD: Circuits and Devices. Chichester: John Wiley & Sons; 2015

[18] Wang W, Dong S, Zhong L, Zeng J, Yu Z, Liu Z. GGNMOS as ESD protection in different nanometer CMOS process. In: Proceedings of the IEEE International Conference on Electron Devices and Solid-State Circuits (EDSSC); 2014

[19] Paul M, Russ C, Kumar B, Gossner H, Shrivastava M. Physics of current filamentation in ggNMOS devices under ESD condition revisited. IEEE Transactions on Electron Devices. 2018; **65**:2981-2989

[20] Maloney T, Khurana N. Transmission line pulsing techniques for circuit modeling of phenomena. In: Proceedings of the Electrical Overstress/ Electrostatic Discharge Symposium (EOS/ESD). 1985

[21] Lee J, Wu K, Huang S, Tang C. The dynamic current distribution of a multi-fingered GGNMOS under high current stress and HBM ESD events. In: Proceedings of the IEEE International Reliability Physics Symposium (IRPS); 2006

[22] Richier C, Salome P, Mabboux G, Zaza I, Juge A, Mortini P. Investigation on different ESD protection strategies devoted to 3.3 V RF applications (2 GHz) in a 0.18 μm CMOS process. Journal of Electrostatics. 2002;**54**:55-71

[23] Chen T, Ker M, Wu C. Experimental investigation on the HBM ESD characteristics of CMOS devices in a 0.35-μm silicided process. In: Proceedings of the IEEE International Symposium on VLSI Technology, Systems, and Applications. VLSI-TSA; 1999; Hsinchu

[24] Song B, Han Y, Li M, Liou J, Dong S, Guo W, Huang D, Ma F, Miao M. Design analysis of novel substrate-triggered GGNMOS in 65nm CMOS process. In: Proceedings of the IEEE International Symposium on the Physical and Failure Analysis of Integrated Circuits (IPFA); 2010

[25] Ker M, Hsu K. Overview of on-chip electrostatic discharge protection design with SCR-based devices in CMOS integrated circuits. IEEE Transactions on Device and Materials Reliability. 2005;**5**:235-249

[26] Dai C, Chen S, Linten D, Scholz M, Hellings G, Boschke R, Karp J, Hart M, Groeseneken G, Ker M, Mocuta A, Horiguchi N. Latchup in bulk FinFET technology. In: Proceedings of the IEEE International Reliability Physics Symposium (IRPS); 2017

[27] Chang T, Hsu Y, Tsai T, Tseng J, Lee J, Song M. High-k metal gate-bounded silicon controlled rectifier for ESD protection. In: Proceedings of the Electrical Overstress/Electrostatic Discharge Symposium (EOS/ESD). 2012

[28] Ker M, Hsu K. Substrate-triggered SCR device for on-chip ESD protection in fully silicided sub-0.25-μm CMOS process. IEEE Transactions on Electron Devices. 2003;**50**:397-405

[29] Jang S, Gau M, Lin J. Novel diode-chain triggering SCR circuits for ESD protection. Solid-State Electronics. 2000;**44**:1297-1303

[30] Russ C, Mergens M, Verhaege K, Armer J, Jozwiak P, Kolluri G, et al. GGSCRs: GGNMOS triggered silicon controlled rectifiers for ESD protection in deep sub-micron CMOS processes. In: Proceedings of the Electrical Overstress/ Electrostatic Discharge Symposium (EOS/ESD). 2001; Portland

[31] Lin C, Chang R. Design of ESD protection device for K/Ka-band applications in nanoscale CMOS process. IEEE Transactions on Electron Devices. 2015;**62**:2824-2829

[32] Bhatia K, Jack N, Rosenbaum E. Layout optimization of ESD protection diodes for high-frequency I/Os. IEEE Transactions on Device and Materials Reliability. 2009;**9**:465-475

[33] Chen S, Linten D, Lee J, Scholz M, Hellings G, Sibaja-Hernandez A, Boschke R, Song M, See Y, Groeseneken G, Thean A. Proceedings of the IEEE International Electron Devices Meeting (IEDM); 2014

[34] Yeh C, Ker M, Liang Y. Optimization on layout style of ESD protection diode for radio-frequency front-end and high-speed I/O interface circuits. IEEE Transactions on Device and Materials Reliability. 2010;**10**: 238-246

[35] Voldmm S, Schulz R, Howard J, Gross V, Wu S, Yapsir A, et al. CMOS-on-SOI ESD protection networks. In: Proceedings of the Electrical Overstress/Electrostatic Discharge Symposium (EOS/ESD). 1996

[36] Ruberto M, Degani O, Wail S, Tendler A, Fridman A, Goltman G. A reliability-aware RF power amplifier design for CMOS radio chip integration. In: Proceedings of the IEEE International Reliability Physics Symposium (IRPS); 2008

[37] Son M, Park C. Electrostatic discharge protection devices with series connection using distributed cell-based diodes. Electronics Letters. 2014;**50**:168-170

[38] Lin C, Fan M, Ker M, Chu L, Tseng J, Song M. Improving ESD robustness of stacked diodes with embedded SCR for RF applications in 65-nm CMOS. In:

Proceedings of the IEEE International Reliability Physics Symposium (IRPS); 2014

[39] Lin C, Fu W. Diode string with reduced clamping voltage for efficient on-chip ESD protection. IEEE Transactions on Device and Materials Reliability. 2016;**16**:688-690

[40] Lin C, Fan M. Optimization on layout style of diode stackup for on-chip ESD protection. IEEE Transactions on Device and Materials Reliability. 2014; **14**:775-777

[41] Lin C, Chen C. Resistor-triggered SCR device for ESD protection in high-speed I/O interface circuits. IEEE Electron Device Letters. 2017;**38**:712-715

[42] Afzali-Kusha A, Nagata M, Verghese N, Allstot D. Substrate noise coupling in SoC design: Modeling, avoidance, and validation. Proceedings of the IEEE. 2006;**94**:2109-2138

[43] Lin C, Chu L, Ker M. ESD protection design for 60-GHz LNA with inductor-triggered SCR in 65-nm CMOS process. IEEE Transactions on Microwave Theory and Techniques. 2012;**60**:714-723

[44] Ker M, Chen S. Implementation of initial-on ESD protection concept with PMOS-triggered SCR devices in deep-submicron CMOS technology. IEEE Journal of Solid-State Circuits. 2007;**42**: 1158-1168