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Fully Integrated CMOS Low-Gain-Wide-Range 2.4 GHz Phase Locked Loop for LR-WPAN Applications

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1. Introduction

The last decade has been marked by a rapid growing of wireless market and this phenomenon trends to accelerate in future years. This market serves different demands in wireless applications for cellular phones, wireless local area networks (WLAN), wireless personal area networks (WPAN), phased array RF systems, and other emerging wireless communication such as wireless body area network (WBAN), radar, and imaging applications operating in a very wide frequency range: few MHz up to 100GHz (ITRS, 2007). The introduction of digital signal processing inside communication systems constitutes one of the main reasons of this growth. This digital revolution results from research and development related to high performance CMOS technologies, coming with lower cost than classical bipolar technology and allows the integration of complex digital and analog function on the same chip. Today, digital evolution and the market flight of mobile communications lead to several changes in the analog part of the radio-frequency (RF) front end of transceivers (interface between antenna and digital modem). The need for RF front end to detect very weak signal (few μV) at very high frequency (~GHz) and in the same time to be able to transmit high power signal (few Watts) requires high performance analog circuits such as filters, amplifiers, mixers and oscillators. Historically, RF communications was reserved to military uses where the performance predominated without real cost constraints. The introduction of wireless communication in commercial and public domain where cost reduction is the leitmotiv has leaded the analog part to be the most critical part of current and future RF systems (Chen, 2000).

2. Evolution of LR-WPAN: Standardization

Coming with rapid developments of information technology in the 1980s, laptops have begun to be used elsewhere than as part of the office. With the accession of the Internet in 90's, mobility has become problematic: strong demand appeared to allow connecting to the internet everywhere. The emerged solution was to connect computers to each other by the

way of radio wave rather than wire, resulting to wireless local area network (WLAN). WLAN requires a fixed access point that can connect multiple mobile stations.
The dramatic rise of the demand and application fields has conducted to standardization. It defines an interface between "client" and "access point" in the wireless network by specifying both the physical layer (PHY) and the software layer (or MAC: Medium Access Control). The goal is to ensure the interoperability of data networking, the security services and a range of wireless home and building control solutions. This will assure consumers to buy products from different manufacturers with confidence that the products will work together (ZigBee Alliance). Working group is formed to create different standards according to their characteristics: distance of coverage, data-rate, communication protocol, etc. The IEEE 802.15 working group relates wireless personal area network (WPAN) which focuses low-cost, low power, short range and very small size circuit. There are three classes of WPAN according to data rate, battery life, and quality of service (QoS). The high data rate PAN (IEEE 802.15.3) is suitable for multi-media applications (streaming) that require very high QoS. Medium rate WPANs (IEEE 802.15.1/Blueetooth) will handle a variety of tasks ranging from cell phones to PDA communications and have QoS suitable for voice communications. The low rate WPANs (IEEE 802.15.4/LR-WPAN) is intended to serve a set of industrial, residential and medical applications with very low power consumption and cost requirement not considered by the above WPANs and with relaxed needs for data rate and QoS.
ZigBee standard is one of existing LR-WPAN. It is expected to provide low cost and low power connectivity for equipment that needs battery life as long as several months to several years but does not require data transfer rates as high as those enabled by Bluetooth. In addition, ZigBee can be implemented in mesh networks larger than that of Bluetooth. ZigBee compliant wireless devices are expected to transmit 10-75 meters, depending on the RF environment and the power output consumption required for a given application, and will operate in the unlicensed RF worldwide (2.4GHz global, 915MHz Americas or 868MHz Europe). The data rate is 250kbps at 2.4GHz, 40kbps at 915MHz and 20kbps at 868MHz. (ZigBee Alliance)

3. Wireless communications: transceiver circuit challenges

Each wireless transceiver, responds to its proper characteristics and constraints according to the application, in order to achieve an efficient transmission of the data without altering neighbor transceivers. Among the main characteristics, one can note the maximum distance of coverage, the number of the communication channels, the value of the carrier frequency, the power level of the transmitted signal, the bit-error-rate (BER), the noise and so on. Mobile applications are subjected to many constraints, namely the circuit cost, the autonomy of the battery, the interoperability with other applications, etc.
The operating characteristics of the transceiver can be derived from the standard definition; however, hard constraints related to the system architecture, the power and the cost constitute real challenges for current and future wireless communications. These performances depend both on the quality and the cost of the technology used to implement the design and on the design solution adopted to meet the standard as well as the given specification requirement.

3.1 Technology consideration

The feasibility of many wireless products mainly depends on the intrinsic performances of the technology used in radio-frequency (RF) and analog/mixed-signal (AMS) which can be divided to four categories depending on the field of applications. Compound III-V semiconductors (GaAS, InP, etc.) have traditionally dominated the millimeter wave spectrum over the past several decades. However, today, with the drive to low-cost high-volume applications such as auto radar, along with scaling to sub-100nm dimensions, devices implemented with Si and SiGe are rapidly moving up to frequencies that were once the exclusive domain of the III-Vs. CMOS, BiCMOS and SiGe for heterojunction bipolar transistor are the most adopted process, while implementing monolithic system-on-chip (SoC) and intellectual property (IP) for wireless applications.

Generally, the choice criterion of the technology is driven by cost, frequency bands, power consumption, functionality, volumes of product and standards and protocols. Today, BiCMOS in cellular transceivers has the biggest share in terms of volume compared to CMOS. But, the opposite may occur in the future as evident by the expanding wireless local area network (WLAN) connectivity market that is dominated by CMOS transceivers (ITRS, 2007). CMOS process is mainly used to implement on chip digital circuits since it allows high integration density with a lower cost than any other processes. The size reduction and the process refinement of CMOS devices allowed increasing the transition frequency and the operating frequency of RF and analog/mixed signal circuits. Several wireless transceiver designs (GSM, DECT, DCS1800, etc.) have taken benefits of this feature and have been efficiently realized with CMOS technology (Mikkelsen, 1998). However, scaling down the gate size comes with supply voltage reduction, penalizing the voltage dynamic, signal-to-noise ratio, and linearity. Additional process step is then required during the fabrication for higher voltage supply increasing the cost. Figure 1 depicts some examples of wireless applications fully implemented in CMOS technology as a function of operating frequency (Crols & Steyaert, 1995).

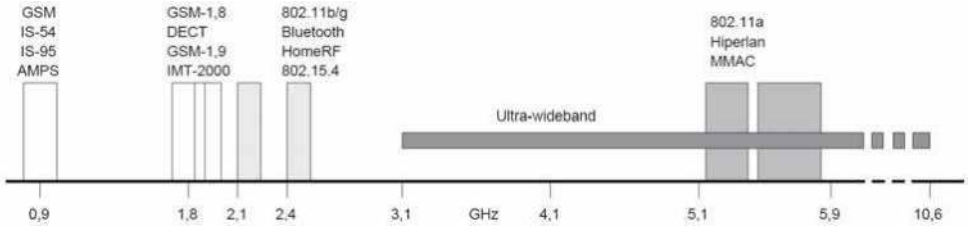

Fig. 1. Repartition of some wireless applications versus operating frequencies

3.2 Wireless communication design challenges

The constraints imposed by Bluetooth or wireless fidelity (WiFi) standards in terms of data-rate, channels spacing and access method (CDMA) are not compatible with the design objectives related to the achievement of low-cost products such as LR-WPAN. IEEE 802.15.4 aims to define a production cost of chips < $2, with substantial autonomy battery life (>1 year). In practice, this hard consumption requirement imposes the system to standby for 99.9% of battery lifetime. Note that this network will coexist with other networks operating in the same frequency band (Bluetooth, WiFi, etc.). Thus, the fact that it operates only 1% of the time makes LR-WPAN system little disruptive of other networks.

Despite recent advances in terms of power consumption: dedicated circuit topology for very low power, reduction of leakage currents in CMOS process thanks to SOI device for example, good performance of ZigBee are mainly due to its "sleepy" (standby mode) resulting to very weak utilization of the medium protocol (MAC). Moreover, very low cost constraints lead to innovative transceiver architectures which are little greedy in silicon area while achieving good performances. The example of Zigbee transceiver, illustrated in Figure 2, uses low-IF receiver technique. It takes the advantage of many of the desirable properties of zero-IF architectures, but avoids the DC offset and 1/f noise problems. The use of a non-zero IF re-introduces the image issue. However, when there are relatively relaxed image and neighbouring channel rejection requirements they can be satisfied by carefully designed low-IF receivers. Image signal and unwanted blockers can be rejected by quadrature downconversion (complex mixing) and polyphase filtering.

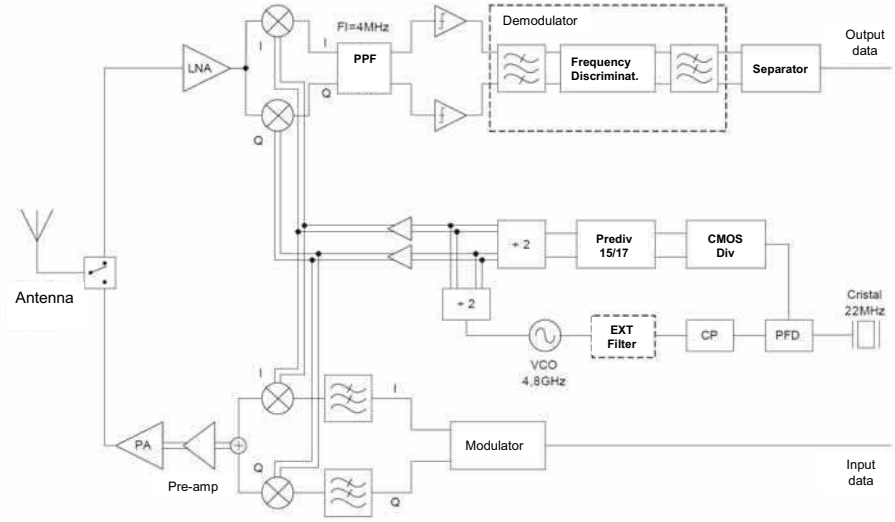

Fig. 2. Example of Zigbee transceiver proposed in (Choi et al, 2003)

In order to facilitate the complete integration of the radio section on chip with lower silicon area and lower cost, zero-IF architecture or direct-conversion receiver constitutes an efficient solution and is a good platform for multi-band multi-standard radios (e.g., 3G-WCDMA handsets and LR-WPAN). This architecture is also well adapted to analog/baseband co-design by the implementation of RF impairments compensation algorithms (e.g., DC offset, mismatch, low-frequency phase noise). An example of direct conversion receiver architecture is illustrated in Figure 3.

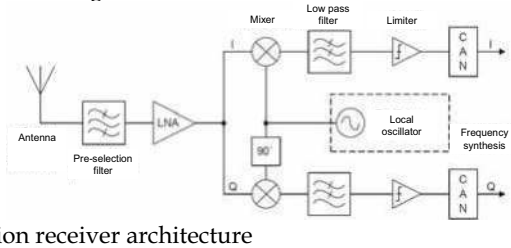

Fig. 3. Direct conversion receiver architecture

The solution adopted in the current work is a full CMOS zero-IF transceiver dedicated to very low cost and low power LR-WPAN applications and working at 2.4GHz frequency band as depicted in Figure 4. In this feature, multi-function phase locked loop (PLL) is used to synthesize 10 carrier frequencies corresponding to the transmission channels (2404 to 2488 MHz) and to modulate the data with frequency shift keying (FSK) scheme.

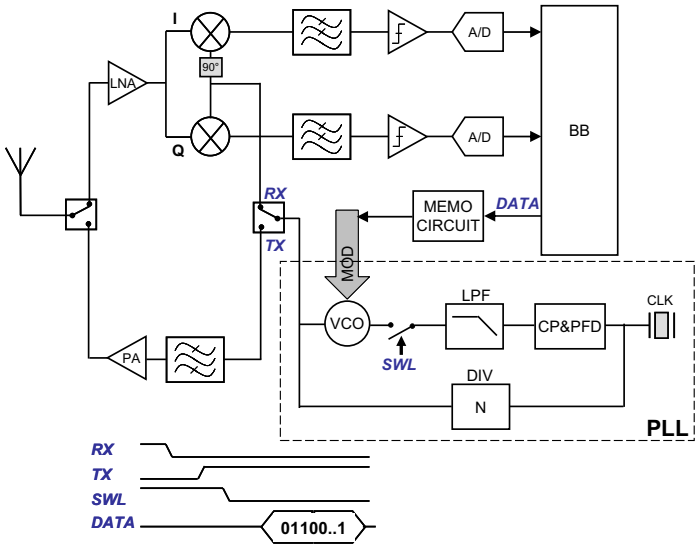

Fig. 4. IEEE 802.15.4 based transceiver architecture with direct conversion scheme.

The particularity of this solution remains in the fact that the PLL works with an open loop during the transmission mode. This provides the opportunity to completely turn off each bloc composing the PLL except the VCO and the modulation circuit allowing significant power reduction and simplify the transceiver architecture. Such simplification is possible with some modifications of the characteristics originally provided in the IEEE 802.15.4 standard including smaller channels number and therefore a larger width (10 channels of 8-MHz width), a maximum bit-rate of 125kbps and bit-error-rate (BER) of 10^{-3} instead of 50kbps and 6.10^{-5} respectively for IEEE 802.15.4.
This chapter will demonstrate the feasibility of low noise sensitivity 2.4GHz PLL for use in wireless communications in low cost LR-WPAN applications. Based on IEEE 802.15.4 specifications, this PLL is used both in a single conversion receiver as frequency synthesizer and in a direct conversion transmitter as a frequency shift keying (FSK) modulator. This multi-function low power and low cost system uses low-gain-multi-band Voltage Controlled Oscillator (VCO) which achieves a phase noise of -98dBc/Hz @ 1MHz offset while a lock time of 150µs has been obtained from the PLL loop. The circuits have been fully integrated and implemented in 130nm CMOS technology.

4. PLL design for mobile communications

In wireless communications, PLL may be used as frequency synthesizer or frequency modulation. The major challenge facing frequency synthesizer for mobile communication

devices is the need to increase their functionality in terms of operating frequency, frequency range to cover the desired operating frequency band and to accommodate process-voltage-temperature (PVT) variation, power consumption, modulation schemes while simultaneously meeting increasingly stringent linearity, phase noise and power consumption requirements at the same or lower cost. Phase locked loop (PLL) based frequency synthesizer for communication systems typically requires low phase noise and low reference spur PLLs that can be tuned over a wide range at GHz frequencies over process-voltage-temperature variations. Generally, ring oscillator ensures wide tuning range but comes with a much larger phase noise than their LC counterparts. A wide loop bandwidth is necessary to appropriately reject the high phase noise of the ring oscillator. But increasing the voltage controlled oscillator (VCO) tuning gain (K_{VCO}, in MHz/V) severally degrades the PLL phase noise and spurs performance. Meeting these conflicting requirements is the biggest challenge facing the development of future PLL modules.

4.1 Modulation circuit topology

FSK modulation has been adopted as it allows the use of power efficient, non linear RF power amplifier (McMahill & Sodini, 2002). The high tolerance to system linearity allows decreasing operating current and supply voltage. There is only a single frequency modulated carrier which is insensitive to amplifier non-linearities. Non-coherent demodulation meets the bit error rate performance requirements of this protocol and translates to simpler transceiver architectures, reducing the cost of the solution (Razavi, 1996; Razavi, 1997; Roden, 2003). Among the proposed solution in the literature concerning the frequency modulation, we can note four main methods, namely: i) sigma-delta (Σ-Δ) modulator (Huff & Draskovic, 2003; Pamarti et al, 2004), ii) two points FSK modulator (Neurauter et al, 2002), iii) Quadrature modulator and iv) two combined PLL with mixer modulator. In the very popular Σ-Δ modulation, the PLL synthesizer is directly modulated by varying the division value of the feedback divider with the output of the Σ-Δ modulator as shown in Figure 5.

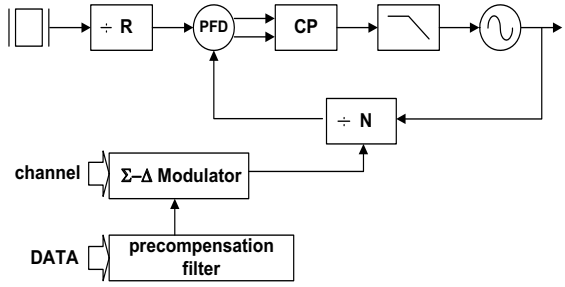

Fig. 5. Sigma-delta fractional PLL based frequency modulation

For high data rate modulation of few Mbits/s, (like DECT, CDMA2000, WCDMA), the PLL loop bandwidth (few decades of kHz) attenuates the high frequency data resulting to information lost. To overcome the limited modulation bandwidth, digital pre-emphasis filter is required (Huff & Draskovic, 2003; Pamarti et al, 2004). This operation is difficult to realize since a good matching between the analog transfer function of the PLL and the pre-emphasis digital transfer function must be ensured for proper operation. Moreover

fractional PLL is involved increasing the circuit complexity and cost. In order to bypass the loop bandwidth attenuation, more robust solution (see Figure 6) consists to apply the modulation signal at two distinct points: the low frequency signal at the Σ-Δ modulator that controls the PLL dividers while the high frequency signal is directly applied to the VCO input just after the loop filter.

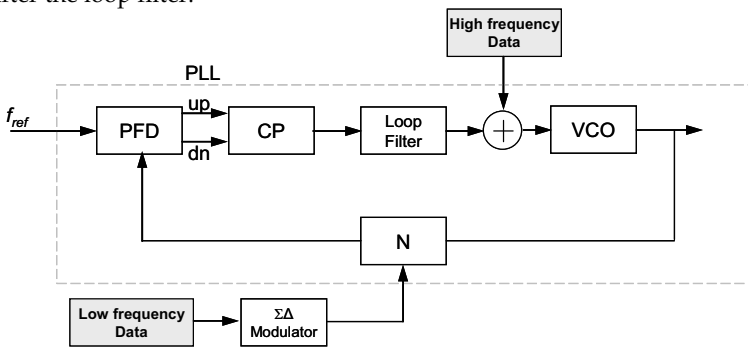

Fig. 6. GMSK two points modulation with fractional PLL

This solution requires stabilizing the VCO gain and the frequency versus temperature and process. The quadrature, or I-Q modulator, illustrated in Figure 7 is the most flexible one since any modulation type may be produced through correct choice of I(t) and Q(t) signals (McMahill & Sodini, 2002). The transmitted data sequence is processed digitally through a DSP and then converted to analog base band signal through a pair of digital-to-analog converters (DACs) to drive RF mixers whose local oscillator inputs are in quadrature. The price remains in terms of complexity and power consumption.

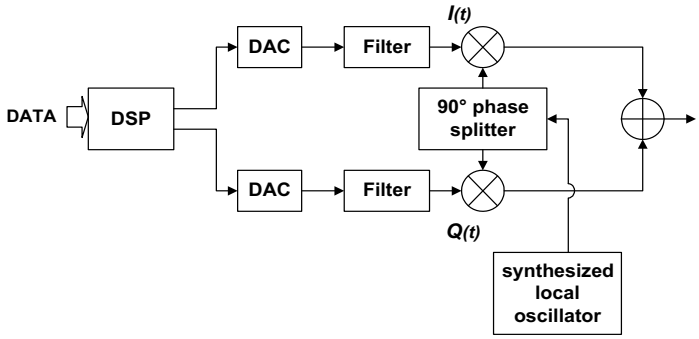

Fig. 7. Schematic of I-Q modulation method

The system illustrated in Figure 8 is a simple, low power and low cost, multi-function PLL used both in a single conversion receiver as frequency synthesizer and in a direct conversion transmitter as a frequency modulator. It can transmit or receive FSK modulated data in one of each ten 8MHz bandwidth channel and then is able to synthesize 30 frequencies from 2.404 to 2.488GHz with 2MHz step size with an open loop modulation of the VCO in the transmission mode. The modulation procedure is done in two steps: the first one is the calibration phase during which the loop is closed and the division factors are set to the first

then the second modulation frequencies. These values are injected into a memory module. The second step corresponds to the modulation phase during which the loop is opened and the data can be transmitted by directly modulating the VCO through the memory module. In terms of power consumption point of view, significant power saving is done during the transmission mode. In addition, thanks to the open loop, this modulation is not sensitive to the PLL bandwidth. However, the free running VCO is subjected to temperature, process drift and noise. The quality of the transmitted signal directly depends on its quality. During the emission phase, the entire parasitic spectrums are also amplified by the power amplifier. In order to lower the VCO sensitivity to the input noise, low gain PLL has been chosen. In fact, this solution is a simple and an efficient one for the current purpose where good signal-to-noise ratio, low phase noise and sufficiently low frequency drift are mandatory to guarantee the integrity of the emitted data. However, decreasing the conversion gain of the VCO leads to lower frequency tuning range and several VCOs are required so as to cover the entire frequency band of the transmission channels and to overcome the PVT drift. Unfortunately, this solution is not suitable for low cost, low power design requirement. In order to meet these open loop modulation constraints, new VCO topology has been proposed.

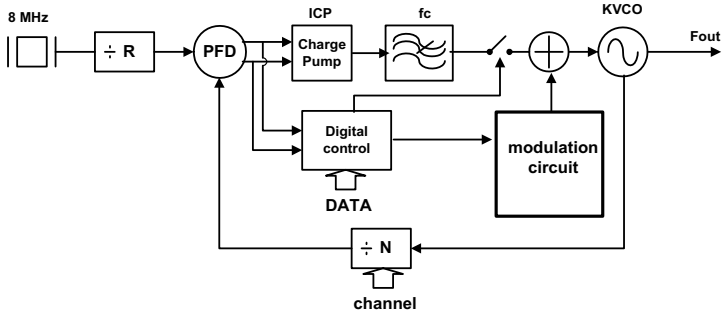

Fig. 8. Schematic of the 2.4GHz PLL and the modulator

4.2 PLL noise versus gain

The non ideality of the signal at the output of the PLL results from several design parameters. The most significant one comes from the phase noise of the VCO. But any other elements composing the PLL participates to noise degradation, the frequency divider, the noise generated by the loop filter components (thermal noise of resistors, 1/f-noise from active components), the jitter resulting from the current peak at the output of the charge-pump. Moreover, the charge-pump mismatch leads to PLL lock time degradation. Generally, PLL with a high gain generates higher noise and jitter than PLL working with lower gain. There are many solutions given in the literature in order to increase the accuracy of the synthesized frequencies. Most of them are based on the adaptive bandwidth technique (Lee & Kim, 2000; Lim et al, 2000; Vaucher, 2000) or a variant of this one. The principle is based on the modulation of the PLL bandwidth by acting on the charge-pump current together with the loop filter configuration. In fact, a closed-loop PLL can be assimilated to a low pass filter that the loop bandwidth is correlated to the PLL speed. Increasing the bandwidth can speed-up the PLL lock time, but the input noises are less filtered and degrade the spectral purity of the synthesized frequency. The adaptive

bandwidth technique is a good compromise between the PLL speed and the noise. Unfortunately this technique requires the PLL works with a closed-loop configuration and is not an efficient one if an open loop mode is required.
The solution we propose allows to solve this problematic. In fact, we propose to maintain a high charge-pump current in order to guarantee rapid lock time, while the VCO conversion gain will be decreased. The gain of individual element contributes to the overall gain in the PLL circuit where the open loop transfer function can be written such as

$$OL(s) = \frac{K\Phi \cdot K_{VCO} \cdot Z(s)}{s} \tag{1}$$

where $K\Phi$ is the charge-pump gain, K_{VCO} is the conversion gain of the VCO, $Z(s)$ is the loop filter transfer function. Reducing the gain of VCO will lead to a reduction of the frequency tuning range and results in a less versatile PLL circuit. The gain of the charge-pump also contributes to overall gain (and jitter) of PLL circuit. However, charge-pump with lower gain will lock more slowly than a high gain charge-pump and even prevent lock from being achieved at all. Let us assume a linear transfer function of a given VCO belonging to a frequency synthesizer system such as

$$F = K_{VCO} \times (V_0 + Vnoise) = F_0 + (K_{VCO} \times Vnoise) \tag{2}$$

where $F_0 = K_{VCO} \times V_0$ is the center frequency of the VCO, *Vnoise* is the equivalent noise at the input of the VCO which is not filtered by the loop filter. The term $K_{VCO} \times Vnoise$ conducts to phase noise degradation of the synthesizer that directly depends on the conversion gain value. Since low gain VCO is adopted, resulting in low frequency band, more than one should be necessary in order to cover the frequency range of the system. The corresponding transfer function is illustrated in Figure 9, where the required band is ΔF with an overall VCO gain K_{VCO}. Decreasing the gain by a ratio of n reduces the noise sensitivity with the same factor, but n VCO having this low gain (K_{VCO}/n) should be required. The price remains in terms of silicon area, power consumption and circuit complexity.

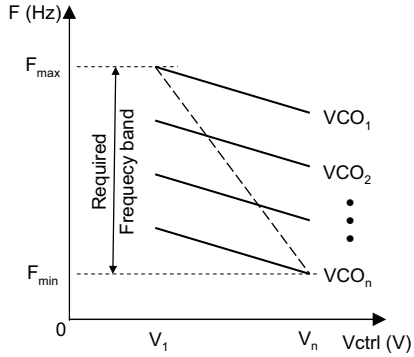

Fig. 9. Transfer function illustrating VCO conversion gain

5. Implementation of the solution

5.1 Low gain-wide-range VCO

A VCO is characterized by its operating frequency, its tuning range, its spectral purity, its power consumption, but one of the critical parameter is the phase noise. In wireless communications, phase noise requirement comes from different considerations such as interferer strength and the modulation scheme. For example, IEEE 802.11a standard (IEEE std 802.11a, 1999) uses Orthogonal Frequency Division Multiplexing (OFDM) based modulation scheme which is more sensitive to phase noise compared to single carrier modulation schemes, e.g., GMSK used in HYPERLAN Standard or FSK in LR-WPAN. Let us give an example: for a low data-rate of 125kbits/s, the current design uses FSK modulation scheme in a 4MHz channel bandwidth. Supposing –70dBm receiver sensitivity and an adjacent interferer 35dB stronger than the desired channel, the VCO phase noise needs to be lower than: PN=-35-10log(4MHz)-20 =-122dBc/Hz, assuming a predetection signal-to-noise ratio (SNR) of 20dB for a BER of 10^{-3}. This translates to a phase noise of –87dBc/Hz @ 1MHz offset. This value is reduced down to -107dBc/Hz @ 1MHz offset for the IEEE 802.11 standard (Bhattacharjee et al, 2002) where the highest data-rate equals 54Mbps using 64-QAM with OFDM in 20MHz channel bandwidth.

LC-VCO exhibits lower phase noise than its ring VCO counterpart for the same power consumption (Hajimiri, 1998; Hajimiri, 1999). Good phase noise is obtained from the high quality factor of the used inductance. Unfortunately, inductance is difficult to integrate and is area consuming; moreover its frequency control is performed thanks to a varicap diode leading to a poor frequency tuning range. In order to meet the low area requirement of the current application, ring oscillator has been chosen to implement the solution. Rather than utilizing several low gain VCOs, a solution based on single circuit that emulates the functionality of numerous VCO has been proposed. The VCO is composed by only two delay cells for an optimal integration and the corresponding schematic as given in Figure 10

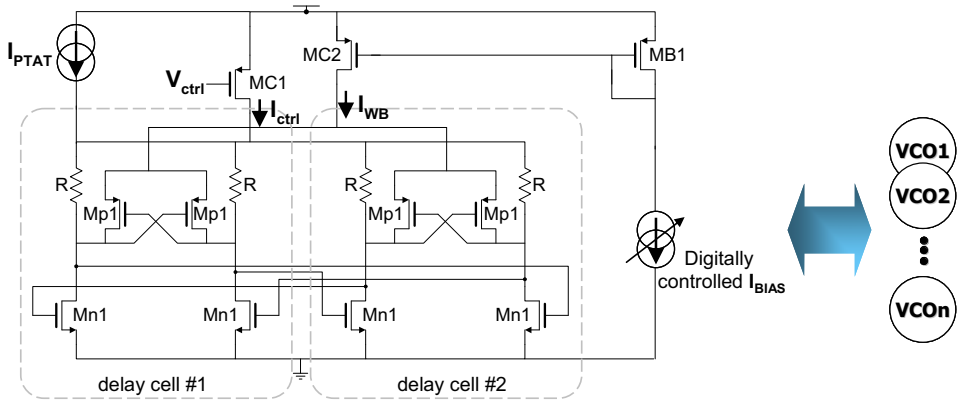

Fig. 10. Schematic of low gain wide range VCO

The circuit operation is as following. The frequency control is achieved by adjusting the transconductance (gmC) of the transistor MC1. Constant current is injected via resistor R in the differential pair Mn1. Therefore, any variation of the cross-coupled pair Mp1 transconductance (gmp1) is reported to that of Mn1 (gmn1). The bias current through the

resistors R provides an opportunity to adjust the ratio gmn1/gmp1. According to Barkhausen criteria, to maintain oscillation, the total phase of the chain has to be 360° under unity gain. At high frequencies, the current waveform may be approximated more closely by a sinusoid due to finite switching time and limited gain; as a consequence, the study can be approximated with linear model. In this condition, the oscillation frequency extracted from the delay cell related transfer function may be written as

$$f_{osc} = \frac{1}{2\pi}\sqrt{\frac{g_{mn1}{}^2 - \left(\frac{1}{R_{eq}} - g_{mp1}\right)^2}{C_{eq}{}^2 - C_{gdn1}{}^2}} \tag{3}$$

where R_{eq} is the equivalent resistance formed by R and the drain to source resistor of Mn1 and Mp1, C_{eq} represents the sum of drain to bulk and the gate to source capacitances C_{dbn1}, C_{dbp1} and C_{gsp1} of Mn1 and Mp1 respectively. As shown in (3) the output frequency directly depends on g_{mn1} and g_{mp1}. Neglecting the Early effect, the transconductance of Mn1 and Mp1 can be expressed as

$$g_{mn1} = \left[2\mu_n C_{ox}\frac{W}{L}\left(I_{bias} + I_{ctrl} + I_{WB}\right)\right]^{\frac{1}{2}} \tag{4}$$

$$g_{mp1} = \left[2\mu_p C_{ox}\frac{W}{L}\left(I_{ctrl} + I_{WB}\right)\right]^{\frac{1}{2}} \tag{5}$$

where I_{ctrl} is the current generated by the frequency tuning transistor MC1 working in ohmic regime while I_{WB} results from the programmable band selection derived from the digitally controlled current source bias, which is correlated with the channel frequency given by the digital control part of the system. Such a structure gives a possibility to emulate several low gain VCOs while covering the whole operating frequency band. The value of the VCO gain is imposed by the open loop operating mode where the effect of the voltage control drift and noise must be minimized. A VCO gain of 50MHz/V has been chosen for the current application.

5.2 Temperature compensation

During the modulation phase, the VCO is free running, and no control from the PLL loop will be applied to correct the output frequency drift from the PVT variations. Consequently, temperature compensation should be realized. The circuit topology given in Figure 10 provides the opportunity to allow double and independent frequency control. The first input is voltage controlled (gate of MC1); it corresponds to the functional input and is dedicated to transceiver parameters (action on the transconductance $g_{mn}(T)$ of Mn1 and $g_{mp}(T)$ of Mp1). The second one is current controlled (I_{PTAT} through the resistor R); it is the calibration input and is dedicated to the physical parameters (process, temperature). For the current application, it is used for temperature compensation by injecting it a temperature dependent biasing current (I_{PTAT}). In this way, the temperature control acts only on g_{mn}(T), making the calibration of the compensation level extremely simple and allowing a good temperature compensation (Rahajandraibe et al, 2007).

5.3 Main loop design

The proposed PLL, illustrated in Figure 11, has been designed in the context of the current work. It is based on the charge-pump (CP) architecture.

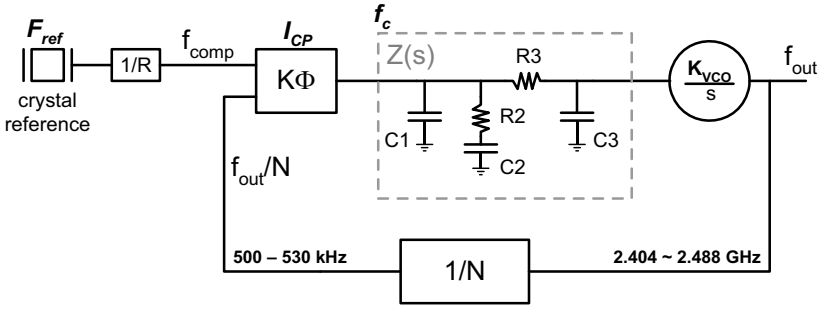

Fig. 11. PLL modeling

The 3rd order passive loop filter has been adopted in order to minimize the spurious gain, under the constraints of a constant loop bandwidth and phase margin. Its transfer function in the frequency domain can be written as

$$Z(s) = \frac{1 + s \cdot \tau_2}{s \cdot C_{tot}(1 + s \cdot \tau_1)(1 + s \cdot \tau_3)} \tag{6}$$

where C_{tot}=*C1+C2+C3*, τ is the time constant such as $\tau 1$=*R2C2C1*/C_{tot}, $\tau 2$=*R2C2* and $\tau 3$=*R3C3*. Starting from (1), the closed-loop (CL(s)) transfer function can be expressed as

$$CL(s) = \frac{N \cdot K\Phi \cdot K_{VCO} \cdot Z(s)}{s \cdot N + K\Phi \cdot K_{VCO} \cdot Z(s)} \tag{7}$$

which can be approximated by the following second order expression

$$CL_2(s) = \frac{\left(\frac{K\phi \cdot K_{VCO}}{N \cdot C_{tot}}\right) \cdot (1 + s \cdot N \cdot \tau_2)}{s^2 + s \cdot \left(\frac{K\phi \cdot K_{VCO} \cdot \tau_2}{N \cdot C_{tot}}\right)} \tag{8}$$

Defining the natural pulsation ω_n and the damping factor ξ as

$$\omega_n = \sqrt{\frac{K\Phi \cdot K_{VCO}}{N \cdot (C1 + C2 + C3)}} \quad \text{and} \quad \zeta = \frac{R2 \cdot C2}{2} \cdot \omega_n \tag{9}$$

and using inverse Laplace transforms, the time frequency response is obtained, from which the lock time of the PLL is derived as

$$LockTime = \frac{-\ln\left(\frac{tol}{f_2 - f_1} \cdot \sqrt{1 - \zeta^2}\right)}{\zeta \cdot \omega_n} \tag{10}$$

where f_2-f_1 is the frequency step, and *tol* corresponds to the maximum tolerance of the frequency at which the PLL is supposed to be locked. Each parameter of the PLL has to be chosen optimally in order to achieve low noise VCO, low power consumption, and fully integration of the loop filter capacitors. The design parameters have been calculated to meet a lock time of 150µs. That is a VCO gain of 50MHz/V, a charge-pump current ICP=3.5mA, a loop filter bandwidth of 32KHz with the following filter components: C1=10pF, C2=120pF, R2=40kΩ, C3=4pF, R3=100kΩ. The theoretical lock time computed from these values is 96µs.

6. Experimental results

In order to validate the design, test chip has been realized with 130nm CMOS technology including the entire digital and analog functional bloc composing the PLL (frequency divider, phase/frequency detector, charge-pump, loop filter, VCO, prescaler and digital blocs). A separated test chip has been implemented in the same technology for the multi-band VCO that provides the opportunity to define its intrinsic characteristics.

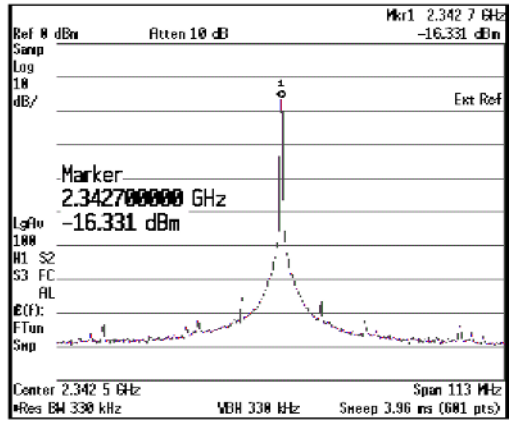

Fig. 13. Output spectrum of the low gain multiband VCO

During the modulation phase, the VCO is free running and must have sufficiently low noise and low frequency drift. The output spectrum of the free-running VCO measured with a spectrum analyzer Agilent E4446A is given in Figure 13. It exhibits an output power of -16dBm at 2.34GHz. The phase noise profile measured on the same VCO exhibits -96dBc/Hz @ 1MHz offset from the carrier. Although this value is lower than that can be achieved with an LC-VCO (-115 to -130dBc/Hz) it presents sufficient margin in view of most of the standard value required for low data rate wireless applications which, for the current application, is fixed at -87dBc/Hz @ 1MHz offset.

Figure 14 depicted the VCO output frequency tuning range as a function of the control voltage and for different configuration of the digitally programmable current source. The frequency range is shown for 10 different channels. VCO gain of 30 to 50 MHz/V is obtained for channel 1 to channel 10. Such a transfer function is equivalent to an overall gain of 90 to 100MHz/V. Lower VCO gain is obtained but the achieved performance is suitable for the current application.

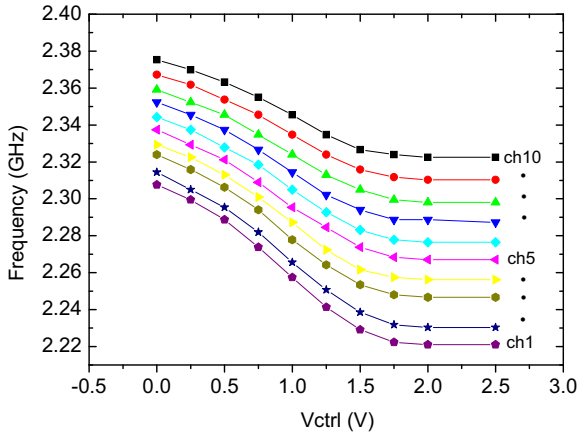

Fig. 14. Measured frequency tuning range of the VCO

The PLL has been designed and implemented in 130nm CMOS technology. A mean lock time of 100µs has been achieved when the circuit is waked up from the sleep mode to an active mode. A settling time of 36µs (see Figure 15) and 50µs are obtained between channels 1 to 2 and channels 1 to 10 respectively.

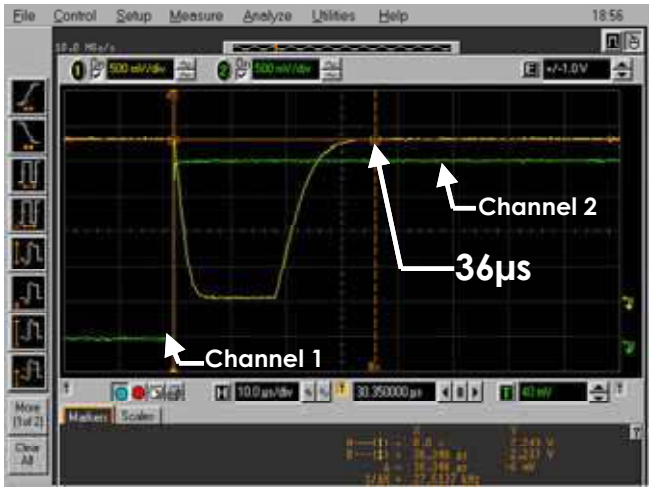

Fig. 15. Measured PLL lock time from sleep mode

A total power consumption of 34mA is obtained under a supply voltage of 2.5V. The duration of the longest pattern is 11ms. During the reception mode, the total energy consumption of the PLL equal 308µAh, however, during the transmission mode, the maximum consumption occurs only during the short locking time of the PLL, after which, the loop is opened and the data modulates directly the VCO through memory model. All the blocks are switched off except the VCO and the modulation circuit. Consequently, the system consumption is lowered down to 187µAh which represents a gain of 40%.

7. Conclusion

After arrival on the market in recent years of several wireless local area networks such as WiFi, Bluetooth, HYPERLAN and so on, news technology also appears promising a bright commercial future for both applications in public domain such as those related to home automation, and for more related field wireless communications in industrial environments: such as the ZigBee network. This WPAN network differs from its two main competitors previously cited from its simplicity of implementation and its low power consumption. ZigBee technology, coupled with the IEEE 802.15.4 standard offers simple protocol which can be declined in several versions depending on the requirement and the desired topology, for purposes of low data rate and weak of use of the medium. This article demonstrates the feasibility of high performance frequency synthesizer for this purpose. The accuracy of the output frequency is guaranteed by the low gain of the VCO without penalizing the time response (lock time) nor the frequency operating range. The design has been implemented on low cost standard CMOS technology. The proposed topology allows to realize much lower gain if it is required with a very simple calibration method.

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Mobile and Wireless Communications Network Layer and Circuit Level Design

Edited by Salma Ait Fares and Fumiyuki Adachi

ISBN 978-953-307-042-1
Hard cover, 404 pages
Publisher InTech
Published online 01, January, 2010
Published in print edition January, 2010

Mobile and wireless communications applications have a clear impact on improving the humanity wellbeing. From cell phones to wireless internet to home and office devices, most of the applications are converted from wired into wireless communication. Smart and advanced wireless communication environments represent the future technology and evolutionary development step in homes, hospitals, industrial, vehicular and transportation systems. A very appealing research area in these environments has been the wireless ad hoc, sensor and mesh networks. These networks rely on ultra low powered processing nodes that sense surrounding environment temperature, pressure, humidity, motion or chemical hazards, etc. Moreover, the radio frequency (RF) transceiver nodes of such networks require the design of transmitter and receiver equipped with high performance building blocks including antennas, power and low noise amplifiers, mixers and voltage controlled oscillators. Nowadays, the researchers are facing several challenges to design such building blocks while complying with ultra low power consumption, small area and high performance constraints. CMOS technology represents an excellent candidate to facilitate the integration of the whole transceiver on a single chip. However, several challenges have to be tackled while designing and using nanoscale CMOS technologies and require innovative idea from researchers and circuits designers. While major researchers and applications have been focusing on RF wireless communication, optical wireless communication based system has started to draw some attention from researchers for a terrestrial system as well as for aerial and satellite terminals. This renewed interested in optical wireless communications is driven by several advantages such as no licensing requirements policy, no RF radiation hazards, and no need to dig up roads besides its large bandwidth and low power consumption. This second part of the book, Mobile and Wireless Communications: Key Technologies and Future Applications, covers the recent development in ad hoc and sensor networks, the implementation of state of the art of wireless transceivers building blocks and recent development on optical wireless communication systems. We hope that this book will be useful for students, researchers and practitioners in their research studies.

How to reference

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Wenceslas Rahajandraibe, Lakhdar Zaid and Fayrouz Haddad (2010). Fully Integrated CMOS Low-Gain-Wide-Range 2.4 GHz Phase Locked Loop for LR-WPAN Applications, Mobile and Wireless Communications Network Layer and Circuit Level Design, Salma Ait Fares and Fumiyuki Adachi (Ed.), ISBN: 978-953-307-042-1, InTech, Available from: http://www.intechopen.com/books/mobile-and-wireless-communications-network-layer-and-circuit-level-design/fully-integrated-cmos-low-gain-wide-range-2-4-ghz-phase-locked-loop-for-lr-wpan-applications

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