2

CMOS and BiCMOS Regenerative Logic Circuits

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1. Introduction

Schmitt triggers with standard CMOS logic circuits are described, first. Mathematical models for calculating basic parameters and their limits are presented. Most of the chapter is dedicated to different solutions for CMOS and BiCMOS Schmitt logic circuits in monolithic integrated circuits. Two types of inverters with entirely different topologies are described. Also, solutions for Schmitt triggers with voltage-controlled thresholds are described. Beside inverters, NAND and NOR Schmitt logic circuits are analyzed. Basic circuit is inverted Schmitt trigger with three pairs of CMOS transistors. Expansion of the number of inputs is reached in a similar way as in standard CMOS and BiCMOS logic circuits. It is shown that voltage transfer characteristics depend, beside voltage supply and parameters of transistors, on the number of logical circuits' inputs. NAND and NOR Schmitt circuits, in which voltage hysteresis in transfer characteristic is generated only through one input, are also described. Analytic models and SPICE simulations are used for analysis of static and dynamic parameters and conditions for work stability and reliability. Areas of reliability, influence of technology and electrical parameters of transistors and their limits are analyzed.
Concerning the field of application, in literature there are different solutions of Schmitt triggers (Zou et al, 2008, Al-Sarrawi, 2008, Katyal et al, 2008, Lo et al, 2010). In this chapter, solutions with fundamental applications in digital integrated circuits – Schmitt logic circuits are described. The author published most of these solutions (Dokic, 1983, Dokic 1984, Dokic 1996, Dokic, 1988). Today, some of them (Dokic, 1984) are treated as conventional.
The term regenerative is used because every change of state is followed by a regenerative process – positive feedback. Owning to that, transfer characteristic has shape of a hysteresis, like in Schmitt trigger. That is why the term Schmitt logic circuits is most commonly used. Unlike conventional logic circuits, where the output level is uniformly determined for the input voltage value, for Schmitt logic circuits, in certain extent, it is not uniformly determined. In fact, due to hysteresis, in the area of the input voltages between two logic thresholds, logic state at the output depends, beside the input voltage value, also on the previous state. Due to that Schmitt circuits can be used as filters for low frequency interferences. An example of this kind of application is given in Fig.1.
Whenever the value of the input signal passes the value of the threshold voltage V_T of the standard logic circuit, a change of the logic state at the output appears. Therefore, the changes of the input voltage created by noise are transferred to the output as glitches. The change of the logic state at the output of the Schmitt logic circuit can appear only after the noise amplitude of which is greater than the voltage hysteresis.

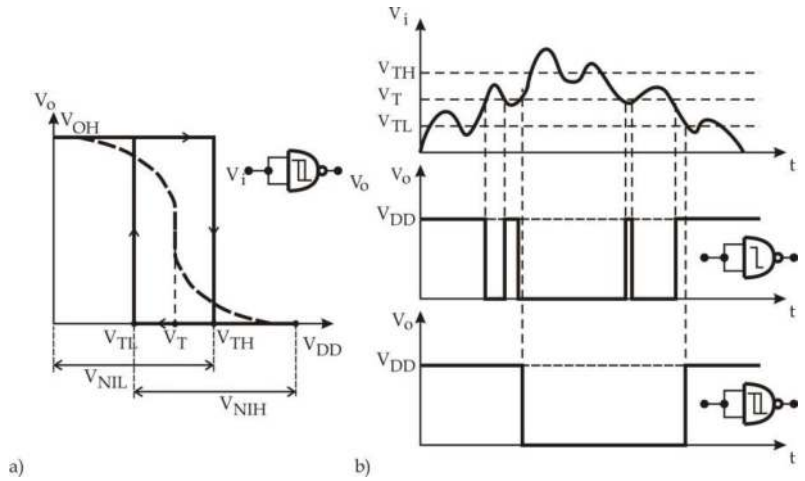


Fig. 1. Transfer characteristic of Schmitt logic circuit (a) and outputs of standard and Schmitt circuit to an input with noise addition (b).

Schmitt trigger is able to hold it's logic state for all changes of the input voltage which are $V_{TL} < V_i < V_{TH}$, where V_{TH} and V_{TL} are the high and the low threshold of the Schmitt trigger. Fig.1 shows the ability of the Schmitt trigger to filter the noise, which, in this case, do not influence the output of the circuit. At the same time at the output of the standard circuit there are two pulse glitches which create system errors.

The hysteresis within the transfer characteristic causes increase of the static noise immunity (Fig.1a). Thus:

$$V_{NIL} = V_{TH}, \tag{1}$$

$$V_{NIH} = V_{DD} - V_{TL} \tag{2}$$

Comparing Schmitt triggers to the standard circuits, the increase of the static noise immunity appears if the threshold voltage V_T of the standard gate lies between the thresholds of the Schmitt circuit, i.e.:

$$V_{TL} < V_T < V_{TH} \tag{3}$$

The transfer characteristic, concerning the noise immunity, is optimum if the thresholds V_{TH} and V_{TL} are symmetric around $V_{DD}/2$. The larger the value of the voltage hysteresis becomes, the noise immunity increases further. The transfer characteristic of the CMOS Schmitt gates is almost perfectly symmetric around $V_{DD}/2$.

There is another advantage of Schmitt circuits compared to the standard ones. Because of the positive feedback, the transfer characteristic is ideal, which means that values of noise margin and noise immunity are equal. Schmitt triggers are used to shape pulses or convert signals that change slowly into pulse signals with short rise and fall times, which is necessary where synchronizing circuits are used. These are the reasons to use Schmitt triggers so often, both as an independent integrated circuit and as a part of a MSI or VLSI circuit. In the second case, Schmitt trigger is almost always used as an input circuit. Also,

integrated circuits with mixed signals contain Schmitt triggers (Young, 2010, Chien, 2011, Li, 2009, Hard & Voinigesku, 2009, Wang et al, 2008, Arrabi 2011).

2. Schmitt trigger with logic circuits

The basic Schmitt trigger consists of two CMOS inverters and two resistors (Fig.2).

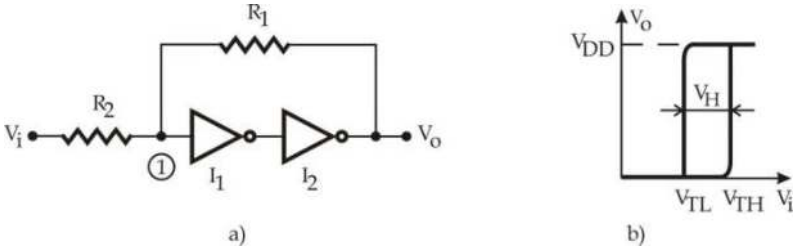


Fig. 2. Schmitt trigger (a) and it's transfer characteristic (b).

The high threshold V_{TH} and the low threshold V_{TL} are defined by the supply voltage V_{DD}, ratio of the resistors R_1/R_2 and the threshold voltage V_T of the inverter I_1. Namely,

$$V_{TH} = V_T\left(1 + R_1 / R_2\right) \tag{4}$$

$$V_{TL} = V_T\left(1 + R_1 / R_2\right) - V_{DD}R_1 / R_2 \tag{5}$$

and voltage hysteresis is given by:

$$V_H = V_{TH} - V_{TL} = V_{DD}R_1 / R_2 \tag{6}$$

where V_T is given by:

$$V_T = \frac{V_{DD} + V_{tp} + V_{tn}\sqrt{k_n / k_p}}{1 + \sqrt{k_n / k_p}} \tag{7}$$

V_{tn} and V_{tp} are threshold voltages of nMOS and pMOS transistors, respectively, and the constants of transistors are given by:

$$k_n = \frac{\mu_n \varepsilon_{ox}}{2t_{ox}} W_n / L_n\,,\; k_p = \frac{\mu_p \varepsilon_{ox}}{2t_{ox}} W_p / L_p \tag{8}$$

where μ_n and μ_p are the mobility of the electrons and the holes, ε_{ox} is oxide dielectric constants, t_{ox} the oxide thickness and W and L are width and length of the transistor's channel.

The fact that basic parameters depend on the ratio of the resistance R_1/R_2 yields a wide choice of their absolute values. These values range from several tens of $k\Omega$ ($R_1 + R_2 \gg R_O$, where R_O represents output resistance of the inverter I_2), to several hundreds of $M\Omega$. On the other hand, their ratio can vary within a broad range. Since it is always true: $V_H < V_{DD}$, then $R_1 < R_2$. The other limitations do not exist, it is possible for the ratio to be $R_1/R_2 \ll 1$. This

means that the voltage hysteresis can be regulated in a very wide range, from several tens of mV to, approximately, V_{DD}.

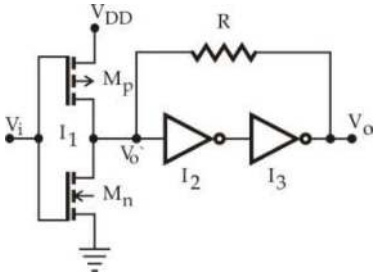


Fig. 3. Schmitt trigger with one resistor (Dokic, 1983).

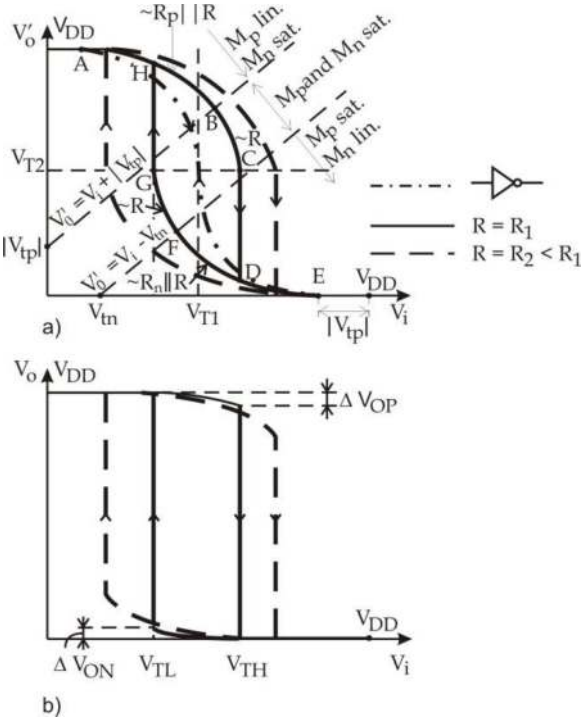


Fig. 4. Characteristics $V_o'(V_i)$ and $V_o(V_i)$ for two values of R.

Another kind of Schmitt trigger which uses discrete CMOS logic circuits (Fig.3) contains three inverters and only one resistor (Dokic, 1983). The advantage of this circuit comparing to the previous one is that it has a CMOS input (very high input resistance). The disadvantage is that the range available for tuning voltage hysteresis is narrower. The resistor R decreases the amplification of the input inverter in the transitional area and moves the characteristic $V_o'(V_i)$ to the right if V_i increases, or to the left if V_i decreases (Fig.4a).

Because of this process, the transfer characteristic is the shape of the hysteresis. In Fig.4a transfer characteristic $V_o' = f(V_i)$ is shown. With line-dot-line, in this same Fig., the transfer characteristic of the inverter I_1 without the resistor R (in other words: $R \to \infty$) is presented.
Let V_i increase from 0 to V_{DD}. Before change of the logic state ($V_i < V_{TH}$) the output of the circuit is $V_o = V_{DD}$, thus R and M_p are connected in parallel (Fig.5a). The slope of the function $V_o' = f(V_i)$ in AB area is determined by the resistors connected in parallel, $R_p||R$, where R_p represents resistance of the drain-source of M_p within the linear area of the characteristic. Between the points B and C, where both M_p and M_n are saturated, slope depends only on R. The change of the logic state appears when:

$$V_o^{'} = V_{T2} \tag{9}$$

where V_{T2} is threshold voltage of the inverter I_2. At this moment the change (fall) of the voltage V_o appears, which is, through the resistor R, transferred to V_o', thus decreasing V_o' even more. In this way positive feedback loop is created which leads to step change of V_o' (area between the points C and D), and thusly of V_o.
In the beginning of the process of which the result is change of V_i from V_{DD} to 0, R and the transistor M_n are connected in parallel (Fig.5b). The change of the logic state also appears if the condition (9) is fulfilled.

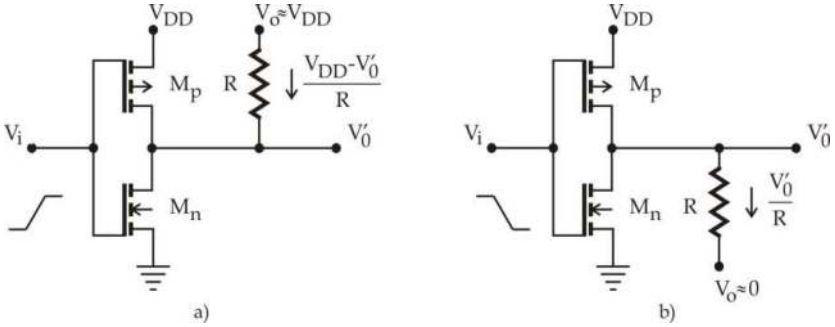


Fig. 5. Equivalent scheme of the circuit for determining V_{TH} (a) and V_{TL} (b).

2.1 Determining the high threshold voltage V_{TH}

The change of V_o' between the points A and C is determined from:

$$I_{Dn} = I_{Dp} + \frac{V_{DD} - V_o^{'}}{R} \tag{10}$$

where I_{Dn} and I_{Dp} represent the drain currents of the transistors M_n and M_p, respectively. During these calculations the working areas of the transistors need to be noted – these are clearly shown in Fig.4. Of special interest is the area BC in which both M_n and M_p are saturated, because that is where the logic state is changed in the circuit. In this area:

$$k_n\left(V_i - V_{tn}\right)^2 = k_p\left(V_{DD} + V_{tp} - V_i\right)^2 + \frac{V_{DD} - V_o^{'}}{R} \tag{11}$$

which leads to:

$$V_o^{'} = V_{DD} - k_p R\left[\frac{k_n}{k_p}\left(V_i - V_{tn}\right)^2 - \left(V_{DD} + V_{tp} - V_i\right)^2\right] \tag{12}$$

Practically, inverters are symmetric, or almost symmetric, circuits. That is why we, in further text, consider such a case: $k_n = k_p$ and $V_{tn} = |V_{tp}|$ of all transistors. Then (12) can be written as:

$$V_o^{'} = V_{DD}\left[1 + k_p R\left(V_{DD} + 2V_{tp}\right)\right] - 2k_p R\left(V_{DD} + V_{tp} - V_{tn}\right)V_i \tag{13}$$

and the condition of change of the output voltage becomes:

$$V_o^{'} = V_{DD} / 2 \tag{14}$$

When $V_o' = V_{DD}/2$, then $V_i = V_{TH}$, so, taking into account (13) and (14), the high voltage of the Schmitt trigger is given by:

$$V_{TH} = \frac{V_{DD}}{2} + \frac{V_{DD}}{4k_p R\left(V_{DD} + V_{tp} - V_{tn}\right)} \tag{15}$$

2.2 Determining the low threshold voltage V_{TL}

Equivalent circuit used to determine V_{TL} is shown in Fig.5b. Then:

$$I_{Dp} = I_{Dn} + V_o^{'} / R \tag{16}$$

Between points F and G both transistors are saturated, so:

$$k_p\left(V_{DD} + V_{tp} - V_i\right)^2 = k_n\left(V_i - V_{tn}\right)^2 + V_o^{'} / R \tag{17}$$

Presuming that the transistors are symmetric, (17) leads to:

$$V_o^{'} = k_n R\left(V_{DD} + V_{tp} - V_i\right)\left(V_i - V_{tn}\right) \tag{18}$$

Combining (14) and (18) and replacing $V_i = V_{TL}$, low threshold voltage is given by:

$$V_{TL} = \frac{V_{DD}}{2} - \frac{V_{DD}}{4k_n\left(V_{DD} + V_{tp} - V_{tn}\right)R} \tag{19}$$

Voltage hysteresis is:

$$V_H = V_{TH} - V_{TL} = \frac{V_{DD}}{2k_p\left(V_{DD} + V_{tp} - V_{tn}\right)R} \tag{20}$$

From the previous analysis, the following conclusions are derived:

- the thresholds are symmetric relative to $V_{DD}/2$;
- V_{TH}, V_{TL} and V_H are inversely proportional to R.

The dependency of the thresholds V_{TH} and V_{TL} on R and V_{DD} is shown in Fig.6.

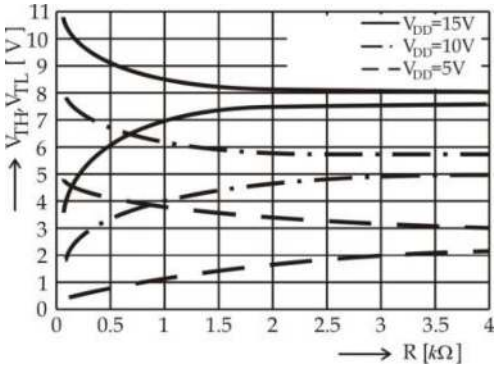


Fig. 6. The high and the low threshold voltages as functions of R and V_{DD}.

The resistance R should be within the range from several hundreds of Ω up to several $k\Omega$. Sensivity of the threshold change decreases if R increases. If $R > 3k\Omega$, this sensitivity is very low.

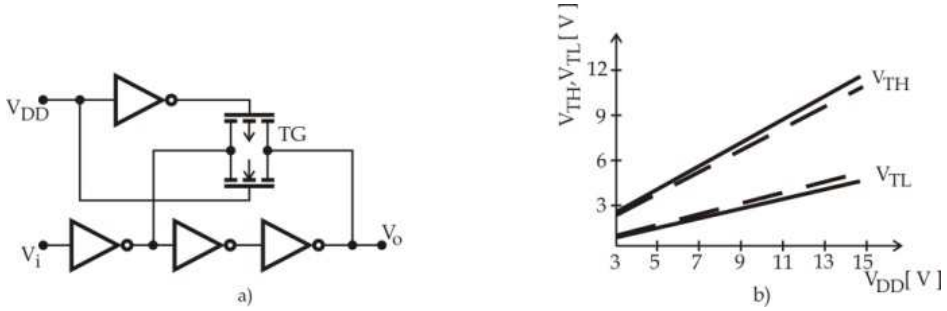


Fig. 7. Schmitt trigger with transmission gate instead of the resistor (a) and the dependency of the high and low threshold voltages on the supply voltage (b).

Instead of resistor R the transmission gate can be used (Fig.7a). The control input of the transmission gate should be in the logic state which keeps it on all the time. In this case, TG acts as a resistor whose resistance depends on the type of TG and the supply voltage. In Fig.7b the dependency of threshold voltages on the supply voltage V_{DD} is shown, if the inverters are CD4069, and TG is CD4066 (full line) or CD4016 (broken line). The resistance of the TG CD4066 is lower, thus the voltage hysteresis of the Schmitt trigger is wider in this case, than when CD4016 is used.
If NAND and NOR logic circuits are used instead of input inverters in Fig.3 and 7a the NAND and NOR Schmitt trigger are obtained.

3. Schmitt trigger – inverter

The basic circuit is the Schmitt trigger – inverter with three pairs of CMOS transistors (Fig.8). This solution has been initially proposed in (Dokic, 1984), which is the most

widely cited single-ended Schmitt trigger (Young, 2010). Transistors M_n and M_p form the standard CMOS inverter I (Fig.8b). In wider part of the transfer characteristic transistors M_{n0}, M_{n1} and M_{p0}, M_{p1} are operating as the inverting nMOS and pMOS amplifier, respectively.

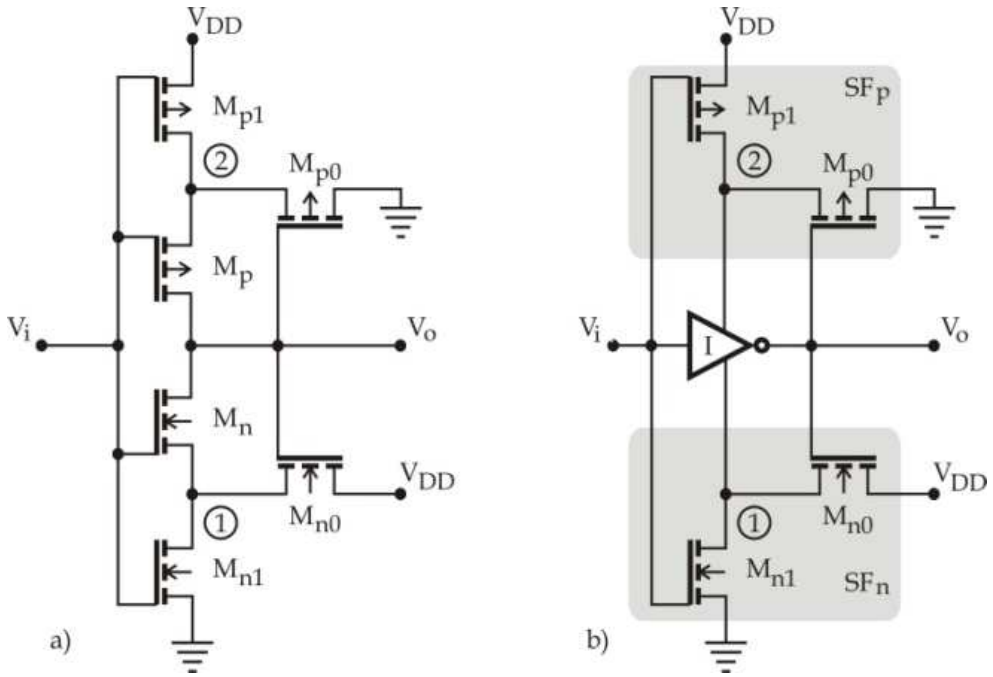


Fig. 8. Inverting Schmitt trigger (a) and it's equivalent (b).

The inverter of nMOS type enlarges the value of input voltage at which M_n turns on, when input voltage increases, and the inverter of pMOS type decreases the value of input voltage at which M_p turns on, when input voltage decreases. Because of this process, the transfer characteristic has the shape of hysteresis. When output voltage V_o changes, nMOS and pMOS inverters have the function of source followers, and through them positive feedback loop is created. They also introduce hysteresis by feeding back the output voltage to points 1 and 2.

To describe the circuit, assume the threshold voltages of all nMOS and pMOS transistors are V_{tn} and V_{tp}, respectively. Constants k of the transistors M_{n0} and M_{p0} are k_{n0} and k_{p0}, and constants k of the other nMOS and pMOS transistors are k_n and k_p, respectively.

For $V_i = 0$, M_n, M_{n1} and M_{p0} are off, and M_p, M_{p1} and M_{n0} are on. Output voltage is V_{DD}. Voltage of point 1 is $V_1 = V_{DD} - V_{tn0}$, because M_{n2} is on and saturated ($V_{GDn0} = 0$). Because of this fact, the high threshold voltage of Schmitt trigger V_{TH} is greater than V_T of standard CMOS inverter (M_n is not on until $V_i = V_{IN} > V_T$). Transistor M_n of standard inverter turns on at $V_i = V_{tn}$.

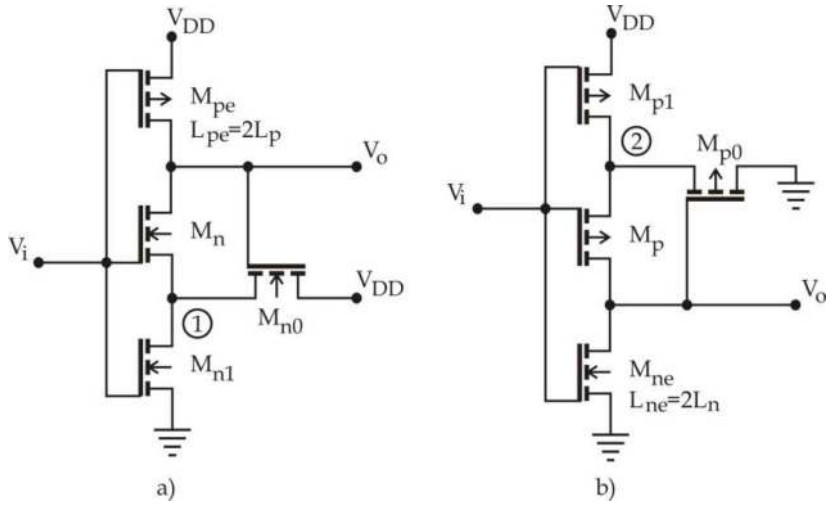


Fig. 9. Equivalent circuits: (a) used to determine V_{TH} and (b) to determine V_{TL}.

Assume V_i increases from 0 up to V_{DD}. Until the output state is changed, M_{p0} is off ($V_{GS} = 0$). M_p and M_{p1} are connected in series and can be replaced with one transistor of which the constant is $k_{pe} = k_p/2$ (Dokic, 1988). For further analysis the equivalent circuit shown in Fig.9a is used.

At $V_i \geq V_{tn1}$, M_{n1} turns on, but M_n is off because $V_i - V_1 < V_{tn}$. Now both M_{n1} and M_{n0} are saturated, thus forming an inverting amplifier with a voltage gain of about A_n(22). Namely, through equalization $I_{Dn1} = I_{Dn0}$ in saturation, we obtain:

$$V_1 = V_{DD} - V_{tn0} - A_n\left(V_i - V_{tn1}\right) \tag{21}$$

where:

$$A_n = \sqrt{\frac{W_{n1}/L_{n1}}{W_{n0}/L_{n0}}} \quad \text{and} \quad V_{tn1} \leq V_i \leq V_1 + V_{tn} \tag{22}$$

Therefore, V_1 decreases as V_i increases (Fig.10a). There is no change of the output state until M_n is off. It turns on when $V_i = V_1 + V_{tn}$, which is equivalent, in regard to (21), to:

$$V_{IN} = V_{tn} + \frac{V_{DD} - V_{tn}}{1 + A_n} \tag{23}$$

where $V_{tn} = V_{tn1} = V_{tn0}$. In further analysis we assume $k_n = k_{n1}$, $k_p = k_{p1}$ and that the threshold voltages of pMOS transistors are also equal, i.e. $V_{tp} = V_{tp1} = V_{tp0}$. With standard CMOS inverter the output voltage begins to decrease at $V_i = V_{tn}$, and with Schmitt trigger it does not until $V_i = V_{IN}$. For $k_{n1} = k_{n0}$, $V_{IN} = 0.5(V_{DD} + V_{tn})$. Thus, an approximate value of the high threshold voltage V_{TH} can be determined by replacing V_{tn} of eq. (7) with V_{IN}. Out of this claim, we obtain $V_{TH} \approx 0.75V_{DD} - 0.25V_{tn}$, when all transistors are symmetric. More accurate value of V_{TH} is determined in a following way.

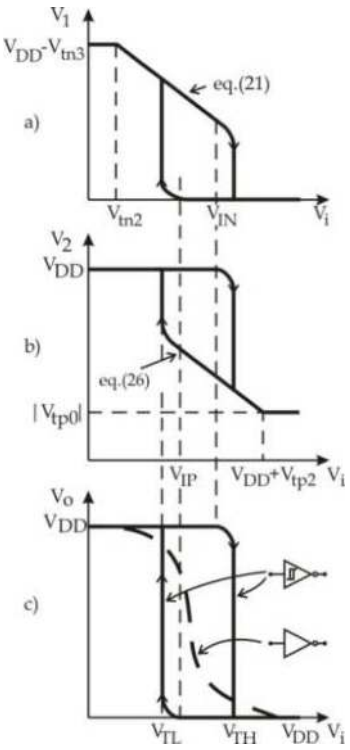


Fig. 10. Voltages in points of interest versus of input voltage.

After M_{n1} is on, V_o starts to decrease slightly. This change, through the gate-source of M_{n0}, is transferred to point 1, which accelerates the process of turning M_n on. When the amplification of the feedback loop achieves the value of (-1), positive feedback leads to step change of the output voltage. During this change, M_{p0} is on, accelerating the process of turning M_p off.

Transistors M_{pe} and M_n (Fig.9a) are in saturation when positive feedback is achieved. Thus, the high threshold voltage V_{TH} can be determined by equalization of drain currents of M_{pe} and M_n in saturation, i.e.:

$$k_n\left(V_i - V_1 - V_{tn1}\right)^2 = k_{pe}\left(V_{DD} + V_{tp} - V_i\right)^2 \tag{24}$$

where V_1 is determined by (21). Replacing $V_i = V_{TH}$, we obtain:

$$V_{TH} = V_{tn} + \frac{V_{DD} + V_{tp} - V_{tn} + B_1\left(V_{DD} - V_{tn}\right)}{1 + B_1\left(1 + A_n\right)} \tag{25}$$

where:

$$B_1 = \sqrt{k_n / k_{pe}} = \sqrt{2k_n / k_p} \tag{26}$$

When $V_i = V_{DD}$, transistors M_p, M_{p1} and M_{n0} are off, and M_n, M_{n1} and M_{p0} are on, so $V_o = 0$. Then voltage of point 2 is $V_2 = |V_{tp0}|$, because M_{p0} is on and saturated ($V_{GDp} = 0$).
Assume V_i decreases from V_{DD} down to 0. All the time until the process of change of V_0 from 0 up to V_{DD} starts, M_{n0} is off, so the equivalent circuit for determining V_{TL} is shown in Fig.9b. At $V_i = V_{DD} + V_{tp1}$, M_{p1} turns on. Equalizing drain currents of transistors M_{p1} and M_{p0} in saturation, we obtain that the voltage of point 2 increases linearly:

$$V_2 = A_p\left(V_{DD} + V_{tp} - V_i\right) - V_{tp} \tag{27}$$

where:

$$A_p = \sqrt{\frac{W_p / L_p}{W_{p0} / L_{p0}}} \tag{28}$$

Transistor M_p turns on when $V_i = V_2 + V_{tp}$, so, considering (27):

$$V_{IP} = V_{DD} + V_{tp} - \frac{V_{DD} + V_{tp}}{1 + A_p} \tag{29}$$

From (29), for $k_p = k_{p0}$, we obtain: $V_{IP} = 0.5\left(V_{DD} + V_{tp}\right) < 0.5V_{DD}$.
Replacing V_{tp} in (7) with V_{IP} ($V_{IP} = -V_{tp}$), we obtain an approximate value of the low threshold voltage of the symmetric Schmitt trigger as follows: $V_{TL} = 0.25V_{DD} - 0.5V_{tp}$. At $V_i = V_{IP}$, V_o starts rising, and this change, through gate-source of M_{p0}, is transferred to point 2 and accelerates the process of turning M_{p1} on. When $|dV_o/dV_i| \geq 1$ positive feedback loop is achieved, so the change of V_o is step. M_p and M_{ne} are saturated, so:

$$k_{ne}\left(V_i - V_{tn}\right)^2 = k_p\left(V_2 + V_{tp} - V_i\right)^2 \tag{30}$$

where V_2 is determined by (27). Replacing $V_i = V_{TL}$, we obtain:

$$V_{TL} = V_{tn} + \frac{A_p\left(V_{DD} + V_{tp} - V_{tn}\right) - V_{tn}}{1 + B_2 + A_p} \tag{31}$$

where:

$$B_2 = \sqrt{k_{ne} / k_p} = \sqrt{k_n / \left(2k_p\right)} \tag{32}$$

When nMOS and pMOS transistors are symmetric, the thresholds V_{TH} and V_{TL} are also symmetric around $V_{DD}/2$, i.e. the transfer characteristic of the Schmitt trigger is optimum. Symmetry in this case is defined with these two conditions:

- symmetric cascode transistors M_n, M_{n1} and M_p, M_{p1};
- symmetric transistors which create positive feedback M_{n0} and M_{p0}.

Therefore, the high V_{TH} and the low V_{TL} threshold voltages, besides supply voltage, depend on the ratio of geometry of cascode transistors and transistors which create positive feedback. This is shown in Fig.11.

Length of the channel is a constant of technology, and most of the transistors within a digital circuit have the same length of the channel. Knowing this, we have:

$$A_n = \sqrt{W_n / W_{n0}}\,, A_p = \sqrt{W_p / W_{p0}} \tag{33}$$

Fig. 11. shows threshold voltages as functions of squared constants A_n and A_p. Rising widths of channel W_{n0} and W_{p0} of transistors M_{n0} and M_{p0}, the high threshold increases and the low threshold decreases.

Voltage hysteresis $V_H = V_{TH} - V_{TL}$ increases as constants A_n and A_p decrease (Fig.12). When constants k_n and k_p of all transistors are equal, voltage hysteresis is somewhat less than $0.5V_{DD}$.

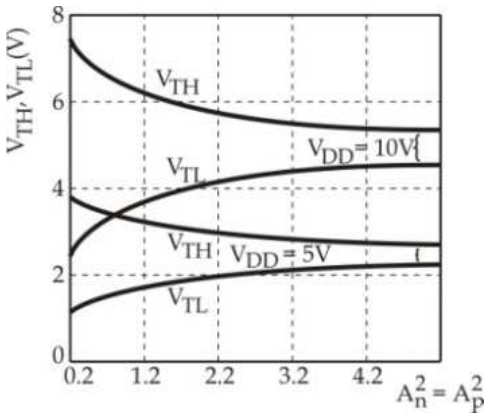


Fig. 11. $V_{TH}$and V_{TL} thresholds versus $A_n^2 = A_p^2$ obtained by SPICE analysis.

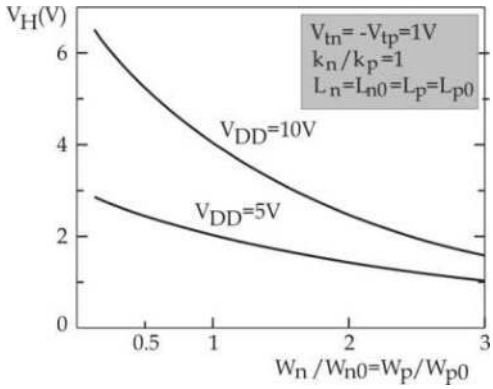


Fig. 12. Voltage hysteresis as function of ratio of transistor channels' widths.

Fig.13. shows the average propagation delay time, obtained by computer simulation using the program SPICE, as a function of the constants $A_n = A_p$ and the capacitive load at $V_{DD} = 5V$. For $A_n = A_p > 1$ the propagation delay time almost does not depend on the M_{n0} and M_{p0} geometry.

Therefore, by controlling the hysteresis through change of A_n and A_p (Fig.12), the propagation delay time is nearly held constant. Thusly, the ratio $W_n/W_{n0} = W_p/W_{p0} \approx 1$ is optimum, when noise immunity and propagation delay time are concerned.
Another, very important, characteristic of this Schmitt trigger is it's absolute stability at a wide number of tolerances of transistor parameters.

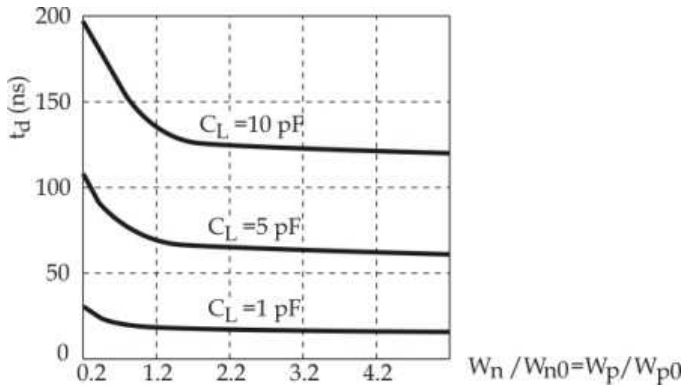


Fig. 13. Average propagation delay time as function of ratio of transistor channels' widths and C_o at $V_{DD} = 5V$.

3.1 Schmitt trigger with four MOS transistors

Schematics of these circuits are shown in Fig.14. and are completely the same as equivalent circuits used to analyze high (Fig.9a) and low (Fig.9b) threshold of Schmitt trigger from Fig.8. That is why, for example, V_{TH} of the circuit from Fig.14a is the same as with the standard Schmitt trigger – only $k_{pe} = k_p/2$ should be replaced with k_p in B_1 (22). Change appears at the low threshold. Namely, while V_i decreases from V_{DD} to V_{TL}, M_{n0} is off. Transfer characteristic, $V_o = f(V_i)$, in that area is determined by CMOS inverter made by M_p and M_n, M_{n1}, so the voltage of the low threshold is determined by (7), where k_n is replaced with $k_n/2$ (M_n and M_{n1} are serially connected), i.e.:

$$V_{TL} = V_{tn} + \frac{V_{DD} + V_{tp} - V_{tn}\sqrt{(k_n/2)/k_p}}{1 + \sqrt{(k_n/2)/k_p}} \tag{34}$$

As it has already been said, area of transfer characteristic for which: $V_{TL} < V_i < V_{DD}$, is completely the same as the characteristic of the standard inverter. During the process of state change, as transistor M_n enters saturation, transistor M_{n0} turns on. Through M_{n0} positive feedback loop is formed, thus further changed of V_o are step.
Analogous explanation is given for the circuit shown in Fig.14c. Therefore, V_{TH} is obtained when k_p is replaced with $k_p/2$ in (7) (because M_p and M_{p1} are serially connected), and V_{TL} is determined by (31), where $k_{ne} = k_n/2$ is replaced with k_n.

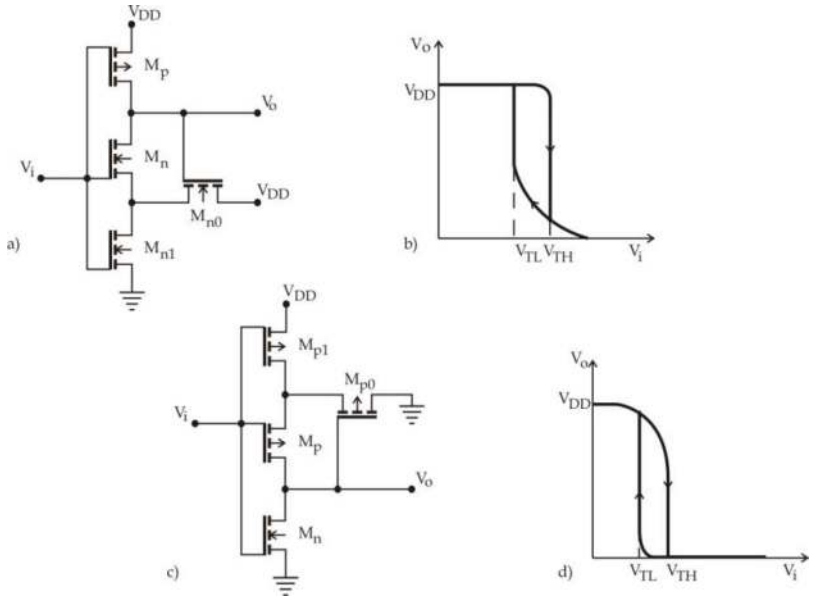


Fig. 14. Schmitt triggers with four transistors and their transfer characteristics.

4. Non-inverting Schmitt trigger

Latch circuit with inverters I_1 and I_2, if applied to output of standard inverter I (Fig.15), can, under certain conditions, work as Schmitt trigger (Bundalo & Dokic, 1985). As it will be shown, transistors of inverter I_1 must be smaller than transistors of the input inverter (smaller W, same L).

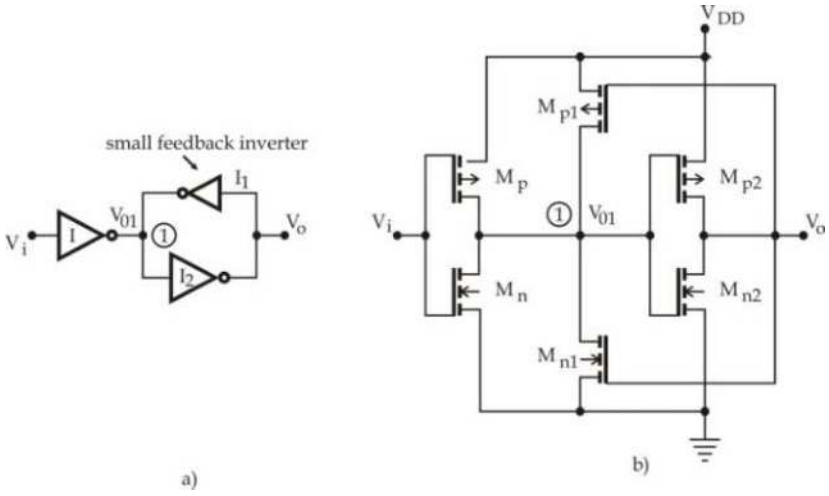


Fig. 15. Logic (a) and expanded schematic of non-inverting Schmitt trigger (b).

Basic idea and characteristics are very similar to the Schmitt trigger in Fig.3. If the input is low, output voltage is: $V_o = 0$. Transistor M_{n1} is off, and M_{p1} on and in linear area of the characteristic. Thus, equivalent circuit, while input voltage increases, is shown in Fig.16a. If M_{p1} is replaced by it's drain-source resistance in linear area, then all equivalent circuits in Fig.s 16a and 5a are completely the same.

While input is high, $V_o = V_{DD}$, M_{p1} is off, and M_{n1} is on. Equivalent circuit (Fig.16b), during the process of input voltage decreasing, is similar to the circuit in Fig.5b, where M_{n1}, which is in linear area, stands instead of resistor R.

Transfer characteristics $V_o(V_i)$ and $V_{o1}(V_i)$ are shown in Fig.17., broken line shows the characteristic of the standard inverter.

Equivalent circuit for determining the high threshold is shown in Fig.16a. Assume that the input voltage increases from 0 up to V_{DD}. For $V_{tn} < V_i < V_{TH}$, all three transistor circuits in Fig.16a are on, so that:

$$I_{Dn} = I_{Dp} + I_{Dp1} \tag{35}$$

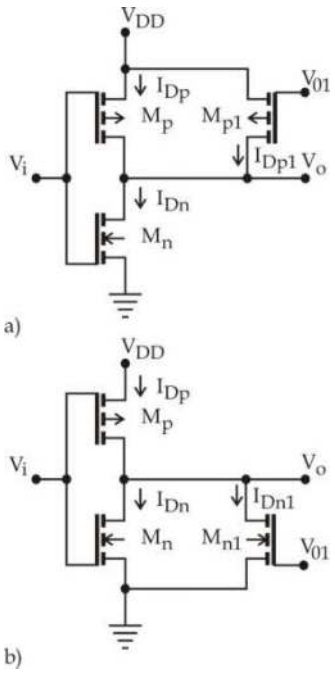


Fig. 16. Equivalent circuit for determi-ning the high (a) and the low (b) threshold voltage.

In the beginning of the process M_{n1} and M_{p1} are in linear, and M_n is in saturation area. When $V_{o1} < V_{DD} - |V_{tp}|$, pMOS transistor of inverter I_2 starts to turn on, so the output voltage V_o increases (to the right from the point C in Fig.17b). This leads to increase of resistance of transistor M_{p1} and of the slope of the characteristic $V_{o1}(V_i)$. Between input and output of latch circuit positive feedback loop is established. The process becomes regenerative and it

leads to step changes of V_{o1} and V_o (point A in Fig.17a) when the amplification of the positive feedback loop is:

$$dV_o / dV_i = -1 \tag{36}$$

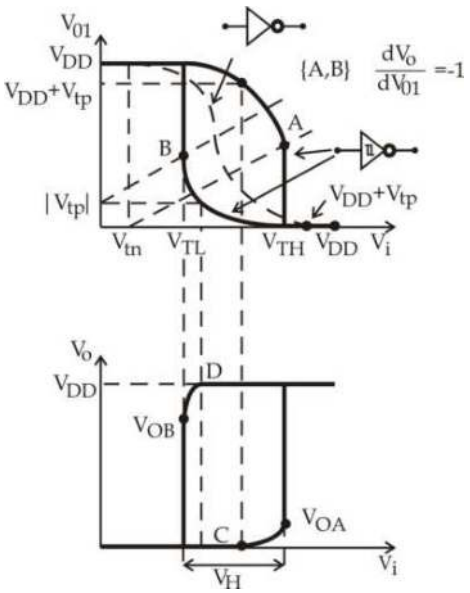


Fig. 17. Transfer characteristics of Schmitt trigger (Fig.15).

Determining the exact value of the high threshold V_{TH}, according to (36), leads to equations of higher degree, making it impossible to find explicit solution for V_{TH}. Because of this approximate method will be used for this purpose. Namely, transistor M_{p1} is in linear area for all values of input voltage: $0 < V_i < V_{TH3}$, so it can be replaced with a resistor of approximate resistance:

$$R_{p1} \approx \frac{1}{2k_{p1}\left(V_{DD} + V_{tp1}\right)} \tag{37}$$

Then the equivalent circuit from Fig.16a is the same as the one in Fig.5a, so the high threshold is obtained by replacing R in (12) with R_{p1}, which leads to:

$$V_{TH} = \frac{V_{DD}}{2} + \frac{k_{p1}}{k_p}\frac{V_{DD} + V_{tp1}}{2\left(V_{DD} + V_{tp} - V_{tn}\right)}V_{DD} \tag{38}$$

As long as the input is high, the output voltage is $V_o = V_{DD}$, which means that M_{p1} is off and M_{n1} is on. The equivalent circuit, when the input voltage starts to decrease, is shown in Fig.16b. Positive feedback is established when $dV_o/dV_i = -1$ (point B in Fig.17). Transistor M_{n1} is in linear area, and can, thus, be replaced with a resistor of approximate resistance:

$$R_{n1} \approx \frac{1}{2k_{n1}\left(V_{DD} - V_{tn1}\right)} \tag{39}$$

Voltage of the low threshold can be determined by replacing R in (16) with R_{n1}, so:

$$V_{TL} = \frac{V_{DD}}{2} - \frac{k_{n1}}{k_n}\frac{V_{DD} - V_{tn1}}{2\left(V_{DD} + V_{tp} - V_{tn}\right)}V_{DD} \tag{40}$$

Transfer characteristic is optimum when inverters are symmetric, because V_{TH} and V_{TL} are symmetric around $V_{DD}/2$. Then voltage hysteresis is given by:

$$V_H = \frac{k_1}{k}\frac{V_{DD} - V_t}{V_{DD} - 2V_t}V_{DD} \tag{41}$$

where: $k_1 = k_{p1} = k_{n1}$, $k = k_p = k_n$ and $V_{tn} = V_{tn1} = |V_{tp}| = |V_{tp1}| = V_t$.
Therefore, basic parameters, V_{TH}, V_{TL} and V_H, besides supply voltage V_{DD} and threshold voltages of the transistors, depend on ratio of geometry of the transistors of feedback inverter I_1 and input inverter I. Range in which ratio can be changed is limited. As it has already been said, changes of state at the output are caused by existence of points in characteristic $V_o(V_{o1})$ with unit amplification, i.e. $dV_o/dV_i = 1$. In the worst case, during static states, voltage V_{o1} has to be, at $V_i = V_{DD}$, less than, and at $V_i = 0$ greater than the threshold of inverter I_2, i.e.:

$$V_o\left(V_{DD}\right) \le V_{T2} = V_{DD}/2 \text{ and } V_o(0) \ge V_{T2} = V_{DD}/2 \tag{42}$$

The equations show that the changes are conditioned by ratio of geometry of transistors: M_{p1} and M_n (M_p and M_{n1} are off) in first ($V_i = V_{DD}$), and M_p and M_{n1} in second ($V_i = 0$) case.
It can be shown that the Schmitt trigger in Fig.15 will operate reliably for all acceptable supply voltages, if:

$$k_n / k_{p1} > 2 \text{ and } k_p / k_{n1} > 2 \tag{43}$$

4.1 Schmitt triggers with five transistors

The Schmitt trigger shown in Fig.15 has a hysteresis shaped characteristic if one of the transistors of the inverter I_1 is left out. Such simplified circuit is shown in Fig.18. The circuit in Fig.18a will be analyzed. While input voltage increases, this circuit is completely the same as the circuit shown in Fig.15, because during this process M_{n1} was off. Thus, the high threshold voltage is determined in (38).
During negative change of V_i, M_{p1} is off. Since there is no feedback loop, a low threshold voltage is equal to the threshold voltage of input inverter I. During the change of output from high down to low logic level, regenerative process is established. Namely, for $V_o > V_{DD} - |V_{tp}|$, M_{p1} is off and the shape of $V_o(V_i)$ function is determined by cascode inverters I and I_2. At $V_o = V_{DD} - |V_{tp}|$ (point A in the transfer characteristics), M_{p1} turns on and establishes positive feedback loop, thus making change of V_o step.
The whole analysis is analogically applicable for the circuit in Fig.18b, with the difference that the high threshold is equal to the threshold voltage of inverter I, and the low threshold is determined by (40).

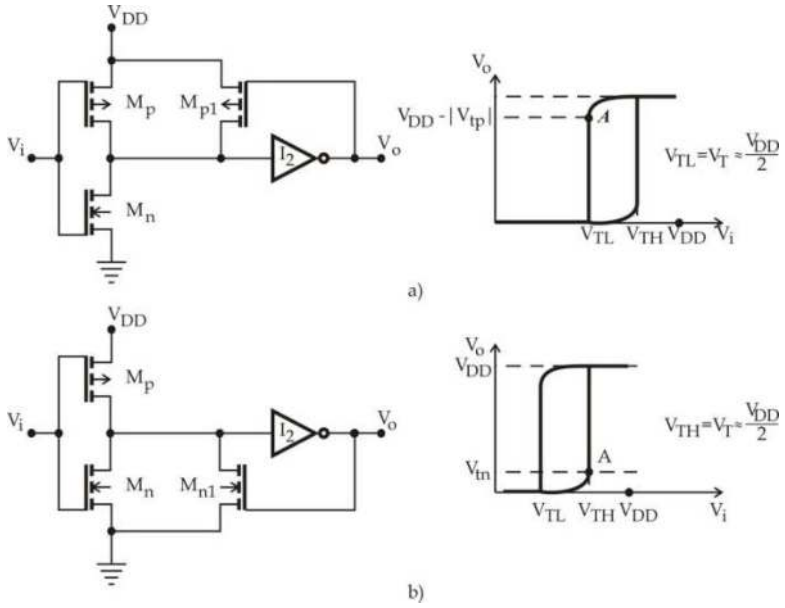


Fig. 18. Schmitt triggers with five transistors and their transfer characteristics.

5. Schmitt trigger with voltage controlled thresholds

All Schmitt circuits analyzed so far have fixed parameters (V_{TH}, V_{TL} and V_H), at defined supply voltage. Often there is a need to control parameters of Schmitt trigger, depending on the field of application. Control of it's parameters from outside of the circuit is demanded. Such possibility exists when the Schmitt trigger shown in Fig.19 is used. Here, in cascode connection with transistors M_{n1} and M_{p1} of the circuit shown in Fig.15, the transistors M_{n0} and M_{p0} are added.

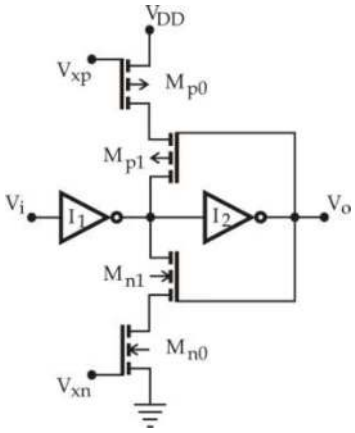


Fig. 19. Schmitt trigger with voltage controlled thresholds.

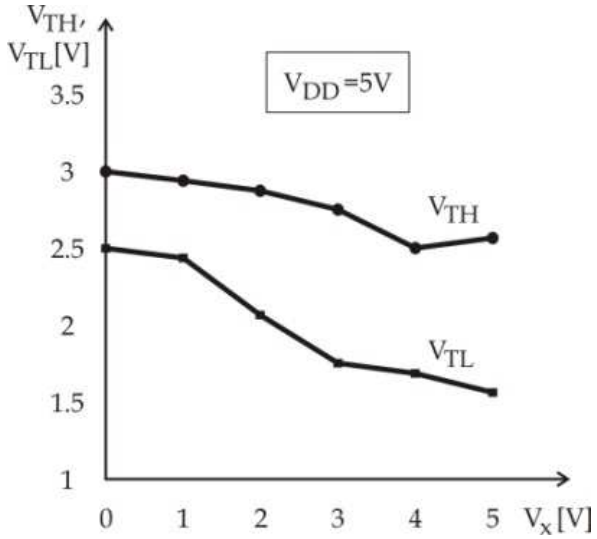


Fig. 20. Threshold voltages of Schmitt trigger in Fig. 19 as functions of common control voltage V_x

Over the gates of transistors M_{n0} and M_{p0}, control voltages V_{xn} and V_{xp} are supplied. These voltages are used to change equivalent resistance of M_{p0} and M_{p1} towards V_{DD}, and M_{n0} and M_{n1} towards ground. While input voltage increases, this resistance is the resistance of transistors M_{p1} and M_{p0} in linear area (M_{n1} is off, so influence of M_{n0} is blocked). Since the resistance of M_{p0} depends on voltage, thus total resistance towards V_{DD} is a function of V_{xp}. Voltage V_{xn} is used to modulate the low threshold of Schmitt trigger by changing the resistance of M_{n0}. Controlling the thresholds is independent for each of them: V_{xp} influences only V_{TH}, and V_{xn} only V_{TL}.
When gates of M_{n0} and M_{p0} are short circuited, control voltage is common. It influences both V_{TH} and V_{TL} in the same amount. In this way voltage hysteresis remains constant (Fig.20).

6. NAND and NOR circuit design

Thus, the Schmitt trigger-inverter (Fig.1) consists of one conventional CMOS inverter (M_n, M_p), one nMOS inverter (M_{n1}, M_{n0}) and one pMOS inverter (M_{p1}, M_{p0}). The same principle is used for design of the NAND and NOR Schmitt circuits shown in Fig.21 (Dokic, 1996). In this case conventional CMOS, nMOS and pMOS NAND and NOR gates are used instead of the corresponding inverters.
Since the transistors M'_{n1}, …, M'_{nm} and the nMOS transistors of the conventional CMOS NAND gates are connected in series, the output of the circuit in Fig.21a will be low only when all inputs are high, i.e. $\bar{Z} = x_1 x_2 \dots x_m$, so that $Z = \overline{x_1 x_2 \dots x_m}$. Hence this is an m-input NAND gate.
The output of the circuit in Fig.21b will be high only when all inputs are low (M'_{p1}, …, M'_{pm} and pMOS transistors of the conventional NOR gate are connected in series and must be conducting), i.e. $Z = \bar{x}_1 \bar{x}_2 \dots \bar{x}_m$ or $Z = \overline{x_1 + x_2 + \dots + x_m}$. Hence this is an m-input NOR gate.

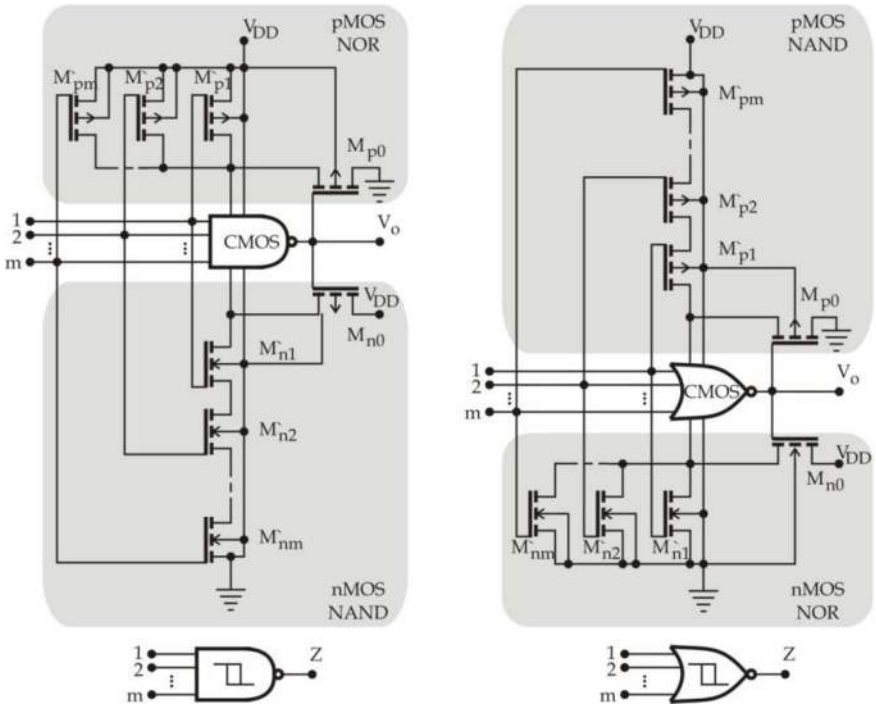


Fig. 21. Principle schematics of m-input NAND and NOR Schmitt circuits (Dokic, 1996).

The transistors M_{n0} and M_{p0} provide feedback to effect rapid change of the output voltage and the transfer characteristic has a shape of the hysteresis curve. Hence the circuits in Figs. 21a and 21b are *m*-input NAND and NOR Schmitt circuits, respectively.

6.1 NAND circuit analysis

Parallel or series transistors can be replaced by one transistor such as the conventional NAND and NOR circuits (Dokic, 1982). In this way, NAND and NOR Schmitt circuits can be replaced by an equivalent Schmitt trigger-inverter (Fig.9) by dc analysis. It will be shown by analyzing an *m*-input NAND Schmitt circuit.

Assume that n inputs are active (at V_i), where $1 \le n \le m$, and that the other m-n inputs are at V_{DD}. Let the input voltage V_i increase from zero to V_{DD}. For $0 \le V_i \le V_{TH}$ the NAND circuits in Fig.21a can be replaced by the equivalent circuit in Fig.9a. M_{p0} and m-n pMOS transistors at $V_i = V_{DD}$ are off. Therefore, the equivalent pMOS transistor M_{pe} consists of n pairs of pMOS transistors M_{pi}, M'_{pi} with active inputs. Hence M_{pe} constant k is given by:

$$k_{pe} = nk_p / 2 \tag{44}$$

Transistor M_{n1} (Fig.9a) needs to be replaced with one equivalent transistor which consists of series nMOS transistors of a conventional NAND gate.

The equivalent constant k of series transistors depends on the number of transistors and position of the first active input (Dokic, 1982). Consequently, for the case of n active inputs

the transistors M_{n1}, …, M_{nm} and M'_{n1}, …, M'_{nm} can be replaced by the equivalent transistors M_{ne} and M_{ne1}, respectively, whose constants k are given by:

$$k_{ne} = k_{ne1} = \frac{k_n}{m-p+1} \tag{45}$$

where p marks the position of the first active input (for example, if $p = 3$, the inputs of the transistors M_{n1}, M'_{n1} and M_{n2}, M'_{n2} are at V_{DD}, and M_{n3}, M'_{n3} are at V_i). Now, eq.(22) and (26) become, respectively:

$$A_{ne} = \sqrt{k_{ne1} / k_{n0}} = A_n (m-p+1)^{-1/2} \tag{46}$$

$$B_{1e} = \sqrt{k_{ne} / k_{pe}} = B_1 \left[n(m-p+1) \right]^{-1/2} \tag{47}$$

where A_n and B_1 are given by eqs. (22) and (26), respectively.
From eq. (25), replacing A_n by A_{ne} and B_1 by B_{1e} we obtain the high threshold voltage of the m-inputs NAND Schmitt circuit:

$$V_{TH} = \frac{V_{DD} + V_{tp} + B_1 \left[n(m-p+1) \right]^{-1/2} \left[V_{DD} + A_n (m-p+1)^{-1/2} V_{tn} \right]}{1 + B_1 \left[n(m-p+1) \right]^{-1/2} \left[1 + A_n (m-p+1)^{-1/2} \right]} \tag{48}$$

To calculate V_{TL} the circuit in Fig.21a can be replaced by an equivalent one shown in Fig.9b. Namely, M_{n2} is off. M_{n1}, …, M_{nm}, M'_{n1}, …, M'_{nm} are on and can be replaced by an equivalent one M_{ne} with the constant k:

$$k_{ne} = k_n / (2m) \tag{49}$$

M_{p2} is on. M_{pi} and M_{p1i} $(i = 1, \ldots, n)$ with active input can be replaced by equivalent transistors M_{pe} and M_{pe1}, respectively, with the constants k:

$$k_{pe} = k_{pe1} = nk_p \tag{50}$$

The k ratios of M_{pe1} to M_{p0} and M_{ne} to M_{pe1}, respectively, are given by:

$$A_{pe} = \sqrt{k_{pe1} / k_{p2}} = A_p n^{1/2} \tag{51}$$

$$B_{2e} = \sqrt{k_{ne} / k_{pe1}} = B_2 (mn)^{-1/2} \tag{52}$$

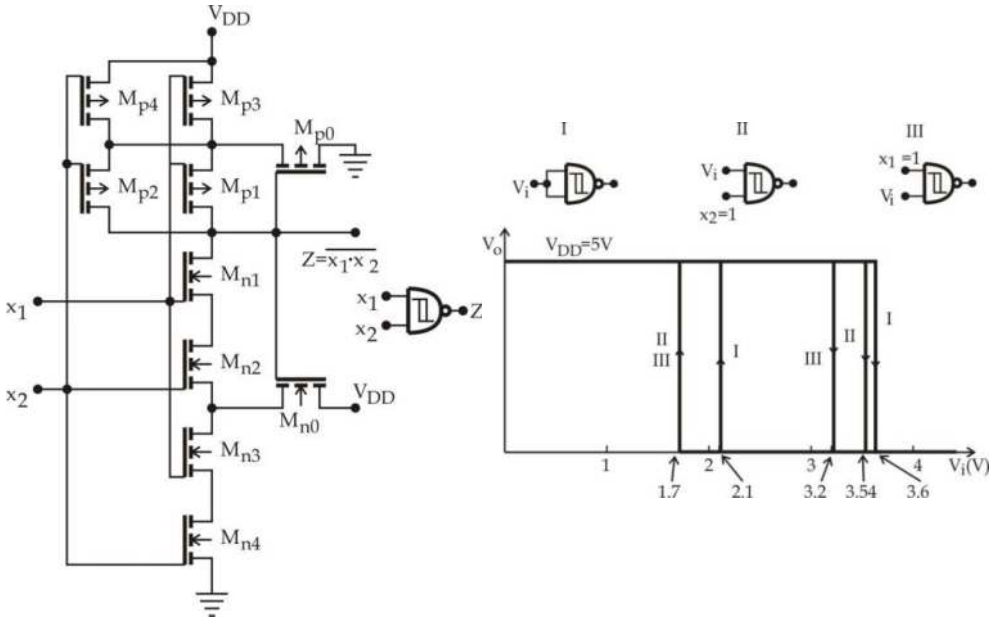
From eq. (36), replacing A_p by A_{pe} and B_2 by B_{2e}, we obtain the low threshold voltage of the m-inputs NAND Schmitt circuits:

$$V_{TL} = \frac{A_p n^{1/2} (V_{DD} + V_{tp}) + B_2 (mn)^{-1/2} V_{tn}}{1 + A_p n^{1/2} + B_2 (mn)^{-1/2}} \tag{53}$$

where A_p and B_2 are given by eqs. (27) and (32), respectively.

The threshold voltages V_{TH} and V_{TL} depend on supply voltage V_{DD}, the ratio of the constants k_n/k_p, k_n/k_{n0}, i.e. k_p/k_{p0}, number of inputs m, and number of active inputs n. Besides, V_{TH} depends on the position of the first active input p.

In Fig.22 two-input Schmitt NAND gate and it's transfer characteristics at $V_{DD} = 5V$, for $k_{ni} = k_n = 2k_{pi} = 2k_p$, $i = 0,\ldots,4$ and $V_{tn} = -V_{tp} = 1V$, are shown. The high threshold depends on the number and the combination of active inputs, and the low only on the number of active inputs. The voltage thresholds, as function of channel widths ratio of cascode transistors and of transistors M_{n0} and M_{p0} in the circuit of positive feedback loop, are shown in Fig.23.



(a) (b)

Fig. 22. Two-input NAND Schmitt trigger (a) and it's transfer characteristic (b) at $V_{DD} = 5V$.

6.2 NOR circuit

As the NOR circuit is obtained from the NAND one through the interchange of the p-channel and n-channel transistors and a power supply polarity change, the previous analysis can be applied analogously to this circuit. In this way we obtain:

$$V_{TH} = \frac{V_{DD} + V_{tp} + B_1(mn)^{1/2}\left(V_{DD} + A_n n^{1/2} V_{tn}\right)}{1 + B_1(mn)^{1/2}\left(1 + A_n n^{1/2}\right)} \tag{54}$$

$$V_{TL} = \frac{A_p(m-p+1)^{-1/2}\left(V_{DD} + V_{tp}\right) + B_2\left[n(m-p+1)\right]^{1/2} V_{tn}}{1 + A_p(m-p+1)^{-1/2} + B_2\left[n(m-p+1)\right]^{1/2}} \tag{55}$$

Therefore, the threshold voltages depend on exactly the same parameters as the thresholds of the NAND circuit except that in the NOR circuit, V_{TH} does not depend on the position of the first active input p.

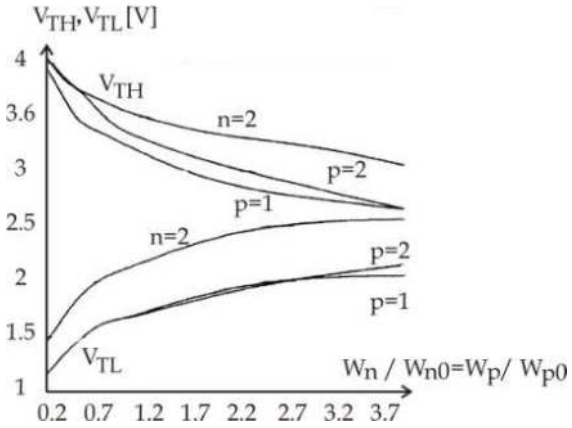


Fig. 23. SPICE values of V_{TH} and V_{TL} for two-input NAND circuit versus $W_n/W_{n0} = W_p/W_{p0}$ for various numbers and combinations of active inputs at $V_{DD} = 5V$ and for optimum geometry ratio of nMOS and pMOS transistors, that is at $k_n/k_p = 2$.

7. CMOS gates with regenerative action at one of inputs

In many applications when NAND and NOR gates are used in an MSI or LSI circuit there is a Schmitt trigger at the external input only. So, for example, a Schmitt trigger action in the clock input of counter provides pulse shaping that allows unlimited clock input pulse rise and fall times. These circuits are made by a conventional NAND or NOR gate and Schmitt trigger on their external input. CMOS NAND or NOR gate and Schmitt trigger action at one input (Fig.24) is a better solution. The Schmitt trigger is an integral part of the gate. The advantages of these circuits, compared with the conventional ones, are: smaller number of transistors, smaller area of the chip and higher switching speed.

7.1 Principle schemes

Fig.24 illustrates the principle schemes of the two input NAND and NOR logic circuits with hysteresis when the input x_1 is active. When the input x_2 is active only, the transfer characteristic is without hysteresis. These circuits consist of the Schmitt trigger on Fig.8 and one pair of CMOS transistors (M_n and M_p). Multiple inputs are made in a conventional way (by adding one pair of CMOS transistors to each input).

Consider the NAND circuit in Fig.24a. When the input x_1 only is active, and $x_2 = 1$, the transistor M_p is off, and M_n is on. Then the transfer characteristic is determined by the Schmitt trigger. If the input x_2 only is active the Schmitt trigger does not operate, so that the transfer characteristic will be the same as that of the CMOS inverter made by the transistors M_n and M_p.

The NOR gate will be described more fully.

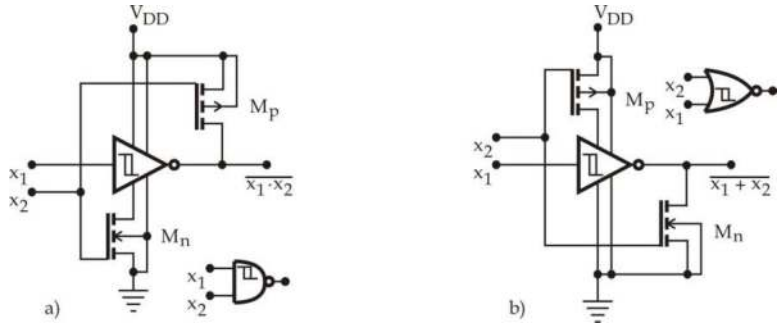


Fig. 24. Two input NAND (a) and NOR (b) gates with the regenerative action only at the input x_1 (Dokic, 1988).

7.2 NOR gate

Fig.25 shows the two-input NOR gate with the regenerative action at the input x_1 only. The transistors M_{ni} and M_{pi} $(i = 0,1,2)$ make the Schmitt trigger circuit (Fig.8).

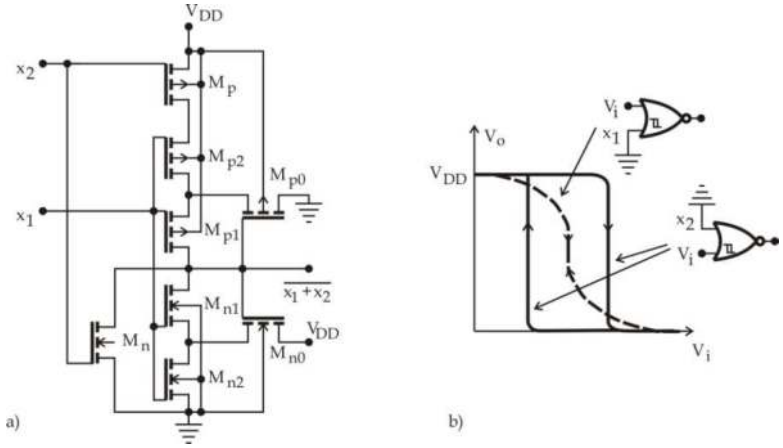


Fig. 25. Scheme of the NOR gate (a) and voltage transfer characteristic (b).

When the input x_2 is active and $x_1 = 0$ the transistors M_{p1} and M_{p2} are on, and M_{n1}, M_{n2} and M_{p0} are off. Hence there is no feedback between the output and the input, the transfer characteristic is without hysteresis (see Fig.25a – broken line) and it is exactly the same as for the conventional two-input gate with the active input.
When the input x_1 is active and $x_2 = 0$ the transistor M_p is on, and M_n is off. Then the circuit in Fig.25 acts as the Schmitt trigger. Namely, the transistors M_p and M_{p2} can be replaced by an equivalent with constant $k_{pe} = k_p/2$, so that the Schmitt trigger on Fig.8 is obtained.

8. BiCMOS Schmitt circuits

Non-inverting BiCMOS Schmitt trigger is shown in Fig.26 (Dokic, 1995). It consists of CMOS Schmitt trigger at the input (Fig.15) and a BinMOS output with the transistors T_1, T_2, M_{n3}

and M_{n4}. Basic static parameters are completely the same as for an analogous CMOS circuit in Fig.15. The output is a standard BiCMOS with the logic amplitude of $\Delta V_o = V_{DD} - 2V_{BE}$. The transistor M_{n2}, at same time, is used to bleed the base charge of T_1.

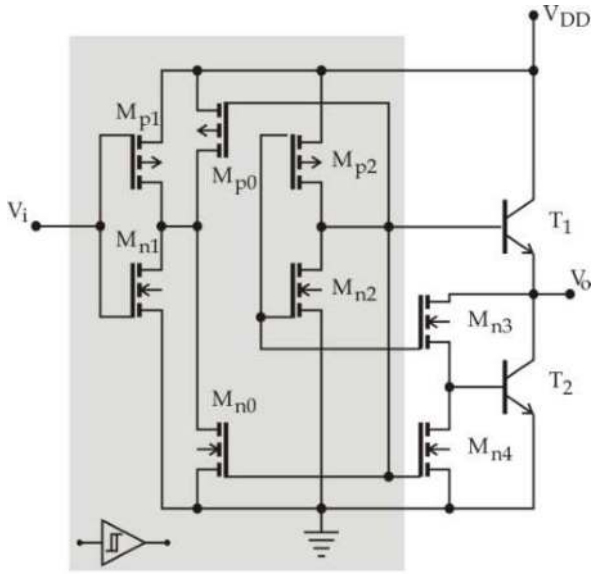


Fig. 26. Non-inverting BiCMOS Schmitt trigger.

Inverting Schmitt trigger is shown in Fig.27. This circuit is very similar to the one shown in Fig.8. Transistors M_{n3} and M_{n2} are MOS bleeding elements. Even the principle of functioning is very similar. Beside increase of speed, bipolar transistor brings certain specifics into static parameters. This increases the amplification with the positive feedback loop, thus leading to a faster change of logic state. Because of this the values of threshold voltages differ from those of the circuit in Fig.8. Practically, as soon as M_n starts conducting at positive, or M_p at negative change of the input voltage, regenerative process is established very fast.

8.1 Short analysis

At $V_i = 0$, transistors M_n, M_{n1}, M_{n3}, M_{p0} and T_2 are off, and M_p, M_{p1} and T_1 are conducting. The output voltage is: $V_o = V_{DD} - V_{BE}$. Transistors M_{n0} and M_{n2} are on, because of $V_3 = V_{DD}$. Hence, the voltage in point 1 is high and equals: $V_1 = V_{DD} - V_{tn0}$, which postpones the process of turning on the transistor M_n in regard to M_{n1}. During the increase of the input voltage from zero to V_{DD}, transistor M_{n1} is turned on first. Since both M_{n1} and M_{n0} are saturated, by equaling their currents, we obtain that voltage V_1 is decreasing, i.e.:

$$V_1 = V_{DD} - V_{tn0} - \sqrt{W_{n1} / W_{n0}}\left(V_i - V_{tn} - V_{BE}\right) \tag{56}$$

where W_{n1} and W_{n0} represent channel widths of transistors M_{n1} and M_{n0}. We assume that the channel lengths are equal. M_n turns on when:

$$V_{gs} = V_i - V_1 = V_{tn} \tag{57}$$

Afterwards, M_{n3} turns on, which, very quickly, leads to establishment of the regenerative process and change of states at the output. Practically, this means that the high threshold is approximately equal to the input voltage at which the condition (57) is fulfilled. Hence, based on (56) and (57), we obtain:

$$V_{TH} \approx \frac{V_{DD} + \sqrt{W_{n1} / W_{n0}}\left(V_{tn} + V_{BE}\right)}{1 + \sqrt{W_{n1} / W_{n0}}} \tag{58}$$

where the thresholds of all nMOS transistors are equal to V_{tn}.

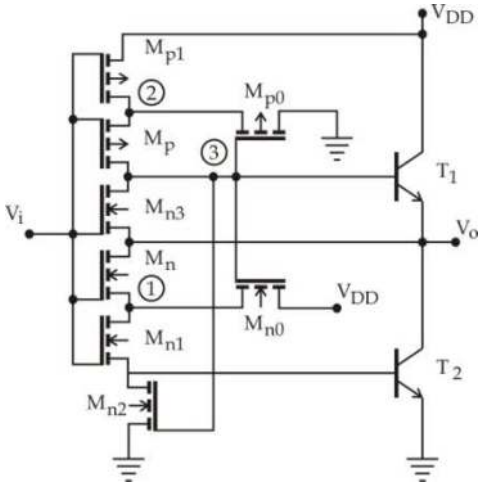


Fig. 27. Inverting BiCMOS Schmitt trigger.

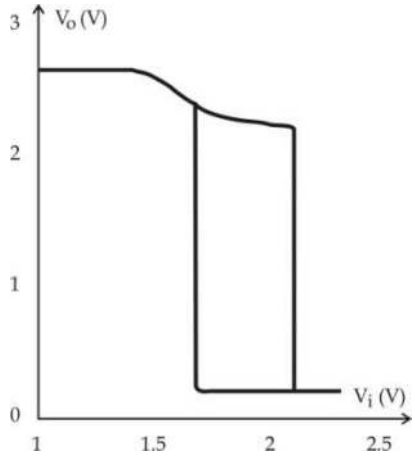


Fig. 28. Static transfer characteristic of inverting Schmitt trigger.

When $V_i = V_{DD}$, transistors M_n, M_{n1}, M_{n3}, M_{p0} and T_2 are on, and M_p, M_{p1}, M_{n0} and T_1 are off. Transistor M_{n3} short-circuits base and emitter of T_1. During the decrease of the input voltage, transistor M_{p1} turns on first. Afterwards, voltage in point 2 increases. Since M_{p1} and M_{p0} are saturated:

$$V_2 = V_{BE2} - V_{tp0} - \sqrt{W_{p1} / W_{p0}} \left(V_{DD} + V_{tp1} + V_i \right) \tag{59}$$

Transistor M_p turns on at:

$$V_i = V_2 + V_{tp} \tag{60}$$

After M_p turns on, the output voltage increases, and a positive feedback loop is established very quickly. Hence V_i in (60) is approximately equal to the low threshold voltage. Based on (59) and (60), we obtain:

$$V_{TL} \approx \frac{\sqrt{W_{p1} / W_{p0}} \left(V_{DD} + V_{tn} \right) + V_{BE}}{1 + \sqrt{W_{p1} / W_{p0}}} \tag{61}$$

Transfer characteristic (Fig.28) is obtained by SPICE analysis at following conditions: supply voltage $V_{DD} = 3V$, $0.8\mu m$ BiCMOS process with minimum channel lengths of all transistors ($L = 0.8\mu m$), transistor threshold voltages $V_{tn} = |V_{tn}| = 0.85V$, channel widths $W_{n1} = W_{n2} = W_{n3} = W_{n4} = 8\mu m$, $W_{p1} = W_{p2} = 24\mu m$, $W_{n0} = 2\mu m$ and $W_{p0} = 6\mu m$.

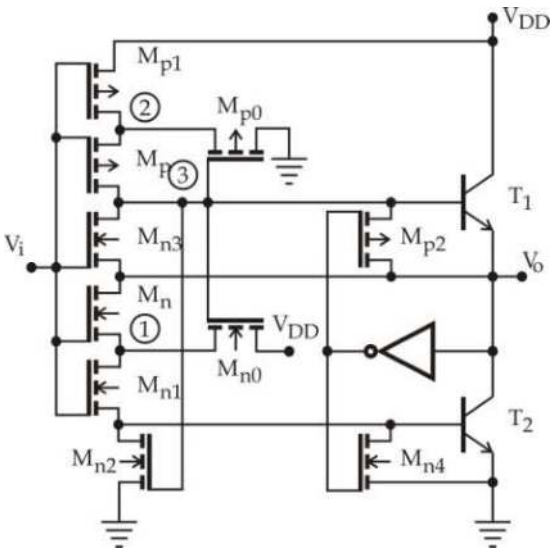


Fig. 29. Low voltage BiCMOS Schmitt trigger.

Calculated values of threshold voltages, by the given parameters including $V_{BE} = 0.7V$, are $V_{TH} = 2.03V$ and $V_{TL} = 1.67V$. Values obtained by simulation are $V_{TH} = 2.12V$ and $V_{TL} = 1.68V$. Errors are very small. These will increase at higher values of supply voltage.

Limitation of application of the circuit in Fig.27 at lower supply voltages is it's decrea-sed logic amplitude of the output voltage $\Delta V_o = V_{DD} - 2V_{BE}$. The low voltage Schmitt trigger is shown in Fig.29. Transistors M_{n4} and M_{p2} through the inverter I hold output voltages at $V_o = V_{DD}$ and $V_o = 0$.

Transistor M_{p4} delivers another improvement. It removes deformation from the transfer characteristic of the standard circuit before the change from high to low level (Fig.28). This deformation is a consequence of the knee-effect of characteristic of bipolar transistor T_1. In Fig.30 SPICE analysis of the output of the low voltage Schmitt trigger designed in $0.8\mu m$ BiCMOS process for equal constants k_n and k_p of all nMOS and pMOS transistors is shown.

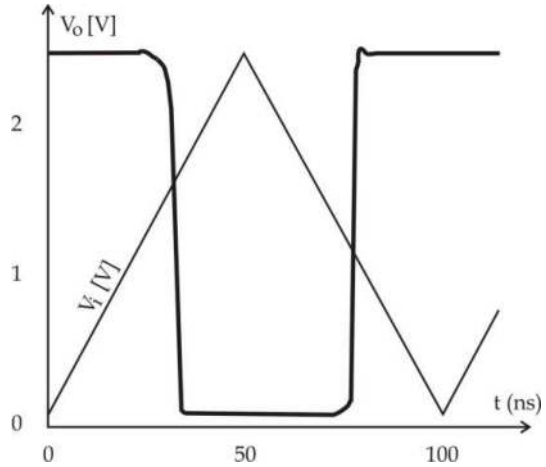


Fig. 30. The output of the low voltage Schmitt trigger to a triangular input at $V_{DD} = 2.5V$.

9. Conclusion

Schmitt logic circuits are produced as independent integrated circuits as well as input circuits of standard MSI/VLSI and ASIC integrated circuits. The author expects that the overview of CMOS and BiCMOS Schmitt triggers will be useful to both engineers who design digital integrated circuits and to those who design digital systems with integrated circuits.

Common characteristics of the described solutions are:

- threshold voltages V_{TH} and V_{TL} are almost symmetric around voltage $V_{DD}/2$, so the transfer characteristics are optimum, concerning noise immunity;
- basic parameters (V_{TH}, V_{TL} and V_H) do not depend on technology.

Overall, the Schmitt inverter (section 3) yields the best characteristic. Its operating stability does not depend on transistor geometries ratio, nor on tolerance of technology. Symmetry of all transistors is optimum, concerning noise immunity and propagation time. While in standard circuits every input is joined by one pair, in Schmitt logic circuits every input is joined by two pairs of CMOS transistors. Taking into account that one pair closes positive feedback loop, it follows that m-input NAND and NOR Schmitt circuits are comprised of $2m$+1 pairs of CMOS transistors. Transfer characteristic of NAND and NOR Schmitt circuits

depend on, like those of the standard ones, the number of inputs, number of active inputs and the position of the first active input.

10. References

Al-Sarawi, S.F. Low Power Schmitt Trigger Circuits, *Electronics Letter*, vol. 38, 29th August 2002, pp 1009-1010.

Arrabi, S. A 90nm CMOS Data Flow Processor Using Fine Grained DVS for Energy Efficient Operation from 0.3V to 1.2V, *IEEE SSC Magazine*, Spring 2011, vol. 3, No. 2, pp 52-58.

Bundalo, Z., Dokic, B., Non-inverting Regenerative CMOS Logic Circuits, *Microelectronics Journal*, vol. 16, No. 5, 1985, pp 5-17.

Dokic, B., CMOS Schmitt triggers, *IEE Procedings - Part G*, vol. 131, No. 5, October 1984, pp 197-202. The paper has been copied to Express Information PEAVT, No. 21, 1985, pp 4-14, The Acadamy of Sciences of USSR.

Dokic, B., CMOS Regenerative Logic Circuits, *Microelectronics Journal* vol. 14, No.5, 1983., pp 21-30. The paper has been copied to Express Information PEAVT, No. 29, 1984, pp 4-14, The Acadamy of Sciences of USSR.

Dokic, B., CMOS NAND and NOR Schmitt Circuits, *Microelectronics Journal* 27, No. 8, November, 1996, pp 757-766.

Dokic, B. et al, CMOS Gates with Regenerative action at One of Inputs, *Microelectronics Journal*, vol. 19, No. 3, 1988, pp 17-20.

Dokic, B. and Bundalo, Z., Regenerative Logic Circuits with CMOS Transistors, *Int. J-Electronics*, 1985, vol. 58, No. 6, pp 907-920.

Dokic, B., Influence of Series and Parallel Transistors on DC Characteristics of CMOS Logic Circuits, *Microelectronics Journal*, vol. 13, No. 2, 1982, pp 25-30.

Dokic, B., Three-State BiCMOS Buffers with Positive Feedback, *Proc. 20th Int. Conf. on Microelectronics (MIEL '95)*, vol. 2, 1995, pp 509-511.

Hard, A. and Voinigesku, S. P., A 1GHz Bandwidth Low-Pass $\Delta\sum$ ADC with 20-50 GHz Adjustable Sampling Rate, *IEEE Journal of SSC*, vol. 44 No. 5, May 2009, pp 1401-1414.

Chien, H., Switch-controllable Dual-hysteresis Mode Bistable Multivibrator Employing Single Differential Voltage Current Converter, *Microelectronics Journal 42*, 2011, pp 745-753.

Katyal, V. et al, Adjustable Hysteresis CMOS Schmitt Triggers, *Circuits and Systems*, 2008 ISCAS 008. IEEE Int. Symposium on, pp 1938-1941.

Lo, Y. et al, Current-input OTRA Schmitt Trigger with Dual Hysteresis Modes, *Int. J. Circ. Theor. Appl. 2010*, vol. 38, pp 739-746.

Pengfei, L. et al., A Delay-locked Loop Synchronization Scheme for High-Frequency Multiphase Hysteretic DC-DC Converters, *IEEE Journal of SSC* vol. 44, No. 11, November 2009, pp 1401-1414.

Wang, C. et al., A 570kbps ASK Demodulator without External Capacitors for Low Frequency Wireless Bio-implants, *Microelectronics Journal* 39, 2008, pp 130-136.

Young, F., A High-speed Differential CMOS Schmitt Trigger with Regenerative Current Feedback and Adjustable Hysteresis, *Analog Integrated Circuits Process*, 2010, 63: pp 121-127.

Zou, Z., et al., A Novel Schmitt Trigger with Low Temperature Coefficient, *Circuits and Systems*, 2008, APCCAS 2008, IEEE Asia Pacific Conference on, pp 1398-1401.

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