Chapter

Power Consumption in CMOS Circuits

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Abstract

In this chapter, we explain the two types of power consumption found in a complementary metal-oxide-semiconductor (CMOS) circuit. In general, a CMOS circuit tends to dissipate power at all times—be it active or inactive. The power consumed by the circuit when it is performing computational tasks is known as dynamic power. On the contrary, the power lost due to current leakage during which the circuit is dormant is referred to as static power. By carefully and properly designing the circuit, current leakage can be suppressed to its minimum. Hence, dynamic power consumption is usually significantly higher than its static counterpart. Some of the techniques that could be adopted to save dynamic power consumption include reducing the supply voltage, clock frequency, clock power, and dynamic effective capacitance. By probing into the activity factors of the design modules, the techniques can be applied to those with high power consumption.

Keywords: dynamic power, static power, switching power, short-circuit power, leakage power, supply voltage, clock frequency, dynamic effective capacitance, switching activity

1. Introduction

More than half a century has elapsed since the three physicists from the AT&T Bell Laboratories—Brattain, Bardeen, and Shockley—invented the first solid-state transistor in December 1947 [1–3]. In comparison with the thermionic triode (which is colloquially known as the vacuum tube), the solid-state transistor is much smaller in size, consumes much lower power, operates at a relatively lower temperature, and exhibits significantly faster response time. Hence, the solid-state transistor swiftly replaced its predecessor as the predominant building block for electronic devices. The inexorable widespread application of solid-state transistors in electronic circuits has triggered a dramatic revolution in the electronic industries.

Today, microchips are built from the solid-state metal-oxide-semiconductor field-effect transistors (MOSFETs). A typical microchip consists of arrays of negative and positive MOSFETs, which are commonly denoted as the NMOS and PMOS transistors, respectively. **Figures 1** and **2** illustrate the symbols and cross-sections of the NMOS and PMOS transistors. As can be seen from the figures, the source and drain terminals

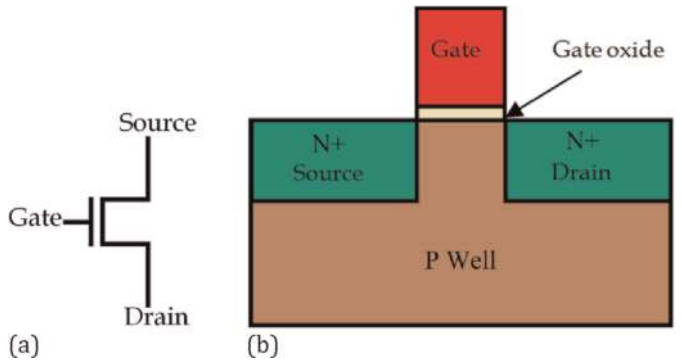

Figure 1.
The (a) symbol and (b) cross-section of a NMOS transistor.

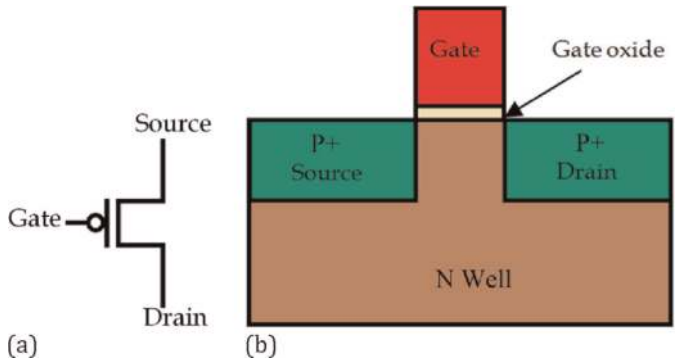

Figure 2.
The (a) symbol and (b) cross-section of a PMOS transistor.

of the NMOS transistor are heavily doped with donator ions, such as phosphorous (P) or arsenic (As), whereas, its body is moderately doped with boron (B) acceptor ions. The PMOS transistor, on the other hand, consists of a high density of B ions at its source and drain and a moderate density of P ions at its body. Since the combination of these two transistors dissipates lower static power and offers higher noise immunity than implementing either the NMOS or PMOS transistor alone, they are both applied concurrently when designing electronic circuits. An electronic circuit that constitutes both the NMOS and PMOS transistors is referred to as the complementary metal-oxide-semiconductor or CMOS.

The insatiable desire to incorporate more functionalities into a microchip has issued a clarion call for a higher number of transistors to be fabricated within it. A state-of-the-art electronic device today, for instance, may be equipped with the fifth-generation (5G) telecommunication, neural engine (NE), augmented reality (AR), cloud computing, facial and speech recognition, and wireless power transmission technologies. These features could only be supported by millions, if not billions, of transistors in the chip. In order to build more transistors into the chip, the size of a transistor has undergone significant reductions over the years [4–6]. By shrinking the size of the transistor, the switching speed of the logic components can also be enhanced, while the operating power can be saved [7]. An advanced microprocessor today possesses more than 50 billion transistors, with technology nodes as small as 5 nm, clock rates of about 5 GHz [3], and an area less than 500 mm^2. Microchips are

now interwoven seamlessly with the fabric of mankind, and, in many aspects, they have become an indispensable necessity to mankind.

2. Power consumption in a CMOS circuit

The total power consumption P_{total} in a CMOS circuit comprises two major components, namely, the dynamic power $P_{dynamic}$ and static power P_{static}, that is,

$$P_{total} = P_{dynamic} + P_{static} \tag{1}$$

$P_{dynamic}$ refers to the power consumed by the circuit when it is performing useful work during the active mode, whereas P_{static} is the power lost due to the leakage current that flows through the transistors when the circuit is inactive [8]. An overview of the different types of power consumption is displayed in **Figure 3**.

2.1 Dynamic power consumption

A CMOS circuit dissipates dynamic power $P_{dynamic}$ in either of the following conditions:

i. When there are switching activities at the nodes. The switching activity (SA) refers to the change of the logic state and the probability that the circuit node switches its state from logic 0 to logic 1 and vice versa, which is known as the activity factor (AF). Clearly, the circuit consumes a higher switching power P_{switch} when the frequency of the transistors toggle increases (i.e., the transistors consist of higher AF).

ii. When both NMOS and PMOS transistors conduct current during signal transitions. When the logic changes its state, there is a short period of time when the PMOS and NMOS transistors are switched on simultaneously. The circuit is, therefore, temporarily short-circuited, resulting in power dissipation P_{short}.

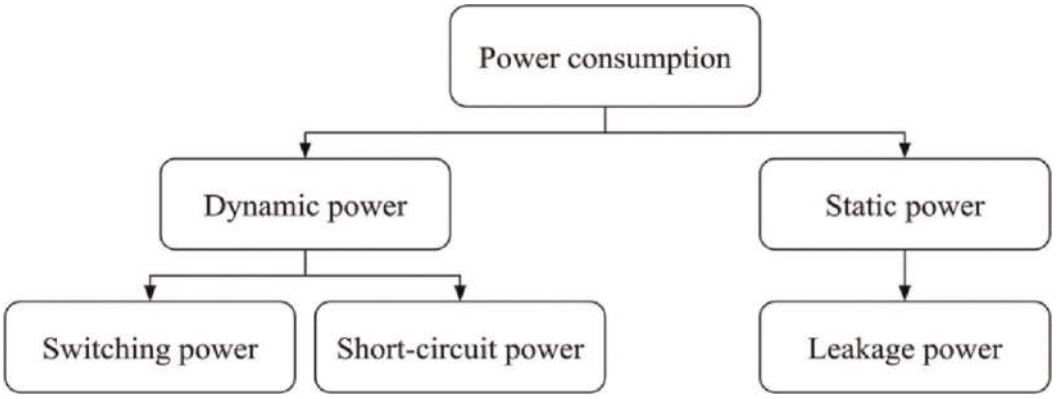

Figure 3.
Different types of power consumption in a CMOS circuit.

Dynamic power dissipation due to the transient short-circuit current path is considerably lower than that caused by the circuits with high switching activities. Hence, emphasis is usually given on finding ways to reduce P_{switch}. Nevertheless, the noise created by the short-circuit current may sometimes be disturbing since it could cause errors in the output logic.

2.1.1 Switching power

In general, the energy delivered to a CMOS circuit can be classified into two parts, namely, the charging and discharging of the load capacitance C_L. To understand how energy delivery takes place, a simple CMOS inverter is shown in **Figure 4**, which is used for illustration.

During the charging phase, the input gate signal switches from logic 1 to 0, and, as a result, the PMOS transistor is switched on, while its NMOS counterpart is switched off. As can be seen in **Figure 4**(a), the load capacitance C_L is connected to the supply voltage via the PMOS transistor, thereby allowing current $I(t)$ to charge C_L to the supply voltage V_{DD}. The energy E_d delivered to C_L is derived in Eq. (2) given below:

$$E_d = \int_0^{\infty} I(t) V_{DD}\, dt. \tag{2}$$

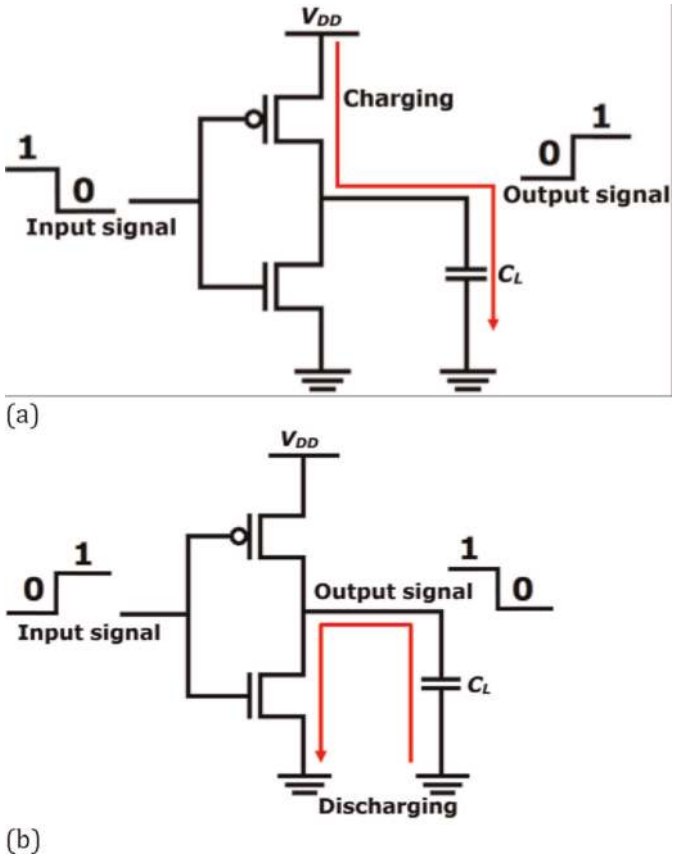

Figure 4.
The (a) charging path (V_{DD} to C_L) and (b) discharging path (C_L to GND*) of the capacitive load in the CMOS circuit.*

Since the current to charge a capacitor C to voltage V can be obtained from

$$I(t) = C\frac{dV}{dt}, \tag{3}$$

E_d in Eq. (2) can, therefore, be expressed as [8].

$$E_d = C_L {V_{DD}}^2. \tag{4}$$

Likewise, the energy stored E_c in C_L during the charging phase for each transition is derived in Eq. (5) given below:

$$E_c = \int_0^\infty I(t)V(t)dt = \frac{1}{2}C_L {V_{DD}}^2 \tag{5}$$

It can be observed between Eqs. (4) and (5) that only half of the delivered energy E_d is stored in C_L, while the remaining half is dissipated in the PMOS transistor. In other words, a CMOS circuit encounters power loss for each logic transition when the current passes the transistors. The changing of the logic state is known as the switching activity. Each time a switching activity occurs for a particular node, the transistors will consume energy. Hence, Eq. (4) rather than Eq. (5) is to be used when determining the switching power consumption of a CMOS circuit. This is because both the energy stored in the load and that dissipated in the transistors have to be taken into account.

When the gate signal changes from logic 0 back to 1, the opposite scenario as that of the charging phase occurs this time, the PMOS transistor is switched off and NMOS switched on. During this discharging phase, the energy stored previously in the load capacitance $E_c = \frac{1}{2}C_L {V_{DD}}^2$ is drained completely to the ground via the NMOS transistor, as seen in **Figure 4**(b).

When deriving Eq. (4), only a single state transition is considered. In reality, however, the scenario of the signal change at the circuit node may be more complicated than that. Since the feeding signal may have more than one transition within a time interval, Eq. (4) has to be multiplied by N times of transitions to obtain the total delivered power E_{dt}, that is,

$$E_{dt} = N \cdot C_L {V_{DD}}^2. \tag{6}$$

Assuming that a circuit node toggles at frequency f_{switch} over a time interval T, N can be written as

$$N = T \cdot f_{switch}. \tag{7}$$

Substituting Eq. (7) into (6), the total energy delivered can be expressed as

$$E_{dt} = T \cdot f_{switch} C_L {V_{DD}}^2. \tag{8}$$

Since power is defined as the rate at which energy is used, the relationship between the switching power P_{switch} and the total delivered power E_{dt} can be described as

$$P_{switch} = \frac{E_{dt}}{T}. \tag{9}$$

Substituting Eq. (8) into (9), the switching power P_{switch} can be written as

$$P_{switch} = f_{switch} C_L V_{DD}^2. \tag{10}$$

Eq. (10) can only be used to accurately calculate P_{switch} as long as the assumption in Eq. (7) holds valid. In most CMOS circuits, however, logic does not really switch at a constant frequency f_{switch}. It is, therefore, more persuasive to express f_{switch} in terms of the product of AF and the clock frequency f_{clk}, that is,

$$f_{switch} = AF \cdot f_{clk} \tag{11}$$

Doing so, P_{switch} in Eq. (10) becomes

$$P_{switch} = AF \cdot f_{clk} \cdot C_L V_{DD}^2 \tag{12}$$

The product of $C_L \cdot AF$ is typically represented by the variable C_{dyn}, which is called the dynamic effective capacitance. Hence, Eq. (12) can be rewritten as

$$P_{switch} = f_{clk} \cdot C_{dyn} V_{DD}^2. \tag{13}$$

According to Weste and Harris [9], activity factor (AF) is defined as the probability that the circuit node changes from logic 0 to logic 1, and this is the only time that the circuit consumes switching power. Therefore, AF is an important element to estimate the power consumption of a circuit. In order to gain a better understanding of AF, assume that the clock is triggered at every single cycle, that is, $f_{switch} = f_{clk}$. From Eq. (11), it can be seen that $AF = 1$. Likewise, AF is found to be 2 for a data signal, which toggles once every two clock cycles. This phenomenon is graphically depicted in **Figure 5**. In most cases, the least significant bit (LSB) and the most significant bit (MSB) contain the highest and lowest AF, respectively.

For a circuit node that switches its logic states in an irregular manner, AF can be determined by multiplying the probability the node switches to logic 0, P_f^0, with the probability it switches to logic 1, P_f^1, that is,

$$AF = P_f^0 \times P_f^1 \tag{14}$$

For instance, a switching function expression is given as $F = \overline{A + BC + \overline{BC}}$. The truth table of F is shown in **Table 1**. Out of the eight combinations of input values in

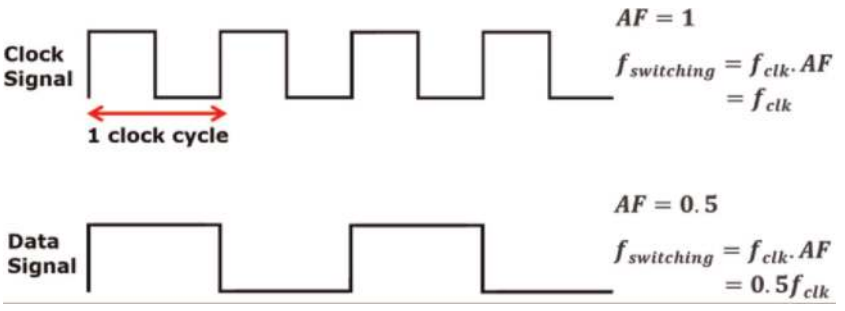

Figure 5.
Clock signal (AF = 1) and data signal (AF = 0.5).

A	B	C	F(A, B, C)
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	0

Table 1.
Truth table of $F = \overline{A + BC + \overline{B}\,\overline{C}}$.

the truth table, two produce logic 1 at output *F,* while the remaining ones produce logic 0. Hence, P_f^0 and P_f^1 can be obtained as $\frac{6}{8}$ and $\frac{2}{8}$, respectively. Substituting these values into Eq. (14), *AF* is then found to be 0.1875. This is to say that, the probability that the circuit is active is only 0.1875, which is clearly low. Comparing this value with the frequency of occurrence for logic 1 found in the truth table, it can be seen that *AF* gives a good indication of the active rate of the circuit.

2.1.2 Short-circuit power

Since it takes time for the parasitic capacitance to charge and discharge, the signal fed to a circuit does not change its logic state instantly. The input signal consists of the finite rise and fall times by this means. Unlike the switching power dissipation, where only one of the transistors is switched on at a time, short-circuit power dissipation P_{short} is induced from the concurrent activation of both the NMOS and PMOS transistors. When the logic changes its state, there is a short window of time where the PMOS and NMOS transistors are switched on simultaneously. A direct current path connecting V_{DD} to the ground is produced within this interval, resulting in short-circuit power dissipation P_{short}. As can be seen in **Figure 6**, the short-circuit current that passes both the PMOS and NMOS transistors during the transition state does not contribute to the charging and discharging of the load capacitance. The power

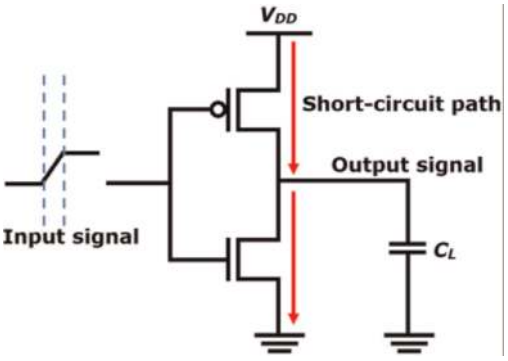

Figure 6.
Short-circuit path (V_{DD} to GND*) in a CMOS circuit.*

produced does not deliver any meaningful activities at the output and is therefore wasted. The short-circuit power P_{short} can be mathematically expressed as

$$P_{short} = T_{sc} \cdot V_{DD} \cdot I_{peak} \tag{15}$$

where T_{sc} is the rising or falling time of the input signal and I_{peak} is the peak current, which could be estimated from the transistor size and technology process.

2.2 Static power

Static power P_{static} refers to the power lost when the CMOS circuit is dormant. The main culprit of P_{static} is the leakage current, which exists mainly because of the short-channel effects [10]. As the technology node continues to reduce toward the sub-nanometer range, leakage current has become a major problem. In 2011, the severity of the leakage reached the brink, which prompted Intel Corporation to introduce the 22 nm tri-gate transistor. The tri-gate transistor is more popularly referred to as the FinFET, owing to its protruding drain and source structures, which resemble the fin of a fish. In comparison with the planar MOSFETs, the FinFET has better control of the current flow, thereby reducing leakage [11].

Among the short-channel effects that contribute predominantly to the P_{static} dissipation are the sub-threshold leakage current and the gate leakage current [12]. Sub-threshold leakage current is the weak current that exists between the source and drain terminals during the off-state of the transistor, as a result of the weak inversion layer at the oxide–substrate interface. This phenomenon occurs when the gate voltage is lower than the threshold voltage V_{TH}. The sub-threshold leakage increases exponentially as the feature size continues to shrink [13]. This is mainly caused by the reduction of the V_{TH}, which is also scaled down accordingly.

When the size of the transistor decreases, the oxide layer is thinned as well. The oxide thickness is continuously thinned until a certain extent, an undesired electric field is induced at the oxide–substrate interface whenever voltage is applied at the gate terminal. The electric field increases the probability of electrons to tunnel through the oxide layer from the channel region into the gate and vice versa [14], leading to gate leakage current. Although its impact is less severe compared to the sub-threshold leakage, current leakage by virtue of this mechanism has gradually exacerbated when the technology node penetrates the nanometric regime.

The equation that describes static power dissipation can be expressed as,

$$P_{static} = V_{DD} \cdot I_{leakage} \tag{16}$$

where $I_{leakage}$ denotes the total leakage current.

3. Dynamic power optimization

With an increasing number of features being installed into a microchip today, higher computing power is drawn by electronic devices. Power consumption has, therefore, become a key concern in a CMOS circuit designs. Clearly, it is imperative to employ effective approaches to cut down the usage of power in microchips.

The first step for power optimization is to analyze the overall power consumed by a CMOS circuit. By substituting Eqs. (13), (15), and (16) into Eq. (1), the total power consumption P_{total} can be obtained as

$$P_{total} = \left(f_{clk} \cdot C_{dyn} \cdot {V_{DD}}^2\right) + \left(T_{sc} \cdot V_{DD} \cdot I_{peak}\right) + \left(V_{DD} \cdot I_{leakage}\right). \tag{17}$$

Upon inspection, it can be observed that P_{total} is dictated by six power components, namely, f_{clk}, C_{dyn}, V_{DD}, T_{sc}, I_{peak}, and $I_{leakage}$. By carefully and properly designing the logic circuit, P_{short} and P_{static} can usually be minimized, if not completely suppressed. Hence, only clock frequency f_{clk}, dynamic effective capacitance C_{dyn}, and supply voltage V_{DD} are typically adjusted to optimize the power consumption of the circuit. Although modifying any of these three components may result in power saving, precaution is to be heeded since some approaches may also impose adverse effects on the circuits. The reduction of V_{DD}, for example, yields a quadratic effect on diminishing the usage of power. Doing so, however, may also impair the performance of the circuit. This approach is generally not recommended unless there is a need to switch the device from high performing to high power saving. Similarly, reducing the clock frequency f_{clk} may not necessarily be effective in curtailing power consumption because the system has to operate for a longer period of time when fed with the same load. Tuning C_{dyn} is perhaps one of the most popular options since it involves decreasing either the parasitic capacitance or the activity factor AF for idle nodes. A summary of some of the existing methods adopted to optimize power usage is presented in the subsequent sections. The first three methods discussed in the subsequent sections are related to the adjustments of the clock frequency f_{clk} and supply voltage V_{DD}, while the remaining ones deal with the dynamic effective capacitance C_{dyn}.

3.1 Dynamic frequency scaling

Weissel and Bellosa [15] proposed an event-driven clock scaling approach for dynamic power management. In their work, schedulers were utilized to determine the appropriate clock frequency for each thread. Finally, the frequency of the dedicated applications can be adjusted based on the recurrent analysis of the thread-specific performance profile. Their analysis showed that at least 37% of energy can be saved with a performance loss of less than 10% when tested on the Intel XScale architecture.

Although this approach shows positive results in power saving, it may suffer from longer application execution time, since the frequency is reduced. As a consequence of this, applications may be corrupted if certain deadlines were missed.

3.2 Multiple supply voltages

Chabini et al. [16] in their study proposed to minimize the dynamic power consumption under performance constraints by scaling down the supply voltage of computational elements off critical paths. In their work, the mixed-integer linear programming (MILP) method was first used to determine a schedule of the computational blocks that will lead to the maximum reduction of dynamic power consumption with designed performance constraints. Once the valid periodic schedule was computed, registers were inserted into the circuit to preserve the behavior of the original circuit. When compared to the design using the highest supply voltages, power reduction factors as high as 69.75% were obtained from their work.

Since multiple voltage domains are involved, multiple power grid structures are required. Power and floor plannings must, therefore, be implemented with care when employing this approach to optimize power consumption.

3.3 Clock gating for clock tree

According to Donno et al. [17], the power drawn by the clock tree in advanced microchips tends to dominate. Hence, they introduced a clock-gating approach that could be adopted at the register transfer level (RTL) to reduce clock power. In the algorithm that they developed, a clock tree topology, which balanced the reduction in clock switching against clock and activation function capacitive loading estimates, was first built. Clock-gating logic was then incorporated into the tree, achieving a balance between its power consumption and the power on the gated clock sub-tree. The physical and functional information was taken as inputs to generate a clock netlist at the output. The netlist was then used to update the structural description of the design. The results show that the capability of their approach in power saving is 75% better than conventional clock-gating methods.

The work proposed in ref. [17] focused on the calculation of the active and idle time frames of different registers and inserting the clock gating logics into the netlist. Since the algorithm implemented in the work did not account for an optimized location for the gating logic, the registers may end up being placed far apart after the netlist is updated. A larger clock network size and higher power consumed by the clock tree may, therefore, ensue.

3.4 Downsizing gates

Gate sizes are proportional to the parasitic capacitances. By this means, dynamic effective capacitance C_{dyn} could be reduced when gates are downsized. By selectively downsizing the gates of a circuit, Aizik and Kolodny [18] demonstrated that dynamic and leakage energy dissipations can be reduced. Doing so, however, may lead to an increase in speed delay. This is to say that the operating speed of a circuit can be traded off in exchange for power reduction. The findings reveal that 25% of dynamic power can be saved for circuits in 32-nm technology when the delay constraint is relaxed by 5%.

3.5 Interconnect-power reduction

A circuit consumes switching power P_{switch} when the interconnection capacitances are charged and discharged. The analysis in ref. [19] showed that the interconnect power occupied more than half of the total dynamic power consumption $P_{dynamic}$, with 90% of it contributed from 10% of the interconnections. To reduce C_{dyn}, larger wire spacing and minimal length routing were implemented for the high-power consuming interconnects. The researchers re-configured the interconnects without sacrificing the area and timing degradation and the results that they obtained showed that $P_{dynamic}$ was saved by 14%.

3.6 Clock network optimization

Lu et al. [20] demonstrated that power consumption is affected by the size of the clock network. They developed an algorithm that navigated the registers' locations during cell placement. When performing the navigation process, the Manhattan ring-based register guidance, the center of gravity constraints for registers, pseudo pin and

net, and register cluster contraction were observed. The clock net wirelength was decreased by 16–33%, with no more than 0.5% increase in signal net wirelength.

However, precautions must be taken when adopting this approach, particularly for circuits with high densities. This is because, reducing the clock network size may increase the risk of routing congestion and this may lead to a poor signal net to wirelength.

3.7 Net ordering and wire space optimization

To optimize power consumption, Moiseev et al. [21] endeavored to reduce the capacitance for the most active nodes within parallel bundles. This can be achieved by finding the best arrangement of adjacent signals in the bundle and rearranging the positions of the wires so that the most active signal shares the smallest cross-capacitance. The approaches that they adopted are net ordering and wire space optimization. In their work, signals with high switching activity (*SA*) share a relatively larger space than those with lower *SA* (as seen in **Figure 7**). Further, the LSB is proposed to be

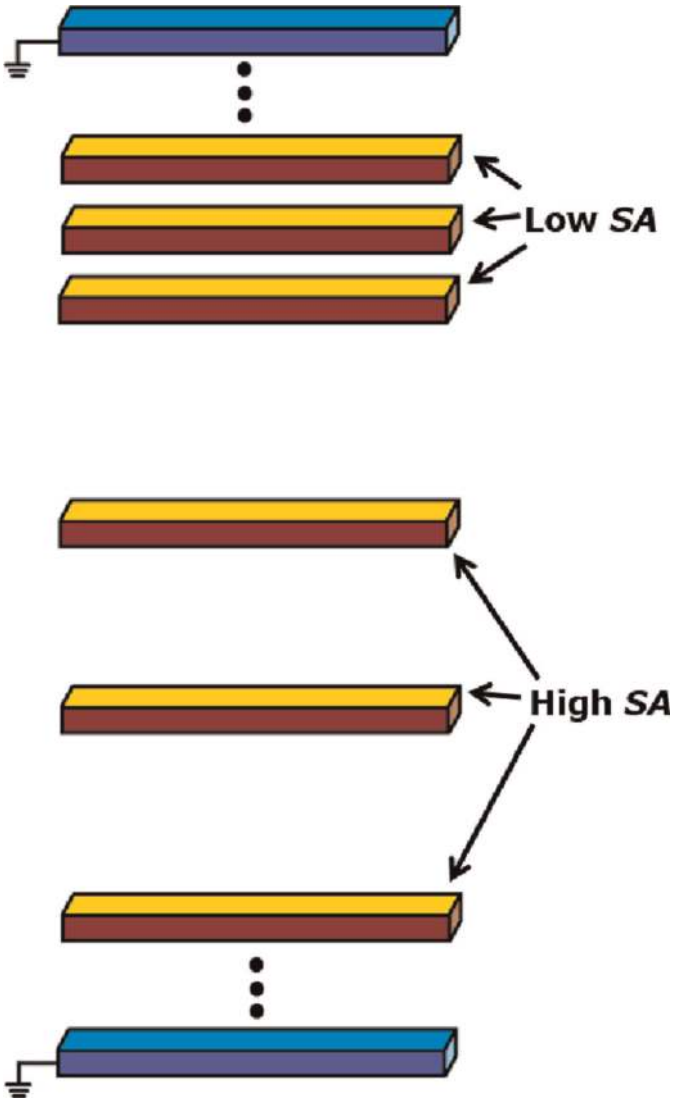

Figure 7.
Wires connected to signals with high SA share a relatively larger space than those with lower SA.

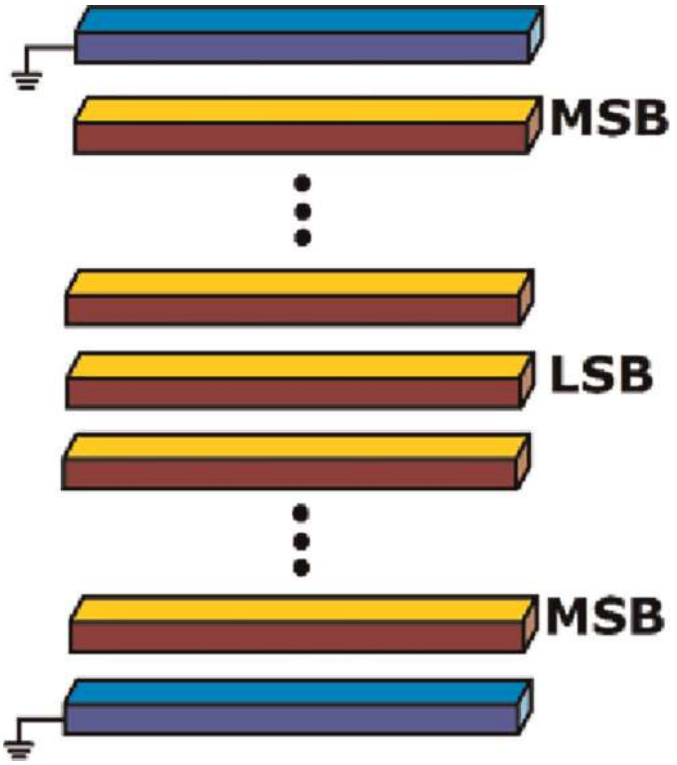

Figure 8.
Net ordering. The LSB (highest switching activity signal) is positioned at the center, while the MSB (lowest switching activity signal) is positioned near the sidewall.

placed at the center of the bundle and the MSBs at the ends, as depicted in **Figure 8**. This spacing and ordering optimization method was applied on industrial layouts of 65 nm process technology and the power saved ranged from 9 to 37%.

3.8 Leaving unused routing conductors floating

To reduce the effective coupling capacitance, Huda, Anderson, and Tamura [22] proposed to leave routing conductors adjacent to those used by timing critical or high activity nets floating. The purpose of doing so is to ensure that the original coupling capacitance among the conductors stays in series with other capacitances in the circuit. It is to be noted that, the equivalent capacitance of a chain of series capacitances is lower. As can be seen in **Figure 9**, tri-state buffers were used to disconnect the unused conductors. During high switching conditions, the tri-state buffer is allowed to be used as a normal buffer, without the loss or delay of data. The results show that the interconnect dynamic power was reduced up to approximately 15.5%, with a critical path degradation of about 1% and a total area overhead of about 2.1%.

4. Switching activity

The power optimization techniques discussed in the previous section involve redesigning the circuit topology. Most of these techniques are conducted based on the assessment of the switching activity. Switching activity *SA* comprises two basic

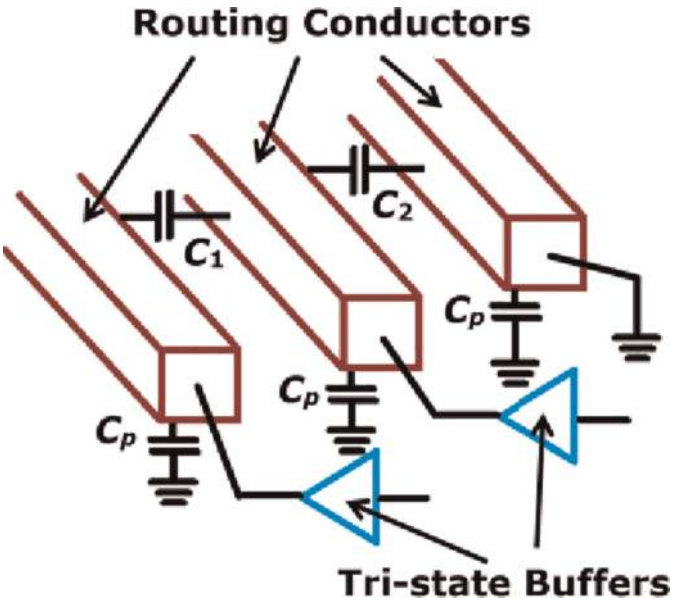

Figure 9.
The unused adjacent routing conductors are left floating, by connecting them to tri-state buffers. C_1 *and* C_2 *denote the coupling capacitance, while* C_p *denotes the plate capacitance (i.e., the parasitic capacitance formed between the substrate and the metal layers).*

elements, namely, (i) the toggle rate and (ii) static probability. The toggle rate gives an indication of the frequency the node toggles for a specified interval, and it is usually measured in millions of transistors per second. The static probability, on the other hand, predicts the logic state of the signal. An *SA* that shows 0.4 static probability, for example, suggests that the signal gives a logic 1 for 40% of the time and a logic 0 for the remaining 60%. **Figures 10** and **11** illustrate two sets of signals with opposite scenarios—the signals in **Figure 10** consist of identical toggle rates but different static probabilities, whereas those in **Figure 11** show different toggle rates, but the same static probability.

Switching activity is an important reference tool when performing power analysis. By reading the *SA*, critical design blocks that consume high power can be identified. The details of the circuit, such as where and when it has the lowest and highest toggle rate, can also be ascertained. This information is important in deciding the appropriate approach to save power.

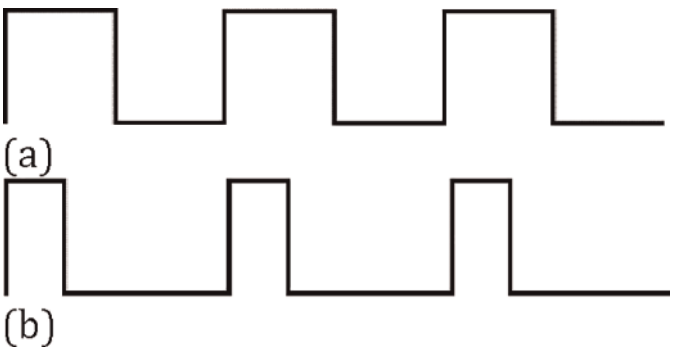

Figure 10.
The pulse trains in (a) and (b) consist of identical toggle rate but different static probabilities. For the pulse train in (a), toggle rate = 6 and static probability = 0.5; and that in (b), toggle rate = 6 and static probability = 0.25.

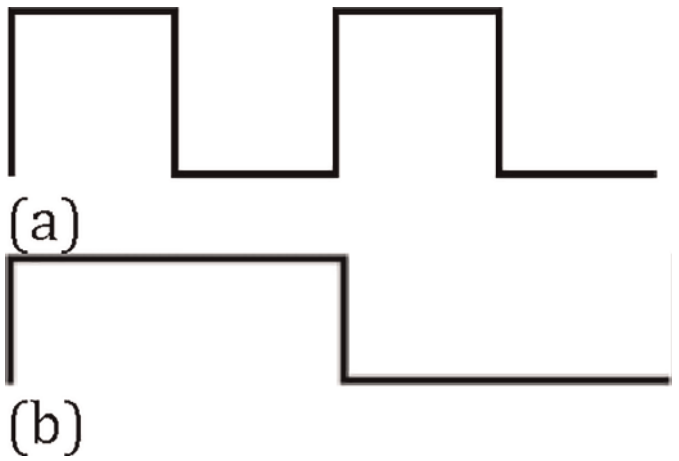

Figure 11.
The pulse trains in (a) and (b) consist of identical static probability but different toggle rates. For the pulse train in (a), toggle rate = 4 and static probability = 0.5; and that in (b), toggle rate = 2 and static probability = 0.5.

5. Conclusion

In this chapter, the power consumed by CMOS circuits is expounded. The total power consumption P_{total} in a CMOS circuit can be classified into two types—viz, the dynamic power $P_{dynamic}$ and static power P_{static}. Dynamic power refers to the power dissipated by the circuit when it is operating. It is induced by the switching activities, which take place at the nodes, and the short-circuit current formed at the transition state of the logic switch. Static power, on the other hand, occurs when the circuit is idle. It is caused mainly by the subthreshold and gate leakage currents. Since dynamic power takes up a significant fraction of the overall power consumption, different approaches have been developed to minimize it. The approaches focus on the reduction of the supply voltages, clock frequencies, or dynamic effective capacitance. By studying the activity factors of the design modules, the approaches can be applied to those with high power consumption.

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